

56-Pin Quad Flatpack No-Lead Logic Package

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ABSTRACT

Texas Instruments (TI) Quad Flatpack No-Lead (QFN) 56-terminal package complies with JEDEC standard MO-220, allows for board miniaturization, and holds several advantages over traditional SOIC, TQFP, TSSOP, and TVSOP packaging. This package, designated RGQ by TI, physically is smaller than traditional leaded solutions, has a smaller routing area, improved thermal performance, and improved electrical parasitics. Additionally, the absence of external leads eliminates bent-lead concerns and issues. This QFN package is packed to industry-standard tape-and-reel specifications. Package marking is in accordance with TI standards.

Contents

1	Introduction	2
2	Industry Requirements	3
3	Physical Description	3
	3.1 Package Characteristics	3
	3.2 Package Nomenclature	5
	3.3 Electrical Performance	5
	3.4 Power Dissipation	6
	3.5 Board-Level Reliability	9
	3.6 Package Reliability	10
4	Board-Level Assembly	11
	4.1 PCB Design Guidelines	11
	4.2 Stencil Design	12
	4.3 Component Placement and Reflow	13
	4.4 Rework	15
5	Tape and Reel	16
	5.1 Material Specifications	16
	5.2 Shipping Labels	18
	5.3 Dry-Pack Requirements for Moisture-Sensitive Material	18
6	Symbolization	18
7	Test Sockets	19
8	Features and Benefits	19
9	Conclusion	20
10	Acknowledgments	20

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11	References	20
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List of Figures

1.	56RGQ Package Drawing	4
2.	Improvement in Inductance and Capacitance of RGQ vs Alternative Packages (Modeled Data)	5
3.	56RGQ θ_{JA} vs Traditional Package Alternatives	7
4.	The Effect of Thermal Vias	7
5.	Derating of 56RGQ per JESD 51-3 (Low Effective Thermal Conductivity) Board	8
6.	Derating of 56RGQ per JESD 51-5 (High Effective Thermal Conductivity) Board	8
7.	Derating of 56RGQ per JESD 51-7 (High Effective Thermal Conductivity) Board	9
8.	Recommended Land-Pad Design for the 56RGQ	11
9.	Recommended Stencil Design for the 56RGQ	13
10.	Generic SnPb-Paste Reflow Profile (Image Courtesy of Senju Metal Industry Co., Ltd.)	14
11.	Carrier Tape Drawing	17
12.	Reel Drawing and Specifications	17
13.	Pin-1 Orientation of QFN Packages	18

List of Tables

1.	56RGQ Physical Attributes	3
2.	56RGQ Compared to Alternative Package Solutions	5
3.	56RGQ Thermal Summary	6
4.	Package-Reliability Test Matrix	10
5.	Carrier-Tape Dimensions in Millimeters	16
6.	Device-Marking Guidelines	19

1 Introduction

The Texas Instruments (TI) 56-pin QFN package, designated RGQ, is a JEDEC standard MO-220-compliant leadless package that has several advantages over traditional SOIC, TQFP, TSSOP, and TVSOP packaging. The RGQ package physically is smaller than traditional leaded solutions, has a smaller routing area, improved thermal performance, and improved electrical parasitics over leaded alternatives. Additionally, the absence of external leads eliminates bent-lead concerns and issues. The RGQ package was developed for the 13-bit to 26-bit registered-buffer function, SN74SSTV16859, to meet the requirements and board-size restrictions of the memory industry's newest low-profile DDR registered dual-inline memory module (RDIMM). The RGQ package is a two-device alternative to the single-device BGA solution for DDR RDIMM applications in situations where simpler printed circuit board (PCB) fabrication is required, due either to capability or to assembly constraints. At this time, the SN74SSTV16859 is the only device offered in the RGQ package. More devices will be released as market interest dictates.

2 Industry Requirements

The consumer-electronics industry is focused on product miniaturization as a result of consumer demands for smaller and better-performing products. DRAM modules have migrated in the same direction as most electronic products. The latest low-profile, stacked, TSOP-based memory modules have eliminated the 64-pin TSSOP package previously used for registered buffers, in lieu of either BGA or QFN, to meet the DIMM height reduction from 1.7 inches to 1.2 inches. To attain smaller products, electronic manufacturers require smaller packages (area and height) to reduce board size and weight. Improved heat dissipation and electrical parasitics also will be required as the packages and systems shrink in size. Heat dissipation is important because packages with better thermal dissipation typically can run at faster speeds, if required, and packages with better electrical parasitics generally have lower signal noise. Both of these are important for high-end processors to deliver a stable, clean signal output. TI has selected the RGY package as one alternative to address these industry requirements.

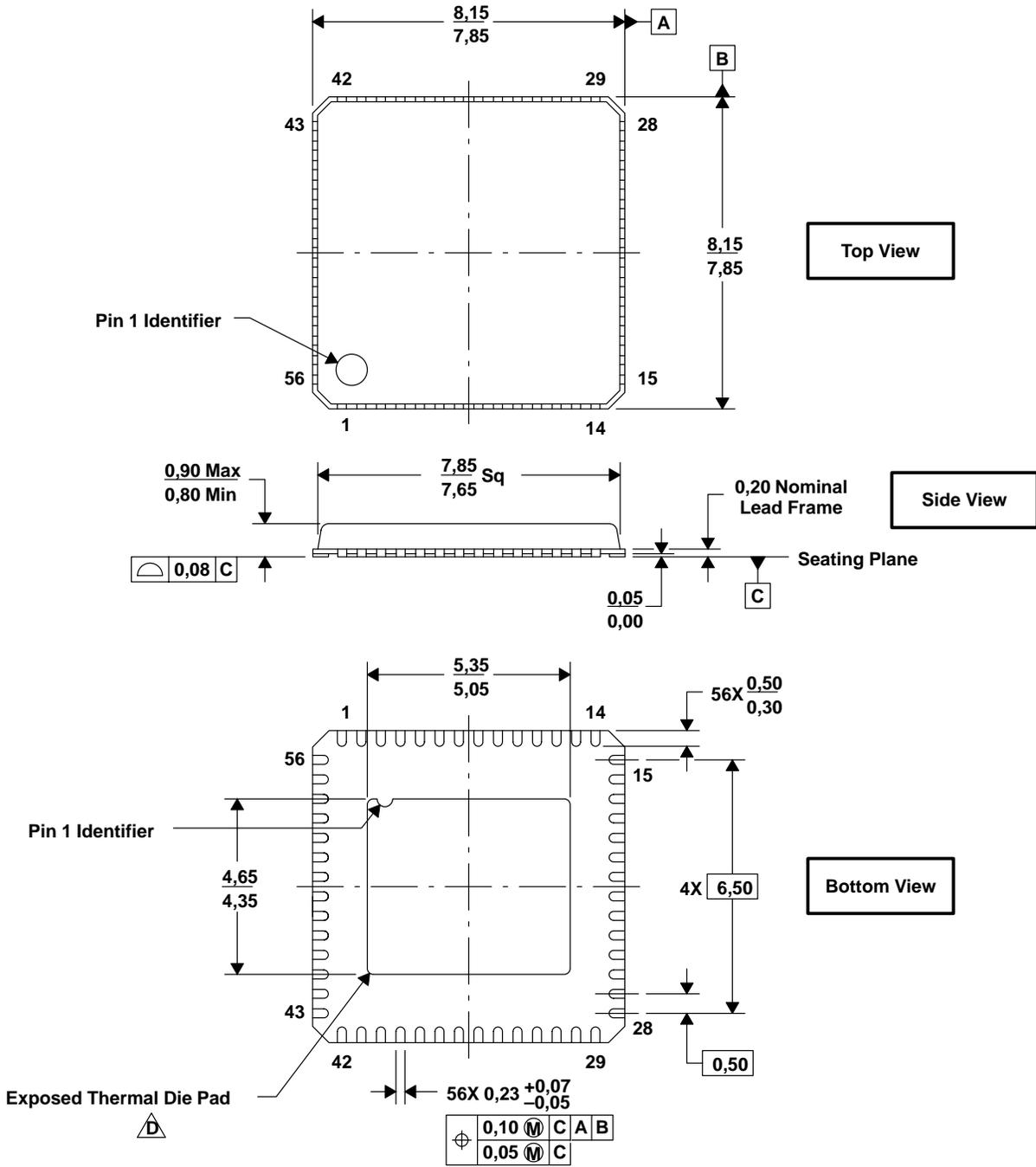
3 Physical Description

3.1 Package Characteristics

Table 1 summarizes attributes of the TI 56-pin QFN package (RGQ). Figure 1 shows the package dimensions, and Table 2 provides a comparison of RGQ physical attributes to alternative package solutions.

Table 1. RGQ Physical Attributes

Attribute	56RGQ
Pin count	56
Square/Rectangular	Square
Package length (mm) nominal	8.0
Package width (mm) nominal	8.0
Lead finger length (mm) nominal	0.40
Lead finger width (mm) nominal	0.23
Exposed pad length (mm) maximum	5.20
Exposed pad width (mm) maximum	4.50
Package thickness (mm) nominal	0.90
Package weight (g)	0.150
Moisture sensitivity	Level 3, 235°C
Lead finish	SnPb
Shipping media, tape and reel (units/reel)	2000



Dimensions are in millimeters.

Figure 1. 56RQ Package Drawing

Table 2. 56RGQ Compared to Alternative Package Solutions

Attribute	64-TSSOP (DGG)	56-TSSOP (DGG)	56-TVSOP (DGV)	64-TQFP (PAG)	56-QFN (56RGQ)
Length (mm)	17.00 ±0.10	14.00 ±0.10	11.30 ±0.10	12.00 ±0.20	8.00 ±0.15
Width (mm)	8.10 ±0.20	8.10 ±0.20	6.40 ±0.20	12.00 ±0.20	8.00 ±0.15
Height (mm), max	1.20	1.20	1.20	1.20	0.90
Pitch (mm)	0.50	0.50	0.40	0.50	0.50
Footprint (mm ²)	137.70	113.40	72.32	144.00	64.00
Weight (g)	0.250	0.235	0.135	0.240	0.150
Area savings	53.5%	43.6%	11.5%	55.6%	–

3.2 Package Nomenclature

Generically, this package is referred to in this application report as QFN. The TI package designator for this 56-pin QFN package is RGQ. The designator is extended to RGQR to designate packing for shipment in tape and reel, as explained in section 5.

3.3 Electrical Performance

The unique construction of QFN packages reduces both inductance and capacitance. The exposed thermal die pad of the QFN package is at board level, following assembly, which minimizes inductance when grounded. Figure 2 compares the percentage improvement of the RGQ package to other packaging options. These models take into account the exposed pad and the fact that the pad is grounded to the board ground.

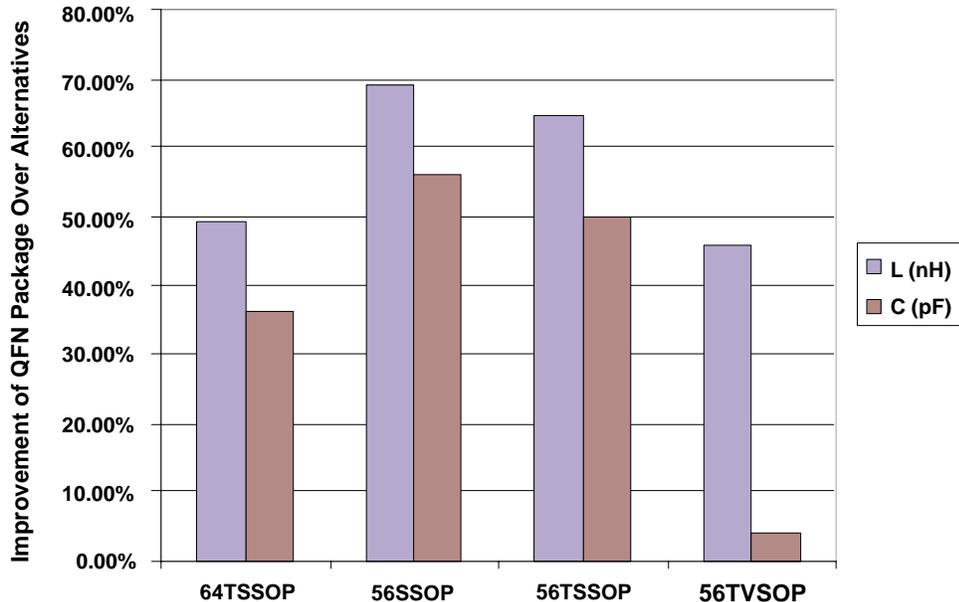


Figure 2. Improvement in Inductance and Capacitance of RGQ vs Alternative Packages (Modeled Data)

3.4 Power Dissipation

When thermal dissipation is crucial, the QFN package has an advantage over standard dual- and quad-leaded packages. The leadframe thermal die pad is exposed at the bottom of the package and should be soldered to a properly designed thermal pad on the PCB. This provides a more direct heat-sink path from the die to the board, and the addition of thermal vias from the thermal pad to an internal ground plane increases power dissipation dramatically. Soldering the exposed pad also significantly improves board-level reliability during temperature cycling, drop testing, package shear, and similar board-level tests.

Unless otherwise stated, the following modeled data assumes that the exposed thermal die pad of the package is soldered to the thermal pad on the PCB. The standards used for these models are available for downloading at <http://www.jedec.org/download/default.cfm>. Customers are highly encouraged to familiarize themselves with the standards mentioned in the following paragraphs when comparing the power-dissipation performance of similar or alternative packages to ensure that the comparison is made on equivalent terms.

It is important to understand that the following data is intended for comparing the RGQ package to alternative packages under similar conditions. System-level performance is heavily dependent upon board thickness and size, metal layers, component spacing (thermal coupling), airflow, and board orientation in the system. The model data provided can be used to construct system-level thermal models to predict performance in a particular system, but does not reflect the package's performance in any system, as listed, except in accordance with the standards under which it was modeled.

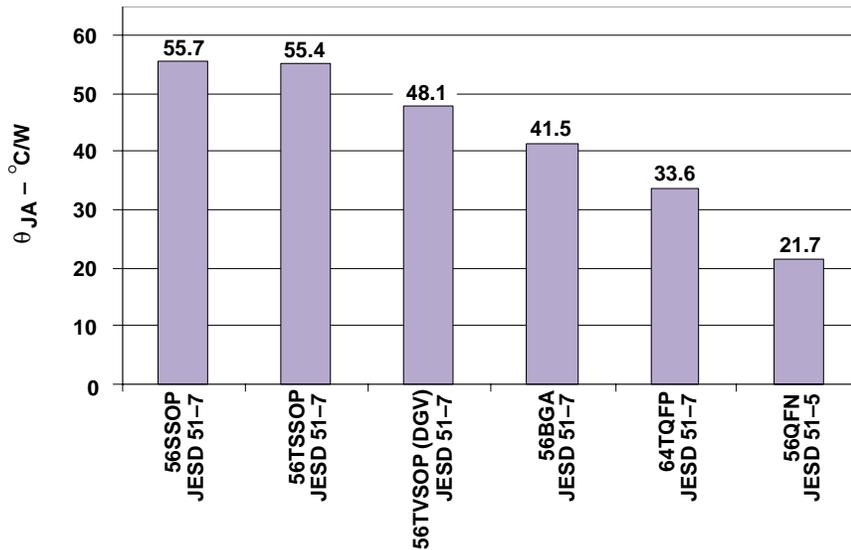
For the data in Table 3, values are given for each standard. All standards use the same land pad and thermal pad design; however, they differ in internal board construction. Test cards complying with JESD 51-3 have no internal metal layers and are, naturally, the worst case in performance. JESD 51-5 has two internal 1-oz. copper-metal layers with thermal vias connecting the upper layer to the thermal pad. These vias are 0.30-mm diameter and are spaced 1.2 mm, center to center. The vias are allowed to populate only the region defined by the perimeter of the thermal pad and cannot extend beyond the perimeter. JESD 51-7 test cards have the same two metal layers as the JESD 51-5 test card, but no vias are allowed. These three standards give a wide range of conditions under which alternative packages can be compared.

Table 3. 56RGQ Thermal Summary

Airflow (linear feet/minute)	θ_{JA} per JESD 51-3 (°C/W)	θ_{JA} per JESD 51-5 (°C/W)	θ_{JA} per JESD51-7 (°C/W)
0	113.8	21.7	51.8
150	104.6	20.1	49.9
250	99.2	19.39	48.8
500	91.5	18.42	47.2
θ_{JB}	N/A	10.5	31.4
θ_{JC}		2.12	

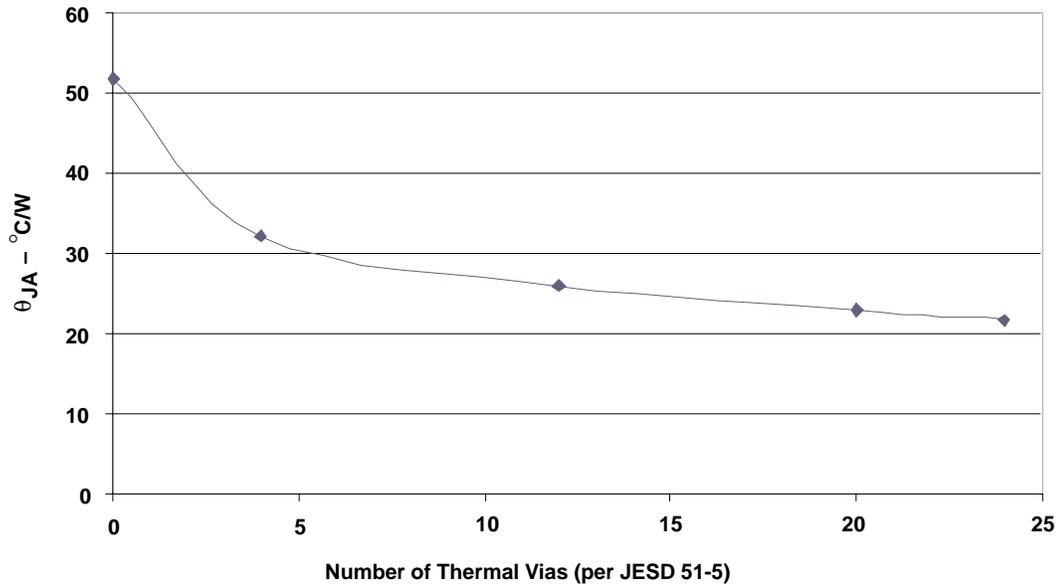
NOTE: Modeled data, assuming maximum junction temperature of 125°C and die size of 165 × 193 mils. Junction-to ambient resistance is a function of many variables, and different die sizes produce different resistance values.

Comparing θ_{JA} values of traditional packages to 56RGQ performance shows the advantage of the thermal-via pad design. If 56RGQ performance is compared per JESD 51-5 and JESD 51-7, the use of thermal vias results in a θ_{JA} value that is 58.7% lower. Figure 3 compares θ_{JA} values for alternative packages to the 56RGQ. JESD 51-5 covers none of the alternative packages because they are not capable of the direct-attach method described in the QFN package standard. Figure 4 shows the effect of the number of thermal vias used vs θ_{JA} .



NOTE: 56RGQ modeled data, assuming maximum junction temperature of 125°C and die size of 165 × 193 mils. For all other packages, assume same junction temperature and maximum die sizes.

Figure 3. 56RGQ θ_{JA} vs Traditional Package Alternatives



NOTE: Modeled data, assuming maximum junction temperature of 125°C and die size of 165 × 193 mils

Figure 4. The Effect of Thermal Vias

Figures 5, 6, and 7 show the theoretical maximum power dissipation per the indicated JEDEC test standards.

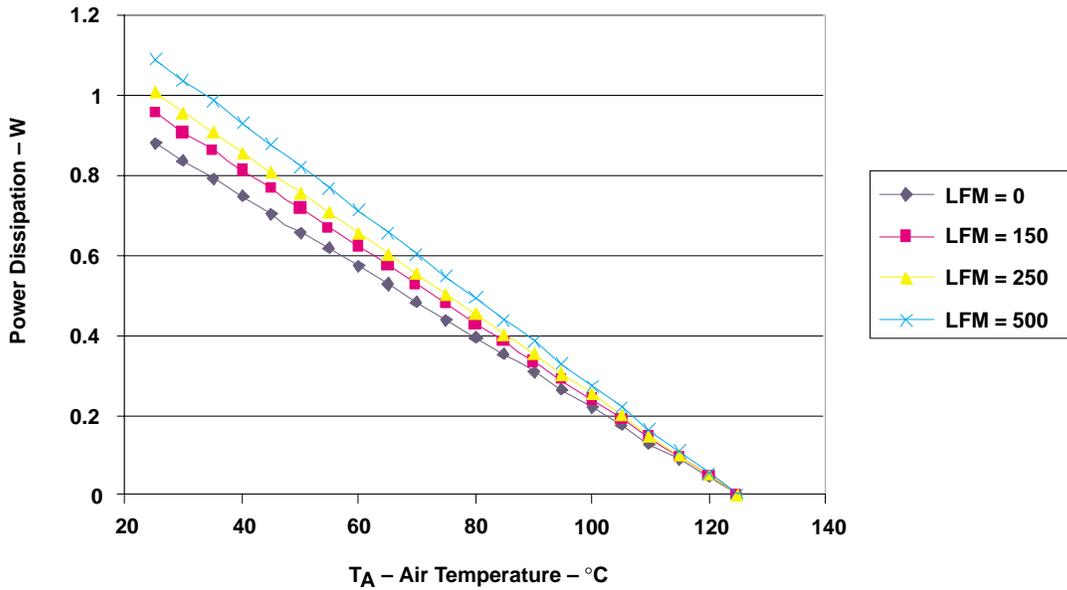


Figure 5. Derating of 56RGQ per JESD 51-3 (Low Effective Thermal Conductivity) Board

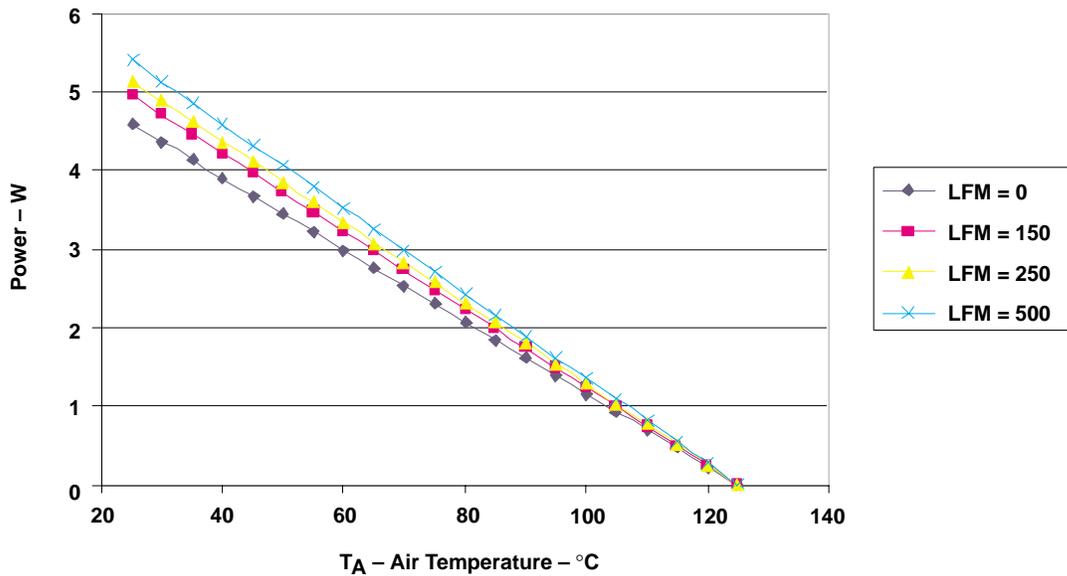


Figure 6. Derating of 56RGQ per JESD 51-5 (High Effective Thermal Conductivity) Board

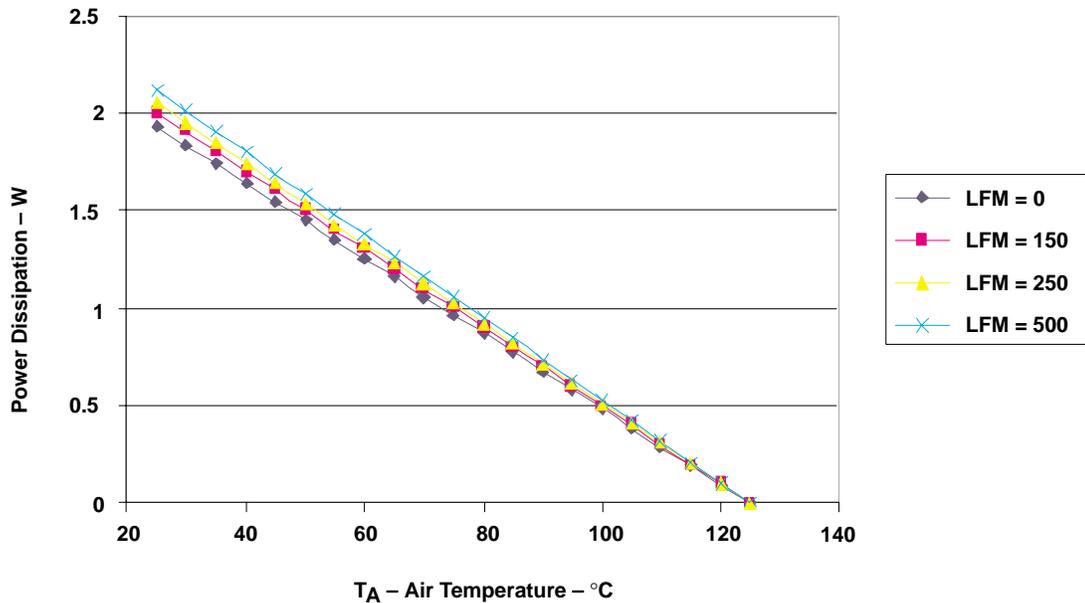


Figure 7. Derating of 56RGQ per JESD 51-7 (High Effective Thermal Conductivity) Board

3.5 Board-Level Reliability

When soldered, the QFN exposed-pad design acts as a package anchor, significantly increasing the board-level reliability over that of an LCC or other leadless packages. The exposed pad must be soldered to provide the structural integrity expected by industry, as well as optimal thermal performance.

There is a significant amount of historical data available on QFN board-level reliability. Various sizes of QFN packages (nonpullback lead design) have shown good performance in temperature cycling, key push, vibration, drop, and three-point bending tests.

A 10 × 10 mm QFN package (3.81- × 3.81-mm die) passed 2600 thermal cycles when mounted to a 0.8-mm-thick FR-4 PCB with NiAu pad finish and SnPb eutectic solder paste. The temperature cycle was per IPC-9701, TC1 (−40°C to 125°C), one cycle per hour. Similar, or better, results are expected for the 8.0- × 8.0-mm 56RGQ when testing is complete. The failure criterion was a resistance increase to 0.5 Ω, or more, for 200 ns or longer.

It is important to solder the exposed pad to the PWB for three reasons. First, the exposed pad is used as an electrical ground for the 56RGQ package. Second, soldering the exposed die thermal pad results in an approximate 60% increased package life during thermal cycling tests. Last, thermal dissipation is vastly improved.

3.6 Package Reliability

The 56RGQ package was qualified at moisture-sensitivity-level 3 (MSL3/235°C) using standard JEDEC-defined test methods. Table 4 shows the results of the qualification testing. The qualification device was an SN74SSTV16859.

Table 4. Package-Reliability Test Matrix

Test	Test Conditions	Lot 1 Pass/Fail	Lot 2 Pass/Fail	Lot 3 Pass/Fail
Steady-state life test†	150°C, 500 hours	40/0	40/0	40/0
Biased HAST†	130°C/85% RH, 100 hours	77/0	77/0	77/0
Unbiased HAST†	130°C/85% RH, 100 hours	77/0	77/0	77/0
Thermal shock†	-65°C/150°C, 1000 cycles	77/0	77/0	77/0
High-temperature storage†	170°C, 420 hours	45/0	45/0	45/0
Solderability	8-hours steam age	10/0	10/0	10/0
Flammability	UL94 V0	5/0	5/0	5/0
Flammability	IEC	5/0	5/0	5/0
X-ray		5/0	5/0	5/0
Physical dimensions	Per package drawing	5/0	5/0	5/0
Salt atmosphere		22/0	22/0	22/0
Moisture-sensitivity measurement	Level 3, 235°C peak			
	Electrical test	12/0	12/0	12/0
	40X visual inspection	12/0	12/0	12/0
	Delamination	12/0	12/0	12/0
	Cross-sectional analysis	12/0	12/0	12/0
Bond strength	Ball shear	30 grams, minimum	45/0	45/0
	Wire pull	3.0 grams, minimum	45/0	45/0
	Die shear	2.5 kg minimum	5/0	5/0
Manufacturability	Per manufacturer's site specification	Pass	Pass	Pass
Visual/mechanical inspection	Per manufacturer's site specification	Pass	Pass	Pass

† Denotes preconditioning sequence Level 3, defined as:

1. Storage at 125°C for 24 hours
2. 85°C/85% RH for 168 hours with no bias
3. Board mount (if applicable)
4. Three cycles of a 235°C IR solder reflow simulation and a 5-minute room-temperature delay
5. Clean the device with an isopropyl alcohol rinse, a de-ionized water rinse, and a one-hour drying period at 25°C

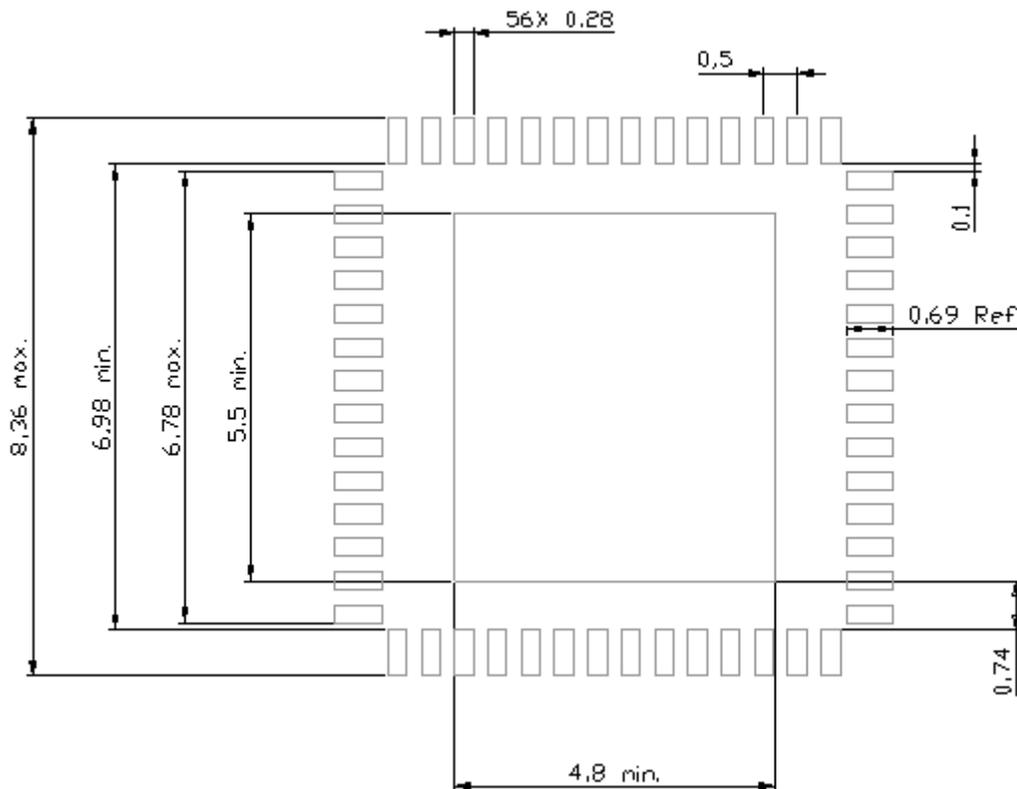
4 Board-Level Assembly

4.1 PCB Design Guidelines

One of the key efforts in implementing the QFN package is the design of the land pattern on the PCB. The 56RGQ has rectangular metal terminals exposed on the bottom peripheral surface of the package body. Electrical and mechanical connections between the component and the PCB are made by screen-printing solder paste on the PCB and reflowing the paste after placement. To ensure reliable solder joints, properly designing the land pattern to match the QFN terminal pattern is essential. IPC-SM-782 is used as the standard for the PCB land-pad designs.

There are two basic designs for PCB land pads for the QFN package: non-solder-mask-defined (NSMD) and solder-mask-defined (SMD). The industry has debated the merits of both designs of land pads and, although we recommend the NSMD pad, both styles are acceptable for use with the QFN package. NSMD pads are recommended over SMD pads because higher capability and tighter tolerances are possible in the copper-etching process than in the solder-masking process. NSMD also provides a larger copper-pad area (surface area, plus pad sidewall) without decreasing minimum pad-to-pad spacing. This allows the solder to anchor to the edges/sidewall of the copper pads, while maximizing pad-to-pad spacing and providing improved solder-joint reliability.

Figure 8 gives the critical dimensions of the 56RGQ land pattern.



Dimensions are in millimeters.

Figure 8. Recommended Land-Pad Design for the 56RGQ

4.2 Stencil Design

The difference in size between the large exposed pad and small terminal leads of the QFN package can present a challenge in producing an even solder-line thickness. Therefore, careful consideration must be given to stencil design. Stencil thickness, as well as the etched-pattern geometry, determines the volume of solder paste deposited on the PCB land. Accurate alignment of the stencil and consistent solder-volume transfer is critical for uniform results in the solder-reflow process. Usually, stencils are made of polymer or stainless steel, with stainless steel being more durable and having less deformation in the squeegee step. Apertures should be trapezoidal in cross section to ensure uniform release of the solder paste and to reduce smearing. The solder-joint thickness for QFN terminal leads should be 50 μm to 75 μm . Usually, stencils are 100- μm to 125- μm (0.004 in. to 0.005 in.) thick. If a step-down stencil design is not used, the SMT device(s) that prove to be the limiting factor on the PCB determine the actual thickness of the stencil.

A squeegee durometer of 95, or harder, should be used. The blade angle and speed must be optimized to ensure even paste transfer. Characterization of the stencil output before placing parts is recommended.

As a guide, a stencil thickness of 100 μm to 125 μm (4 mils to 5 mils) is recommended for the 56RGQ package. Figure 9 gives dimensions of the stencil recommended for the 56RGQ package. The design has an area ratio >0.66 and paste-transfer efficiency of 73% for terminal pads and 100% for thermal pads at a stencil thickness of 0.127 mm (5 mils). At a stencil thickness of 100 μm (4 mils), the area ratio is 0.86; terminal-pad paste-transfer efficiency is 89% and 100% for the thermal pad. The slotted-thermal-pad stencil design is recommended so that the package will not float during reflow and cause opens between the terminal leads and pads (see Figure 9). This feature also allows adequate room for outgassing of paste during the reflow operation, thus minimizing voids.

A low-residue, no-clean Type 3 or Type 4 solder paste is recommended.

Stencil design advice and parameters are provided courtesy of Cookson Electronics, Assembly Materials Group, at <http://www.cooksongroup.co.uk/>

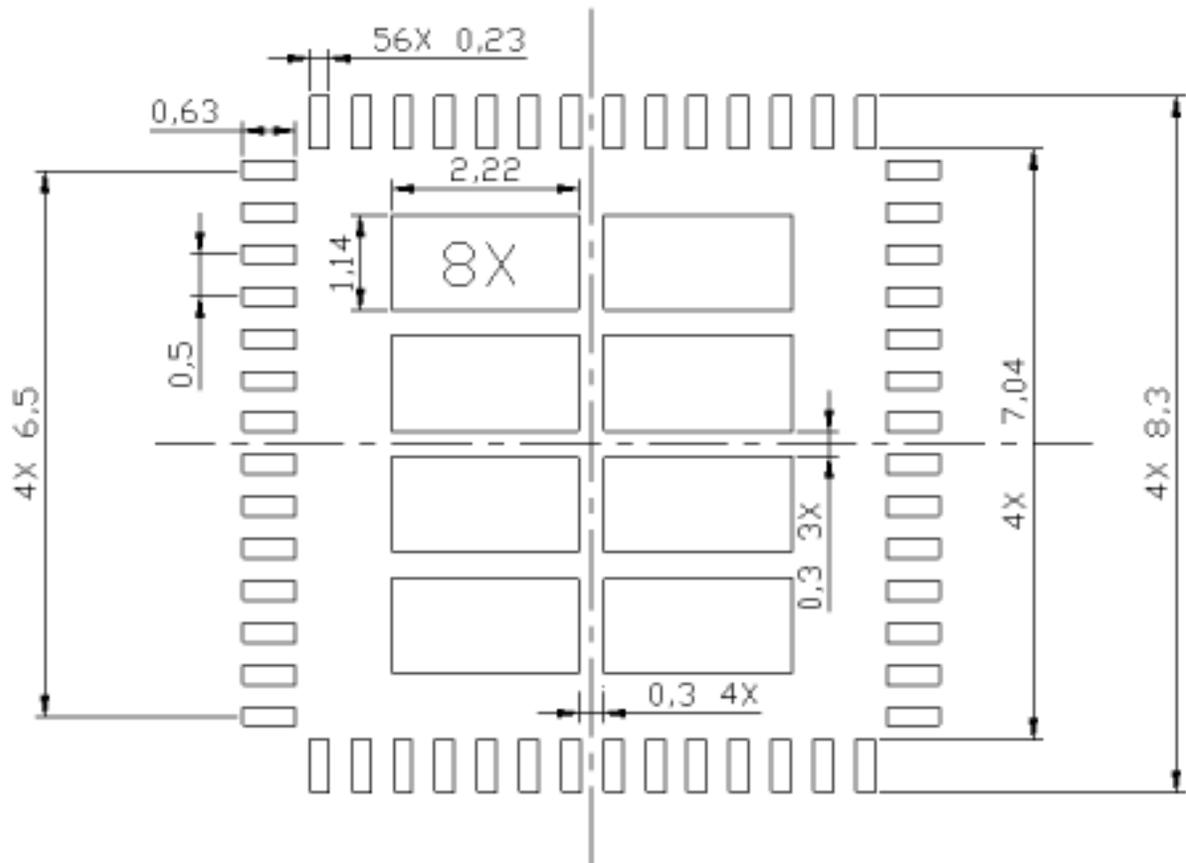


Figure 9. Recommended Stencil Design for the 56RGG

4.3 Component Placement and Reflow

The accuracy of the pick-and-place equipment governs the package placement and rotational (theta) alignment. Slightly misaligned parts (less than 50% off the terminal pad center) will automatically self-align during reflow. Grossly misaligned packages (greater than 50% off terminal pad center) should be removed prior to reflow, as they may develop electrical shorts from solder bridges.

There are two popular methods for package alignment using machine vision:

- Package silhouette. The vision system locates the package outline.
- Lead-frame recognition. Some vision systems can locate directly on the lead-frame pin-1 ID feature (chamfer in exposed pad).

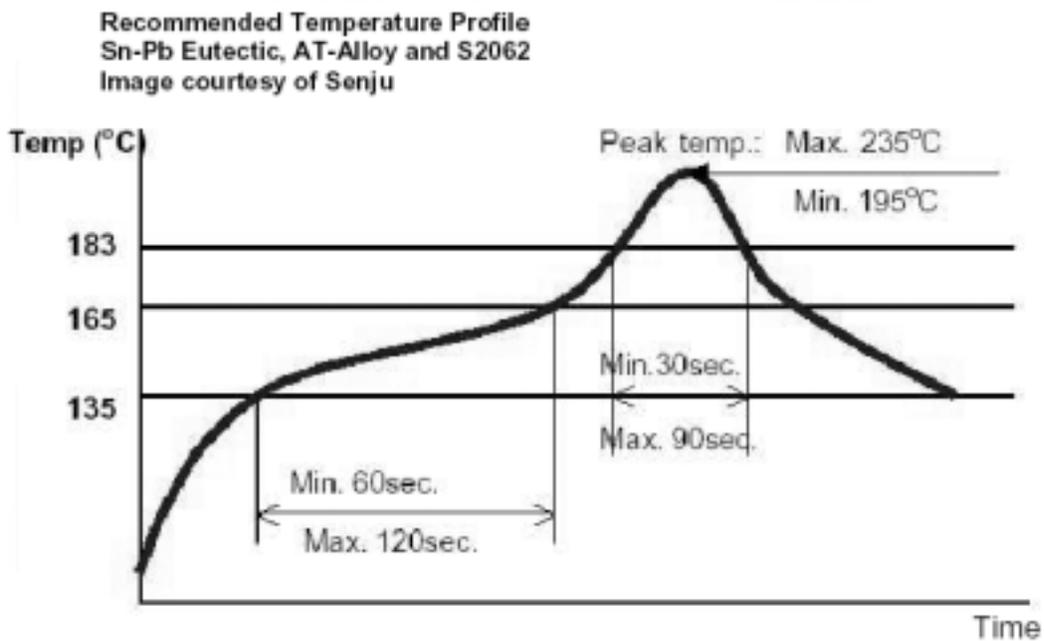
Both methods are acceptable for placement, but both have advantages and disadvantages. The pad-recognition type of alignment tends to be more accurate, but also is slower because more complex vision processing is required of the pick-and-place machine. The package-silhouette method allows the pick-and-place system to run faster, but generally it is less accurate.

Both methods are acceptable, and have been demonstrated successfully by major pick-and-place equipment vendors and contract assembly houses.

There are no special requirements when reflowing QFN packages. As with all components, it is important that reflow profiles be checked on all new board designs at different locations on the board because component temperatures may vary because of surrounding thermal sinks, location of the device on the board, and package densities.

It is recommended that the maximum reflow temperature, soak times, and ramp rates specified for a specific solder paste not be exceeded. Please consult your paste manufacturer for specifics regarding your particular paste because target temperatures and their associated times can vary widely, depending upon metallurgy and flux composition. In general, SnPb peak temperatures will be approximately 235°C.

A generic reflow profile with time/temperature targets is shown in Figure 10.



**Figure 10. Generic SnPb-Paste Reflow Profile
(Image Courtesy of Senju Metal Industry Co., Ltd.)**

4.4 Rework

QFN package rework processes are an adaptation (and, in some cases, a simplification) of ball-grid-array-package rework processes. The basic elements and sequence of this process are:

1. Board preheat (bakeout recommended)
2. Nozzle alignment
3. Reflow of component solder
4. Vacuum removal of component
5. Cleaning and preparation of PCB lands
6. Screening of solder paste
7. Placement and reflow of new component
8. Inspection of solder joints

Many automated rework systems exist that address the previous steps in a variety of ways. Two systems worth noting are manufactured by Air-Vac Engineering (<http://www.air-vac-eng.com>) and Metcal (<http://www.Metcal.com>). The rework steps can be accomplished with high precision on a single machine, under either computer or manual control. All process steps are either automatically initiated, or are prompted for operator input by the computer. Automated process-development software and hardware also is available as an option with the Air-Vac machines.

Rework systems use a conduction tool or hot gas (nitrogen or air), plus a specialized nozzle to remove and replace packages. A simplified process using these machines would be similar to the following:

1. Bakeout board per internal quality standards.
2. Load board onto machine and start rework process file on the computer.
3. Complete package-to-nozzle alignment using the stereoscope split-prism alignment system.
4. Board preheat sequence runs first. The IR thermocouple initiates the next sequence when the proper target board temperature is reached.
5. The removal tool (nozzle or conduction tool) seats on the package per the programmed process.
6. The computer runs the soak, ramp, and reflow stages of the reflow process. At the proper time above liquidus, a vacuum source within the nozzle activates, and the component is pulled off the board.
7. The pads are prepared for package replacement using another nozzle and flux.
8. Solder paste is applied, either by a miniature stencil (<http://minimicrostencil.com>) or by paste dispensing (an option on some machines). Some components can be reworked by using flux and the remaining solder from the previous package.

9. The specific package-installation program is executed on the computer. The computer prompts the operator for component insertion into the nozzle and for any fine tuning of alignment by using the stereoscope split-prism alignment system.
10. The computer controls the soak, ramp, reflow, and cool-down phases of the profile.

A variety of off-the-shelf vacuum collets, nozzles, contact heater tools, and solder screens are available from both Air-Vac and Metcal. Please reference <http://www.air-vac-eng.com> and <http://www.Metcal.com> for open tools and for custom tooling requirements.

5 Tape and Reel

5.1 Material Specifications

TI offers tape-and-reel packing for the 56RGQ package in standard packing quantities (SPQ) of 2000 units/reel. The units are shipped in embossed carrier tape, sealed with heat-activated or pressure-sensitive cover tape, and wound on plastic reels. All of the tape-and-reel materials comply with EIA-481 B and EIA-541.[5,6] The EIA specifications are shown in Table 5 and in Figures 11 and 12. The carrier tape is made of conductive polystyrene and has a surface resistivity that falls within the static-dissipative range (1×10^5 to $1 \times 10^{12} \Omega/\text{square}$). Heat-activated or pressure-sensitive antistatic, clear polyester film is used for the cover tape. The dimensions of most interest to the end user are tape width (W), cavity pitch (P), and cavity size (A_0 , B_0 , K_0) as shown in Figure 11.

The units are placed in the carrier-tape cavity, with pin 1 located as described in EIA-481B. Pin 1 is closest to the round sprocket holes as shown in Figure 13. Each reel has a minimum trailer of 300 mm and a minimum leader of one full wrap of empty carrier tape, so that no units are visible. All dimensions are in millimeters.

Table 5. Carrier-Tape Dimensions in Millimeters

Package	Carrier-Tape Width (W)	Cavity Pitch (P)	Cavity Width (A_0)	Cavity Length (B_0)	Cavity Depth (K_0)	Device Quantity Per Reel (SPQ)
56-Pin QFN	16.0 ± 0.3	12.0 ± 0.1	8.3 ± 0.1	8.3 ± 0.1	1.1 ± 0.1	2000

Package	D_0	D_1 Min	E_1	P_0	P_2	R Ref	S_1 Min	T Max	T_1 Max
56-Pin QFN	1.5 +0.1/-0.0	1.5	1.75 ± 0.1	4.0 ± 0.1	2.0 ± 0.05	30	0.6	0.6	0.1

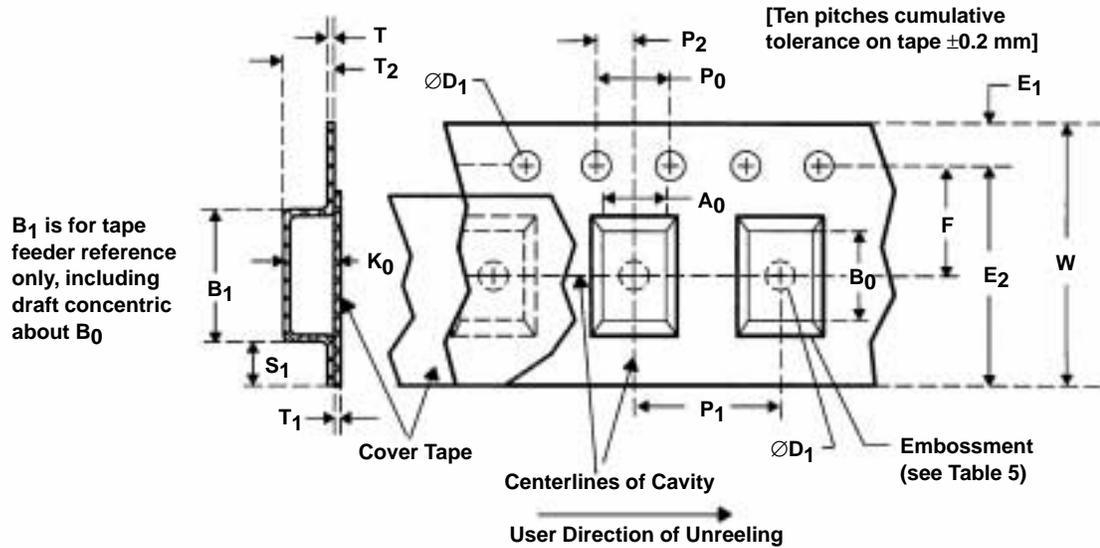
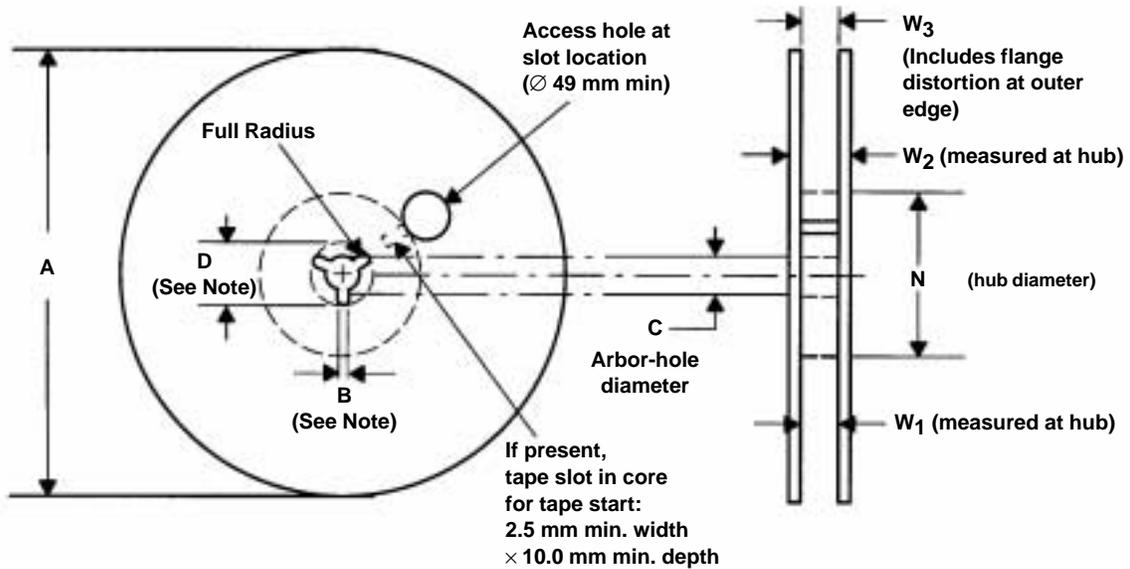


Figure 11. Carrier Tape Drawing



Reel Diameter (A)	Reel Width (W1)	Hub Diameter Max (N)	Reel Thickness (W2)	Arbor-Hole Diameter (C)
330 ± 0.60	12.4 + 2.0/-0.0	60 ± 0.50	13.65 ± 1.95	13.0 + 0.5/-0.2

NOTE: Drive spokes are optional; if used, dimensions B and D shall apply.

Figure 12. Reel Drawing and Specifications

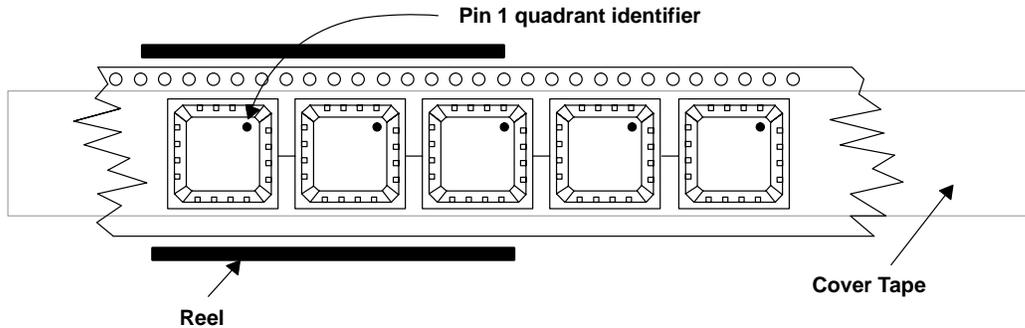


Figure 13. Pin-1 Orientation of QFN Packages

5.2 Shipping Labels

All reels have an electrostatic discharge (ESD) caution symbol (embossed or paper) on the hub, and a barcode label placed on the same side of the reel and on the side opposite the carrier-tape round sprocket holes.

The intermediate container or shipping box also must have a 2D barcode label and an ESD label.

5.3 Dry-Pack Requirements for Moisture-Sensitive Material

Moisture-sensitive material, as classified by JEDEC standard J-STD-033, must be dry packed. The 56RGQ package is MSL3/235°C, and is dried before sealing in the moisture-barrier bag (MBB) with desiccant and a humidity indicator card (HIC). The MBB has a moisture-sensitivity caution label (as defined by J-STD-020) to indicate the moisture-sensitive classification of the enclosed devices, as well as the 2D barcode shipping label. The intermediate box also has a moisture-sensitive identification label.

The calculated shelf life for dry-packed components shall be a minimum of 12 months from the MBB seal date, when stored in a noncondensing atmospheric environment of $40^{\circ}\text{C}/90\% \text{RH}$. Once opened, the 56RGQ package has a floor life of 168 hours at $30^{\circ}\text{C}/60\% \text{RH}$ before bakeout is required.

6 Symbolization

The top of the 56RGQ package is laser marked with device name, corporate ID, date code, assembly/test site code, assembly-lot trace code, and pin-1 location. Table 6 shows the symbolization guidelines for 56-pin QFN packages.

Table 6. Device-Marking Guidelines

QFN Symbolization Guidelines					
Pins	Package/ Designator	Namerule and Format	Maximum Characters Per Row	Maximum Rows	Symbol Format
56	QFN (RGQ)	C2	7	3	<ul style="list-style-type: none"> • SS859 TI YMS LLLL

The symbol-format column in Table 6 has the following definitions:

- SS859 = Short device name for SN74SSTV16859RGQR
- TI = Texas Instruments
- Y = Year
- M = Month
- S = Site code
- LLLL = Lot trace code
- = Pin-1 quadrant identifier (data sheet specifies exact pin-1 location)

For specific marking on any particular device, please see the device data sheet at www.ti.com.

7 Test Sockets

Test sockets for the 56-pin QFN devices can be obtained from:

Plastronics
 2601 Texas Drive
 Irving, Texas 75062
 Phone: 972-258-2580
 Fax: 972-258-6771

Socket Part Number:
 56 Pin: 56QN50T18080

8 Features and Benefits

In summary, key features and corresponding advantages for logic products in the QFN package are:

- Significant area savings over comparable TSSOP, TVSOP, and TQFP packages. The 56RGQ is 11% to 55% smaller than its equivalent-pin counterpart. Similarly, board routing area is reduced.
- Leadless package eliminates bent-lead issues.
- Exceptional board-level reliability under temperature cycle, vibration, and drop testing
- Superior thermal characteristics, especially when used in conjunction with thermal vias
- Superior package parasitics, when compared to TSSOP, SSOP, TVSOP, and TQFP packages. The unique construction of QFN packages reduces both inductance and capacitance. For device specifications, please refer to the applicable device data sheet at <http://www.ti.com/>

9 Conclusion

The TI 56RGQ 56-pin QFN package is a leadframe-based leadless package, with improved thermal performance, electrical performance, and package volume over similar TSSOP, TVSOP, and TQFP packages. Additionally, the 56RGQ package has reliable solderability using SnPb eutectic solder pastes, and can be reworked and manufactured using conventional equipment. The package allows for product miniaturization and is registered under JEDEC standard MO-220.

10 Acknowledgments

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11 References

References 1 through 4 are available at: <http://www.jedec.org/download/default.cfm>

1. JEDEC Standard MO-220, *Thermally Enhanced Plastic Very Thin Quad Flat No Lead Package (HP-VFQFP-N)*
2. JESD 51-5, *Extension of Thermal Test Board Standards for Packages with Direct Thermal Attachment Mechanisms*
3. JESD 51-7, *High Effective Thermal conductivity Test Board for Leaded Surface Mount Packages*
4. JESD 51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
5. EIA-481 B, *Taping of Surface Mount Components for Automatic Placement*
6. EIA-541, *Packing Material Standards for ESD Sensitive Items*
7. IPC-SM-782, *Surface Mount Design and Land Pad Standard*

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