

Quick Start Guide SLDU018–May 2015

PGA900EVM Quick Start Guide

The following quick start guide will help the user to quickly test the front end (GAIN + ADC) and the back end (DAC + GAIN) of the PGA900. It will also show the different memories and software related tools available in the PGA900. Before proceeding, make sure the PGA900EVM is configured in its default configuration and properly connected to the USB2ANY as shown in Figure 1.

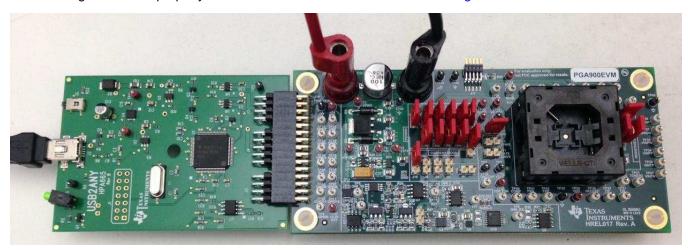


Figure 1. PGA900EVM Default Configuration

All trademarks are the property of their respective owners.

1 Enabling Communication

- 1. Bring up the PGA900 GUI.
- 2. The default configuration for PGA900EVM is for voltage mode application. Therefore, configure the PGA900EVM by clicking on the "Interface Settings" tab and setting both the "RLOOP" and the "Additional Voltage" to 0.

PGA900	
File Script Debug Help	
Digital Interface SPI I2C OWI OWI Activation Mode Through Pulse 💌 🛛 USB2ANY Disconnected	
Selection	
section Implementation Sections Implementation Sections 1 O Gan & ADC AC & PWM Settings O ADC & Server DIGITAL INTERFACE CONFIGURATION Izc CONFIGURATION Izc CONFIGURATION O MUX Low Level Configuration Diversion Speed CS Value IoNAL Even Configuration OWI CONFIGURATION OWI CONFIGURATION OWI CONFIGURATION OWI CONFIGURATION OWI Configuration Ricop Configuration Ricop Configuration Ricop O ohm Configure POT 2 Additional Voltage Out V Configure POT 3	
idie 3.1.0.0 HW CONNECTED 🖑 TEXAS INST	RUMENTS
	and a second sec

Figure 2. Configuring the Hardware for Voltage Mode



www.ti.com

 The microcontroller is running at power-up. Set the microcontroller in reset by clicking on the "Microcontoller" button as shown in Figure 3. The button will change to "Digital Interface" to indicate the different digital interfaces are enabled for communication with the device.

Microcontroller SPI	I2C OWI OWI Ac	tivation Mode	Thro	ugh Pulse 🖉	- USE	32ANY Disc	onnecte	d			
Selection A	` 🔽 🖅 🖉 🖉 🔽							υ	pdate Mode I	mmediate	
- 🔷 Interface Settings	Register Map						Fiel	d View			
	Register Name	Address	DevAddr	BaseAddr	Default	Value 🖌	-1.22	u mon			
-	CSR	riddrood	Derriddi	Dabertaal	Deldan	Talat					
ADC & PWM Settings	RAMBIST CONTROL	0x02	0x02	0x40000500	0x00	0x00					
♦ EEPROM, DEVRAM & OTP	RAMBIST STATUS	0x03	0x02	0x40000500	0x00	0x00 ≡					
	CLK_CTRL_STATUS	0x04	0x02	0x40000500	0x00	0x00					
Low Level Configuration	DIG IF CTRL	0x06	0x02	0x40000500	0x47	0x47					
	OWI_ERROR_STATUS_LO	0x08	0x02	0x40000500	0x00	0x00					
	OWI_ERROR_STATUS_HI	0x09	0x02	0x40000500	0x00	0x00					
	OWI INTERRUPT	0x0A	0x02	0x40000500	0x00	0x00	-				
	OWI_INTERRUPT_ENABLE	0x0B	0x02	0x40000500	0x00	0x00					
	OTP PROG DATA1	0x10	0x02	0x40000500	0x00	0x00					
	OTP PROG DATA2	0x11	0x02	0x40000500	0x00	0x00					
	OTP PROG DATA3	0x12	0x02	0x40000500	0x00	0x00					
	OTP PROG DATA4	0x13	0x02	0x40000500	0x00	0x00					
	OTP_PROG_ADDR1	0x14	0x02	0x40000500	0x00	0x00					
	OTP_PROG_ADDR2	0x15	0x02	0x40000500	0x00	0x00	-				
	OTP_PROG_CTRL_STAT	0x16	0x02	0x40000500	0x00	0x00	-		12		
	OTP_PAGE_ADDR	0x18	0x02	0x40000500	0x00	0x00					
	DATARAM_PAGE_ADDR	0x19	0x02	0x40000500	0x00	0x00					
	DEVRAM_PAGE_ADDR	0x1A	0x02	0x40000500	0x00	0x00					
	WDOG_CTRL_STAT	0x1C	0x02	0x40000500	0x00	0x00	-				
	WDOG_TRIG	0x1D	0x02	0x40000500	0x01	0x01					
	PIN_MUX	0x1E	0x02	0x40000500	0x00	0x00					
	PADC_DATA1	0x20	0x02	0x40000500	0x00	0x00	-				
		0v01	0,000	0~10000500	0,000	nvnn	- I				
	() III					1					
	Register Description										
											į.
				2.2							_

Figure 3. Setting the Microcontroller to Reset



2 Setting Up PGAIN and Reading PADC Data

Once the digital interfaces are enabled, the device must first be taken out of shutdown mode so that the PGAIN and PADC can be used.

- 1. Click on the "Gain & ADC" tab.
- 2. Enable the VREF buffer, disable the analog shutdown and enable the ADCs as shown in Figure 4

PGA900	
File Script Debug Help	
Digital Interface SPI	I2C OWI OWI Activation Mode Through Pulse 💌 🗇 USB2ANY Disconnected
Selection A High Level Configuration	Enable VREF Buffer Analog Power ADC_CFG_1
Angli Level configuration	Disabled ShutDown Mode ADC_EN
Bridge Ctrl & Status	
ADC Capture	P. SENSOR & P. ADC 2 3 4 T. SENSOR & T. ADC
OAC & PWM Settings	TEMP_SENSOR
EEPROM, DEVRAM & OTP	P_GAIN PGAIN_OPEN TEMP_MUX_CTRL TSEM_N 5 ▼ Disabled VINTP-VINTN ▼ SINGLE ENDED
♦ Low Level Configuration	INT T SENSOR EXT T SENSOR
	IESI_MUX_P_EN T_GAIN ITEMP_CTRL IESI_MUX_I_EN
	Disabled 1.33 OFF Disabled
	P. ADC T. ADC
	PADC_EN PADC_EN_24BIT PADC_DECL_RATE TADC_EN TADC_EN_24BIT TADC_DECL_RATE Disabled 16 Bit Output 64 us Disabled 16 Bit Output 64 us
	Disquied 10 Dit Output 04 US
	P.ADC Data T.ADC Data
	Reg1 (MSB) Reg2 (MID) Reg3 (LSB) Voltage (V) Reg1 (MSB) Reg2 (MID) Reg3 (LSB) Voltage (V) Temp (deg)
	READ ADC Clear READ ADC Clear
	TRACE_FIFO_ENABLE None TRACE FIFO Dump Folder Path 0 %
	None TRACE FIFO Dump Folder Path 0 76
	READ FIFO PGA900/FIFO DUMP
-	
Idle	3.1.0.0 HW CONNECTED 🖑 TEXAS INSTRUMENTS

Figure 4. Enabling the Analog Power in PGA900



www.ti.com

3. Click on the "Bridge Ctrl & Status" tab and enable the bridge voltage as shown in Figure 5. The resistive bridge in the PGA900EVM is now being excited by the 2.5 V coming from the PGA900. The bridge in the PGA900EVM has only variable leg (top left). It consists of a 4.7-kΩ resistor in series with a dual digital potentiometer, where the potentiometers are in a parallel configuration. The user has the ability to change one or both or both potentiometers with the Potentiometer Mode menu. For demo purposes, to obtain a 10-mV differential input voltage use Table 1.

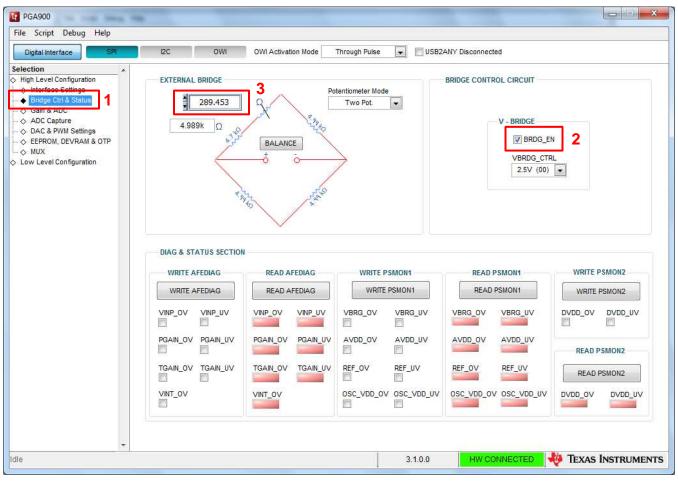


Figure 5. Enabling Bridge Voltage in PGA900 and Configuring Resistive Bridge in PGA900EVM

Table 1. Potentiometer Mode

Approximate differential voltage (mV)	One pot (Ω)	Two pot (Ω)
10	209.7	209.4
15	171.1	170.3
25	92.5	92.2

In the potentiometer box, type the desired resistance from the table above and then click outside the box. You can measure these input voltages by connecting a multimeter between TP34 (VINPP) and TP35 (VINPN) in the PGA900EVM.



Setting Up PGAIN and Reading PADC Data

www.ti.com

4. Click on the "Gain & ADC" tab. Select a gain for the PGAIN and enable the multiplexers to connect the PGAIN to the PADC as shown in Figure 6. The number of bits and decimation rates can also be chosen. Then click on "Read ADC". For this particular example a gain of 10 V/V was selected for PGAIN and the differential input voltage was set to approximately 10 mV in the previous step. As a result, the ADC input voltage is close to 100 mV.

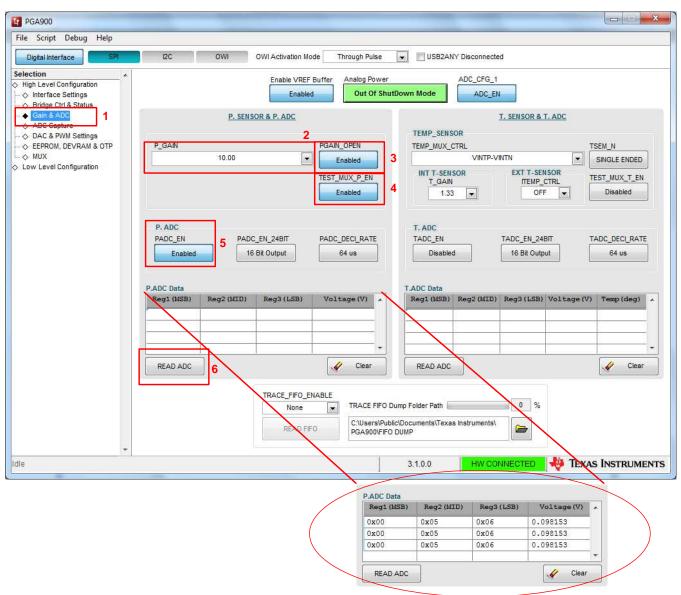


Figure 6. Configuring the PADC



www.ti.com

3 DAC Output Reading

The PGA900GUI can also be used to write directly to the DAC and measure the analog output.

- **NOTE:** For the DAC to output the data from the ADC (either pressure or temperature), the M0 needs to be running the proper software. A reference firmware for the M0 can be found at the product folder for the PGA900.
- 1. Connect a multimeter between TP1 (VOUT after feedback) and TP39 (ASIC_GND).
- 2. The microcontroller has to be in reset. Click on the "DAC & PWM Settings" tab.
- 3. Enable the DAC and the test mux for the DAC.
- 4. Select the DAC configuration, absolute or ratiometric. Ratiometric is proportional to VDD, therefore for demo purposes, absolute should be chosen.
- 5. Select the gain from the DAC buffer . The gain is respect to VREF=1.25 V. Therefore, a gain of 4 V/V would imply a maximum output voltage of 5 V.
- 6. Write to the DAC in hex format. Mid-code is 0x1FFF, full code is 0x3FFF written to the DAC_REG0 register. With the gain set to 4 V/V, mid-code and full code should create a 2.5 and 5V DAC outputs respectively. Please notice that if a 10 V/V gain is selected, the input voltage to the EVM has to be greater than 12.5 V.

 Charling Satissies Bridge Charlos Satissies Bridge Charlos Satissies Configuration Carlo Configuration	1 PGA900		
Selection With Level Configuration O Right Chi Status O Gain A COL O CoC Cepture O Cepture CoopBack Contput CoopBack Ins to be enabled to read LoopBack Output CoopBack Ins to be enabled to read LoopBack Output CoopBack Ins to be enabled to read LoopBack Output CoopBack Ins to be enabled to read LoopBack Output Cepture Cepture O Cepture O Ce	File Script Debug Help		
O High Level Configuration O High Level Configuration O Loc Registers O Loc Configuration O Loc Configuration O Loc Registers O Loc Configuration O Loc LoopBack Ctri D Loc LoopBack Ctri D Loc LoopBack Cutput D Loc LoopBack Cutput LoopBack has to be enabled to read LoopBack Cutput Correct LoopBack LoopBack Cutput Correct LoopBack LoopBack Cutput <td>Digital Interface SPI I2C OWI</td> <td>OWI Activation Mode Through Pulse 💌</td> <td>USB2ANY Disconnected</td>	Digital Interface SPI I2C OWI	OWI Activation Mode Through Pulse 💌	USB2ANY Disconnected
PADC LoopBack Output Reg1 (MSB) Reg2 (MID) Reg3 (LSB) Voltage (V) Image: I	 ♦ High Level Configuration ♦ Interface Settings ♦ Bridge Ctrl & Status ♦ Gain & ADC ♦ DAC Copruse ♦ DAC & PWM Settings 1 ♦ EEPROM, DevrAnt & DTP ♦ MUX ♦ Low Level Configuration 	_MUX_DAC_EN DAC Config Enabled 1.25V (Absolute) ▼ m DAC Registers n DAC REG0 × 3FFF V DAC REG1 × 0000	PWM_EN PWM_Disabled PWM_ON_TIME PWM_OFF_TIME x 0 Read
LoopBack has to be enabled to read LoopBack Output	PADC LoopBack Output		
Idie 3.1.0.0 HW CONNECTED 🙌 TEXAS INSTRUMENTS	LoopBack has to be enab		
	Idle	3.1.0	.0.0 HW CONNECTED 4 TEXAS INSTRUMENTS

Figure 7. Writing Directly to the DAC in the PGA900



Memory

4 Memory

The PGA900 offers different memory options depending on the customer need. The 128 bytes in the EEPROM can be read as shown in Figure 8. Additionally, DEVRAM provides the option to run code in the microprocessor without using OTP. The .hex files can be downloaded into DEVRAM and once the REMAP bit is enabled, the code overlaps the OTP memory location so that the microcontroller can execute it. Once the device is powered down, the DEVRAM content is erased. OTP is a one-time memory programming option. In order to program the OTP, 7.5 V are needed to be applied to the VP_OTP pin in the PGA900. This can be done by closing J15 in the PGA900EVM.

PGA900				
File Script Debug Help				
Digital Interface SPI	I2C OWI OWI Activation Mod	de Through Pulse 💽 🔲 USB2ANY Disconnecte	d	
Selection			OTP PROGRAMMING	
High Level Configuration				
	EEPROM CA	CHE READ	Hex File Path	
→ ♦ Gain & ADC			👝 🗌	
→ ADC Capture	Go' REA	D CACHE		
DAC & PWN Cettings			LOAD VERIFY	
EEPROM, DEVRAM & OTP	FF FF FF FF FF	F FF FF FF	OTP Memory OTP	
- O MUX	FF FF FF FF		Verify OTP will compare the data in the hex file	
Low Level Configuration			path with OTP registers and confirm the match	
	Read Cache Status	0 %	In the indicator	
		0 70	OTP Status	
			Verify OTP feedback file will be created parallel	
			to the selected hex file.	
	EEPROM WRITE	EEPROM READ	2 DEV RAM PROGRAMMING	
	Calculate CRC	Grof READ	Hex File Path	
		Contraction of the second s		
		Unselected page data will be displayed as 0 on reading		
	Select Right Click to Load EEPROM Data from File	Select 2ght click to write EEPROM Data to File		
	0000: FF FF FF FF FF FF FF FF	⊘ 0000: 55 55 55 55 55 55 55 55		
	0001: FF FF FF FF FF FF FF FF	▼0001: AA AA AA AA AA AA AA AA AA ▼0002: 55 55 55 55 55 55 55 55	LOAD Dev RAM REMAP Disabled	
	0003: FF FF FF FF FF FF FF FF	V 0003: AA AA AA AA AA AA AA AA		
	0004: FF	✓ 0004: 55 55 55 55 55 55 55 55 ✓ 0005: AA AA AA AA AA AA AA AA	Load Status	
	0006: FF FF FF FF FF FF FF FF	✓ 0006: 55 55 55 55 55 55 55 55		
	0007: FF FF FF FF FF FF FF FF FF 0008: FF FF FF FF FF FF FF FF FF	✓ 0007: AA AA AA AA AA AA AA AA ✓ 0008: 55 55 55 55 55 55 55 55	Directory Path - Dump Dev Ram Data	
	0009: FF FF FF FF FF FF FF FF	🔽 0009: AA AA AA AA AA AA AA AA	C:\Users\Public\Documents\Texas	
	000A: FF FF FF FF FF FF FF FF FF 000B: FF FF FF FF FF FF FF FF FF	▼ 000A: 55 55 55 55 55 55 55 55 ▼ 000B: AA AA AA AA AA AA AA AA	Instruments\PGA900\Dev RAM	
	000C: FF FF FF FF FF FF FF FF	₹000C: 55 55 55 55 55 55 55 55 55		
	000D: FF	✓ 000D: AA AA AA AA AA AA AA AA ✓ 000E: 55 55 55 55 55 55 55 55	Read Dev RAM	
	000F: FF FF FF FF FF FF FF FF	1000F: AA AA AA AA AA AA AA AA		
	EEPROM Write Status	EEPROM Read Status	Read Status	
	0 %	100 %	0 %	
.				
Idle 3.1.0. HW CONNECTED 👋 TEXAS INSTRUMENTS				
			Y LEAD A REALING	

Figure 8. PGA900 Memory Options

5 Resources

For more information, see the following.

- PGA900 product page
- PGA900EVM product page

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have *not* been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		Applications	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	TI E2E Community	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconne	ctivity	

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2015, Texas Instruments Incorporated