

THS8200 PCB Layout Guidelines

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- The choice of single GND plane or split DGND/AGND plane will depend on board content and parts placement. If a single GND plane is used, keep digital components and return currents away from the analog section. If separate planes are used, keep analog power, decoupling, and traces over the AGND plane and digital traces over the DGND plane.
- Provide adequate power supply filtering, especially the 3.3V AVDD and 1.8V VDD_DLL supplies. Linear regulators are preferred but not a requirement if switching regulators are adequately filtered and properly placed on the PCB.
- Place 0.1 μ F power decoupling capacitors close to each power pin.
- Place the FSADJ resistor and the COMP and VREF capacitors as close as possible to their pins.
- Keep traces as short and delay matched as possible to maximize signal integrity and timing margin. Trace length tolerances will depend on operating frequencies and system setup/hold time margins.
- Series termination resistors are recommended on all digital traces to maximize signal integrity and electro magnetic compliance (EMC). These termination resistors should be placed as close as possible to the digital source. Values required will depend on PCB trace impedance and source impedance of the bus drivers.
- All analog input traces should have a minimum of 10x (x means trace width) clearance between each other and other adjacent traces to minimize any potential crosstalk.
- Place the THS8200 as close as possible to the video/graphics output connector and maintain matched trace lengths. 75-ohm trace impedance is preferred for the analog output traces.
- All high speed signals should be routed over a solid GND/Power plane and not routed over power/GND splits. Route signals over associated power plane where possible.
- Minimize vias in the high speed data and clock traces. Clock and bus daisy-chaining should be avoided for best signal integrity.
- Using GND fills on the top and bottom of the board will improve isolation between signals and also help maximize EMC.
- Avoid routing traces under the thermal pad. Solder the thermal pad to a thermal land on the PCB and via to the internal GND plane. When split GND planes are used, the thermal pad should be connected to the digital GND.
- ESD protection on the analog outputs is recommended.
- Output filtering requirements depend on whether video or graphics formats are being supported. A ferrite bead may be used in the analog output path for high frequency noise reduction, but excessive filtering of RGB graphics outputs should be avoided.
- See Figure 1 below for recommended GND split when split planes are used.

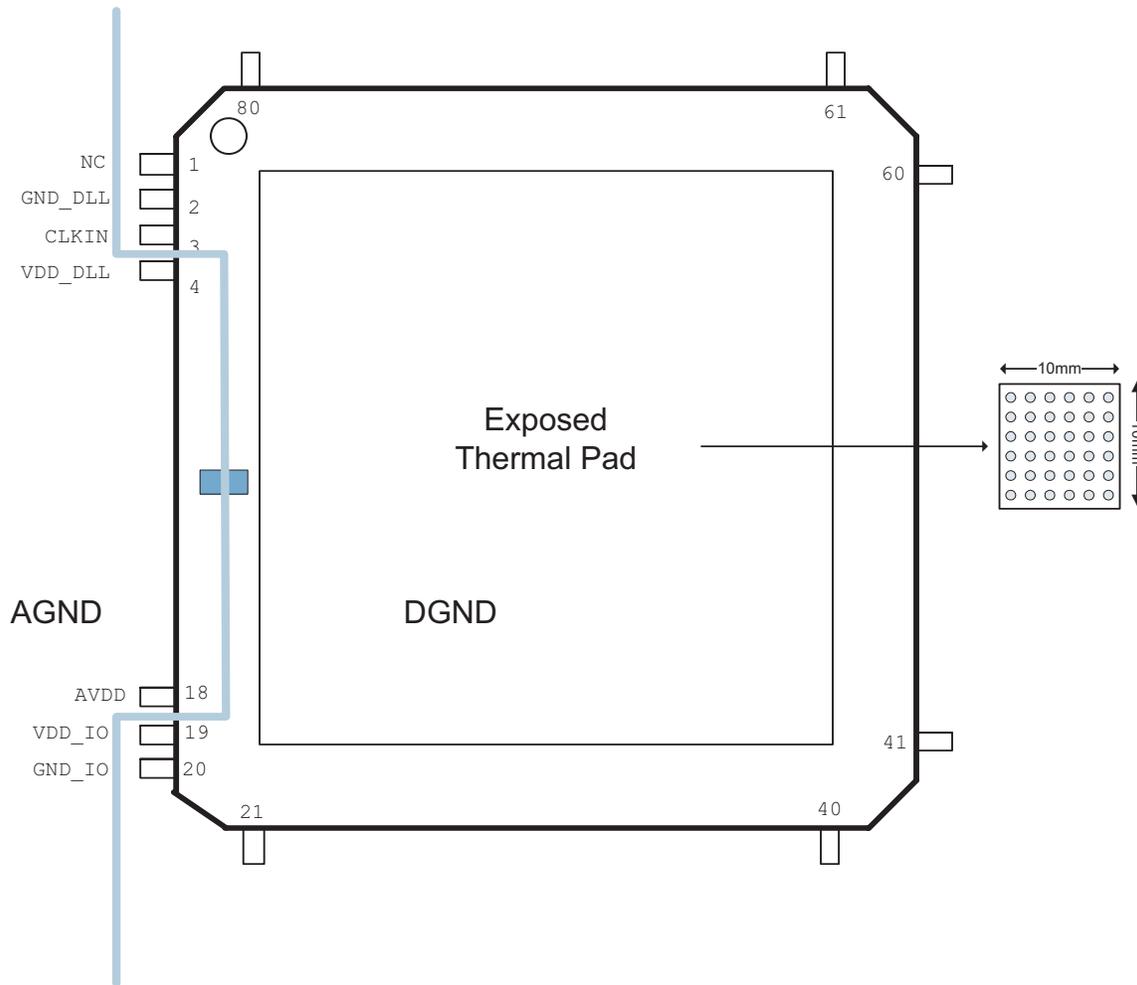


Figure 1. Recommended Split Between GND Planes

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