

## **TSB12LV01B/TSB41AB3 Reference Schematic**

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### **ABSTRACT**

This application report describes the electrical connections between the Texas Instruments TSB12LV01B and TSB41AB3 for common modes of operation. Use this document in conjunction with the TI application report, *Recommendations for PHY Layout* (SLLA020), to successfully design a 1394 system.

The TSB12LV01B is a high-performance, general-purpose IEEE 1394-1995 link-layer controller (LLC) with the capability of transferring data between a host controller and the 1394 PHY-link interface. For more information, refer to Texas Instruments Data Manual, *TSB12LV01B, IEEE1394-1995 High-Speed Serial-Bus Link-Layer Controller* (SLLS435).

The TSB41AB3 is a three-port 400-Mbps physical layer (PHY) device that fully supports provisions of the IEEE 1394-1995 standard and P1394a supplement (version 5.0). The TSB41AB3 can also operate at 100-Mbps and 200-Mbps. For more information, refer to Texas Instruments Data Manual, *TSB41AB3, IEEE1394a Three Port Cable Transceiver/Arbiter* (SLLS418).

### **NOTE**

The reference schematic does not represent an actual test board  
constructed by Texas Instruments, Inc.

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## 1 Cable Interface

The cable interface is shown on page 1 of the TSB12LV01B/TSB41AB3 schematic (Appendix B). It includes two 1394 ports that connect to the PHY. A third 1394 port is not implemented in order to show correct termination of an unused port.

### NOTE

If three or more 1394 ports are implemented, a 1.5-A current-limited fuse must be connected between each port and the bus power.

The cable power from each cable (pin #1, PWR, on the 6-pin 1394 connector) is connected to the other ports and is available as bus power. The PHY operates off of bus power. A voltage regulator regulates the bus power to 3.3 V. To be 1394 compliant, the regulator must maintain 3.3 V when the input voltage ranges between 8 Vdc and 33 Vdc. The voltage regulator is shown on page 1 of the TSB12LV01B/TSB41AB3 schematic (Appendix B). When cable power is not active, the PHY may also be powered from a 12-V source, such as a PC power supply. A diode determines which power source is used. For protection, a 0.75-A fuse must also be used in-line with the 12-V source.

The cable shield from each cable (pins #7 and #8 on the 6-pin 1394 connector) is connected to chassis ground through an RC network. The RC network is designed to prevent current from flowing on the cable shield in case of potential differences between chassis grounds. A combination of a 1-M $\Omega$  resistor, 0.001- $\mu$ F capacitor, and 0.01- $\mu$ F capacitor placed next to each 1394 connector is suggested. This helps prevent the cable shield noise on one port from coupling onto the other port.

The cable ground (pin #2 on the 6-pin 1394 connector) is tied directly to PHY ground. According to the IEEE 1394-1995 standard, all PHYs in a network must be at the same ground potential for common mode signaling to work properly.

The drivers on each port (TPA and TPB) are designed to work with an external 112- $\Omega$  termination-resistor network, which matches the 110- $\Omega$  cable impedance. One network is provided at each end of the twisted-pair cable. The midpoint of the TPA resistor network is directly connected to TPBIAS. The midpoint of the TPB resistor network is coupled to ground through a parallel RC network. These termination resistor networks must be placed as close as possible to the PHY.

The TPBIAS lines indicate the presence of an active connection to other nodes on the bus. A 1- $\mu$ F capacitor external filter must stabilize the TPBIAS lines. A 1- $\mu$ F capacitor-to-ground filter must be connected to the TPBIAS line of any unused ports as well.

## 2 Physical Layer Device-TSB41AB3 (400-Mbps, 3-Port PHY)

The electrical connection for the physical layer device is shown on page 2 of the TSB12LV01B/TSB41AB3 schematic (Appendix B).

All power pins on the TSB41AB3 PHY must be tied together, then decoupled to the associated power pins and ground pins through a series of high-frequency decoupling capacitors. The following rules apply to the decoupling capacitors:

- Place one 0.1- $\mu$ F capacitor as close as possible to each single power pin on the PHY. A single power pin is one that is not adjacent to another power pin. For example, pin #73 (PLLVD) is a single power pin.
- Place one 0.001- $\mu$ F capacitor as close as possible to each power pin. If two or more power pins are adjacent, only one 0.001- $\mu$ F capacitor is required for the group. For example, pin #47 and #48 must be connected only to a single 0.001- $\mu$ F capacitor because they constitute a power pin group.

#### NOTE

Refer to Figure 9 in the TSB41AB3 data manual, *IEEE 1394a Three Port Cable Transceiver/Arbiter (SLLS418)*, for detailed information on capacitor placement.

The TSB41AB3 has 5-V tolerant inputs. When interfacing to a 5-V device, these input pins must be tied to a 5-V source; otherwise they must be connected to the 3.3-V supply voltage of the PHY. The 3.3-V implementation is shown in the schematic (Appendix B).

The  $\overline{ISO}$  pin is used to control the output differentiation logic of the CTL and D lines on the link layer interface for the IEEE 1394-1995 Annex J method of isolation. If the Annex J method of isolation is used, the  $\overline{ISO}$  pin must be tied low. If either the Texas Instruments bus-holder method of isolation or no isolation is used, this terminal must be tied high (to PHY power through a 10-k $\Omega$  pull-up resistor). No isolation is implemented in the schematic.

The CPS pin detects the presence of cable power and is connected to the cable power through a 400-k $\Omega$  resistor. A common resistor value of 390-k $\Omega$  may be used. For a six-pin 1394 connector, the node must always have the CPS pin connected to cable power through a 400-k $\Omega$  resistor, even if the PHY does not use cable power. The only instance in which the CPS pin may not be connected to cable power is the case of a 4-pin 1394 connector or 6-pin connector with power class 000. In that case, the CPS may be tied directly to PHY ground, indicating that cable power is not available.

#### NOTE

For a 200-Mbps PHY, the CPSInt internal interrupt is continuously set after it is cleared, if the CPS pin is tied low. The software must ignore this interrupt. If the software cannot ignore this interrupt, the CPS pin may be directly tied to  $V_{DD}$ , but the PHY reports the wrong cable power status to the node.

When a 1394 port is not brought out to a connector, it must be terminated correctly. To terminate a non-implemented port, the TPB+ and TPB- pins must be tied together and connected to ground. The TPBIAS must be tied to ground through a 1- $\mu$ F capacitor. The TPA+ and TPA- lines can be left unconnected. Port 1 in the schematic illustrates a properly terminated port.

The FILTER0 and FILTER1 function as a filter for the internal phase-locked loop (PLL). A 0.1- $\mu$ F (10% or better) capacitor is the only external component needed to complete this filter.

The SE and SM pins are test-input pins used in the manufacturing testing of TSB41AB3. For normal use, these pins must be tied to ground separately through a 10-k $\Omega$  resistor.

To ensure proper operation, the  $\overline{RESET}$  pin must be asserted low for a minimum of 2 ms from the time PHY power reaches the minimum required supply voltage. When using a passive capacitor on the  $\overline{RESET}$  pin to generate a power-on reset signal, the minimum reset time is met if the capacitor has a minimum value of 0.1- $\mu$ F and satisfies the following equation:

$$C_{min} = (0.0077 \times T) + 0.085 \mu F$$

Where:

$C_{min}$  is the minimum capacitance on the  $\overline{RESET}$  pin in  $\mu$ F

T is the  $V_{DD}$  ramp time from 10%-90% in ms.

The R0 and R1 terminals set the internal operating currents and the cable driver output current. To meet the IEEE 1394-1995 standard output voltage limits, a 6.3-k $\Omega \pm 0.5\%$  resistance is required. To achieve this, a 6.34-k $\Omega \pm 0.5\%$  and 1-M $\Omega \pm 10\%$  resistor are placed in parallel.

The XO and XI terminals are the crystal oscillator inputs. These terminals connect to a 24.576-MHz parallel resonant fundamental mode crystal. There is a strict total tolerance of 100 pulse-position modulation (ppm) on the 24.576-MHz crystal. This tolerance must be met to comply with the overall requirement of 100 ppm per the IEEE 1394-1995 standard. For every crystal, loading requirements depend on the board technology and distance from the PHY.

**Crystal Selection:** To ensure that the PHY crystal starts under all operational conditions, a fundamental parallel mode crystal with a  $C_L$  of 15 pF or less is recommended. The termination capacitor values that must be placed on each leg of the crystal can be calculated with the following equation:

$$C_{termination} = (C_L - C_{board}) \times 2$$

Where:

$C_{board}$  = (Board trace capacitance + PHY input capacitance)

If the crystal is placed close to the PHY, then  $C_{board} \cong 4$  pF and  $C_{termination} \cong 22$  pF.

TESTM is the test control input used during the manufacturing of the TSB41AB3 PHY. It must be tied to  $V_{DD}$ .

The power class pins (PC0-PC2) program the power class value into the PWR field of the transmitted self-ID packet. This allows other nodes on the bus to understand the power requirements of the node. These pins are programmed according to the Power Class Description in the IEEE 1394a standard, Table 7-3. The schematic is programmed to a power class of "100" or decimal 4. This indicates that the node:

- a) May be powered from the bus
- b) Is capable of repeating power
- c) Is using up to 3 W
- d) Needs no additional power to enable the link

The power class pins are hard-wired to their values shown on the schematic.

### 3 PHY-Link Interface

The PHY-link interface electrical connection is shown on Sheet 2 of the TSB12LV01B/TSB41AB3 schematic (Appendix B). The PHY-link interface follows the IEEE 1394-1995 and 1394a standards. No isolation is implemented in this schematic. The PHY and link operate off of the same ground plane.

To reduce EMI emissions and reduce reflections on the SYSCLK line, a series-damping resistor is recommended. The schematic shows a 0- $\Omega$  resistor, which is essentially a placeholder on the board. To reduce EMI, a 22- $\Omega$  resistor on the SYSCLK line is recommended. This resistor must be placed as close to the PHY as possible. Its value can be adjusted to reduce emissions. By slowing down the edge rates on SYSCLK, this 22- $\Omega$  resistor significantly reduces reflections that may occur when the distance between the PHY and link is large (greater than 4 inches in this case).

The link request signal (LREQ) is input to the PHY from the link. The link uses this to initiate a service request to the PHY.

CTL0 and CTL1 are bi-directional signals used to control communication between the PHY and the link. These signals must be directly connected between the PHY and link.

The TSB12LV01B is a 400-Mbps link layer device that uses all data I/O lines (D0-D7) to communicate with the PHY. When status information is received from the PHY, only D0 and D1 are used. The TSB41AB3 is also capable of speeds up to 400-Mbps and provides eight data I/O lines.

C/LKON of the TSB41AB3 is used as both the manager contender programming input and link-on output. Programming is done by tying the terminal through a 10-k $\Omega$  resistor to a high (contender) or low (not contender). If this terminal is tied low, its contender status can also be set via the C register bit. In this schematic, the C/LKON is hardwired to be a contender.

If a power-down option is not implemented, the PD pin on the PHY (pin 18) must be tied to ground through a 1-k $\Omega$  resistor.

### 4 Link-Layer Controller-TSB12LV01B

The TSB12LV01B is a 400-Mbps general-purpose IEEE 1394 link-layer controller. The TSB12LV01B was intended for use in PC peripherals and telecom. It can transfer data between a host controller, 1394 PHY-Link interface, and external devices connected to the local bus interface.

The TSB12LV01B device follows the big-endian architecture. Bit 0 is the most significant bit (MSB).

ADDR0-ADDR7 is the 8-bit host address bus. This bus must be connected to the host processor address bus. All internal memory space (CFR and FIFO) may be addressed with only 6 of the 8 address lines. Address lines 6 and 7 must be grounded. ADDR0 is the MSB of the address lines. It must be connected to the MSB of the host processor address bus, regardless of the host processor endianness.

The 32-bit host interface of the TSB12LV01B was designed to support a Motorola 68K-type microcontroller/microprocessor. The interface supports three access modes: normal, quick, and burst.

DATA0-DATA31 is the 32-bit host data bus. This bus must be connected to the host processor I/O data bus. DATA0 is the MSB of the data lines. It must be connected to the MSB of the host processor data bus, regardless of the host processor endianness.

The BCLK is the clock input to the TSB12LV01B and must be tied to the host output clock. The TSB12LV01B can support clock rates up to 50 MHz.

The  $\overline{CA}$  pin of the TSB12LV01B is the active-low Cycle Acknowledge pin. It is a control signal to the host bus. When asserted, it signals an acknowledge from the TSB12LV01B to the host access cycle. It indicates that the access to the TSB12LV01B configuration register (CFR) space or FIFO is complete.

#### NOTE

If interfacing directly to a Motorola 68K-type microcontroller/microprocessor, the  $\overline{CA}$  pin must be connected to the transfer acknowledge ( $\overline{TA}$ ) pin of the processor.

The  $\overline{CS}$  pin of the TSB12LV01B is the active-low cycle start pin that indicates the beginning of an access to the TSB12LV01B configuration registers or FIFO space.

#### NOTE

If interfacing directly to a Motorola 68K-type microcontroller/microprocessor, the  $\overline{CS}$  pin must be connected to the Transfer Start ( $\overline{TS}$ ) pin of the processor.

$\overline{INT}$  is an active-low Interrupt pin that must be connected to the interrupt pin of the host. When  $\overline{INT}$  is low, TSB12LV01B notifies the host bus that an interrupt has occurred.

$\overline{WR}$  is the read/write enable that must be connected to the WR pin of the host. When  $\overline{CS}$  is low and  $\overline{WR}$  is high, a read from the TSB12LV01B is requested by the host bus controller. To request a write access,  $\overline{WR}$  and  $\overline{CS}$  must be low.

The  $\overline{RESET}$  is the asynchronous system reset to the TSB12LV01B. This pin may be connected to the PHY reset pin, may be controlled by the host controller, or may be controlled via an external reset source.

The CYCLEN input terminal is an optional external 8-kHz clock used as the isochronous cycle clock. This terminal is tied to  $V_{CC}$  since it is not used in this case.

The CYCLEOUT pin is the TSB12LV01B version of the cycle clock. It is based on the timer controls and received cycle-start messages. It must be left open.

GPO0, GPO1, and GPO2 are general-purpose output bits. The power up default function for these terminals is GRFEMP, CYCDE, and CYST respectively. After power up, these terminals may be programmed as general-purpose output pins.

#### **NOTE**

Test headers at the bottom of page 1 of the schematic (Appendix B) are not part of the reference schematic. The test headers are optional and when designed in provide an excellent way of monitoring signals on the different interfaces of the TSB12LV01B link. Some test headers may also be used to generate various bit patterns, which can drive signals on the microcontroller.

## **5 References**

1. *TSB12LV01B, IEEE1394-1995 High-Speed Serial-Bus Link-Layer Controller* (SLLS435)
2. *IEEE Std 1394-1995, IEEE Standard for a High Performance Serial Bus*
3. *IEEE Std 1394a-2000, IEEE Standard for a High Performance Serial Bus – Amendment 1*
4. *IEEE 1394a Three Port Cable Transceiver/Arbiter* (SLLS418)

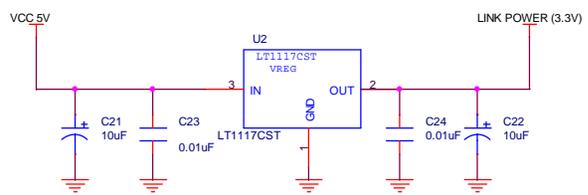
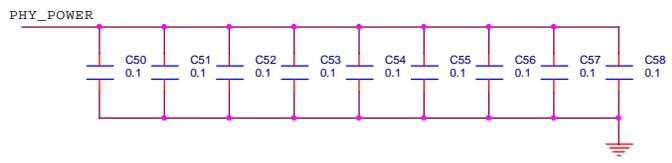
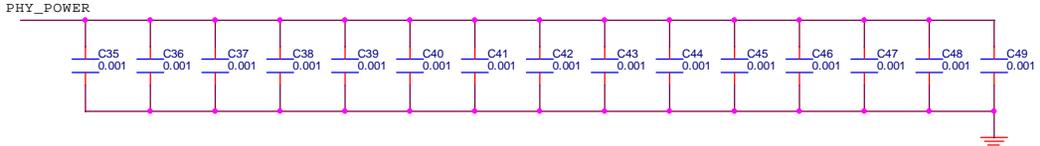
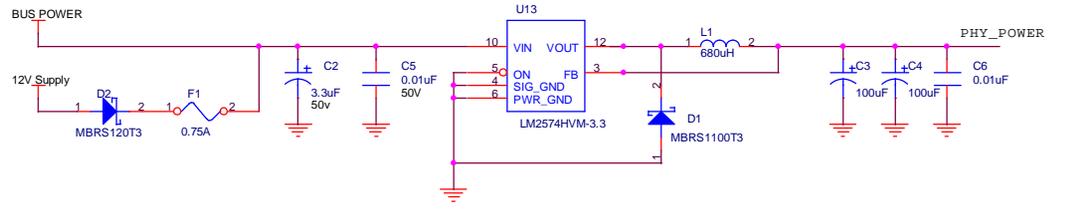
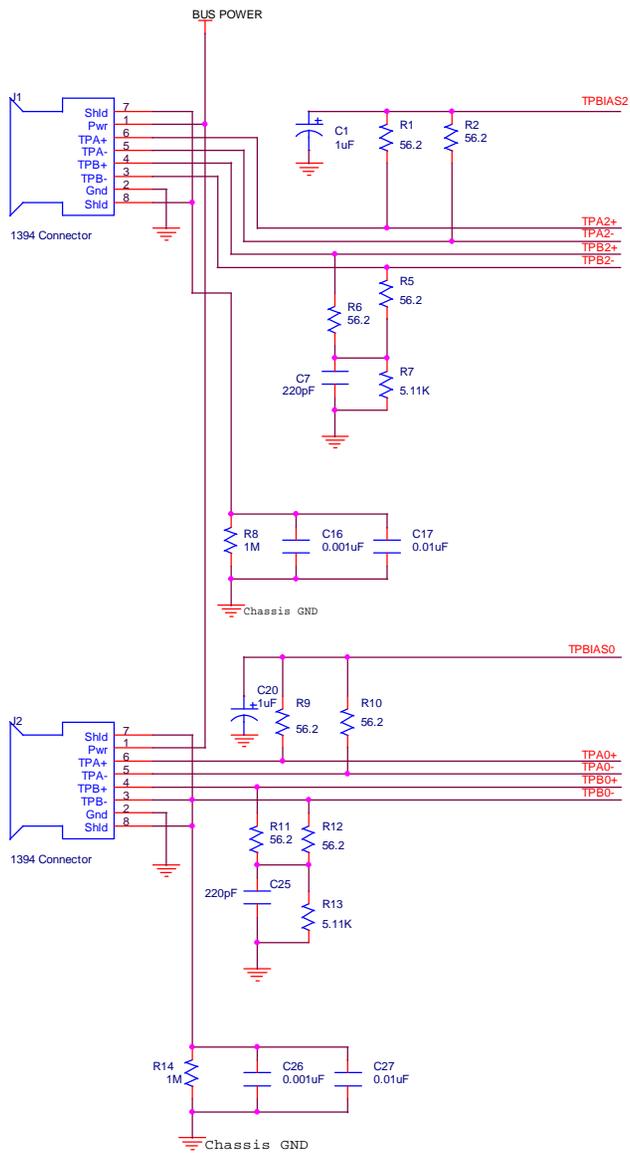
## Appendix A. Parts List for the TSB12LV01B/TSB41AB3 Schematic

The following parts are represented on the schematic pages. Other parts may be used as long as their function and/or parameters meet the IEEE 1394-1995 and IEEE1394.a specifications.

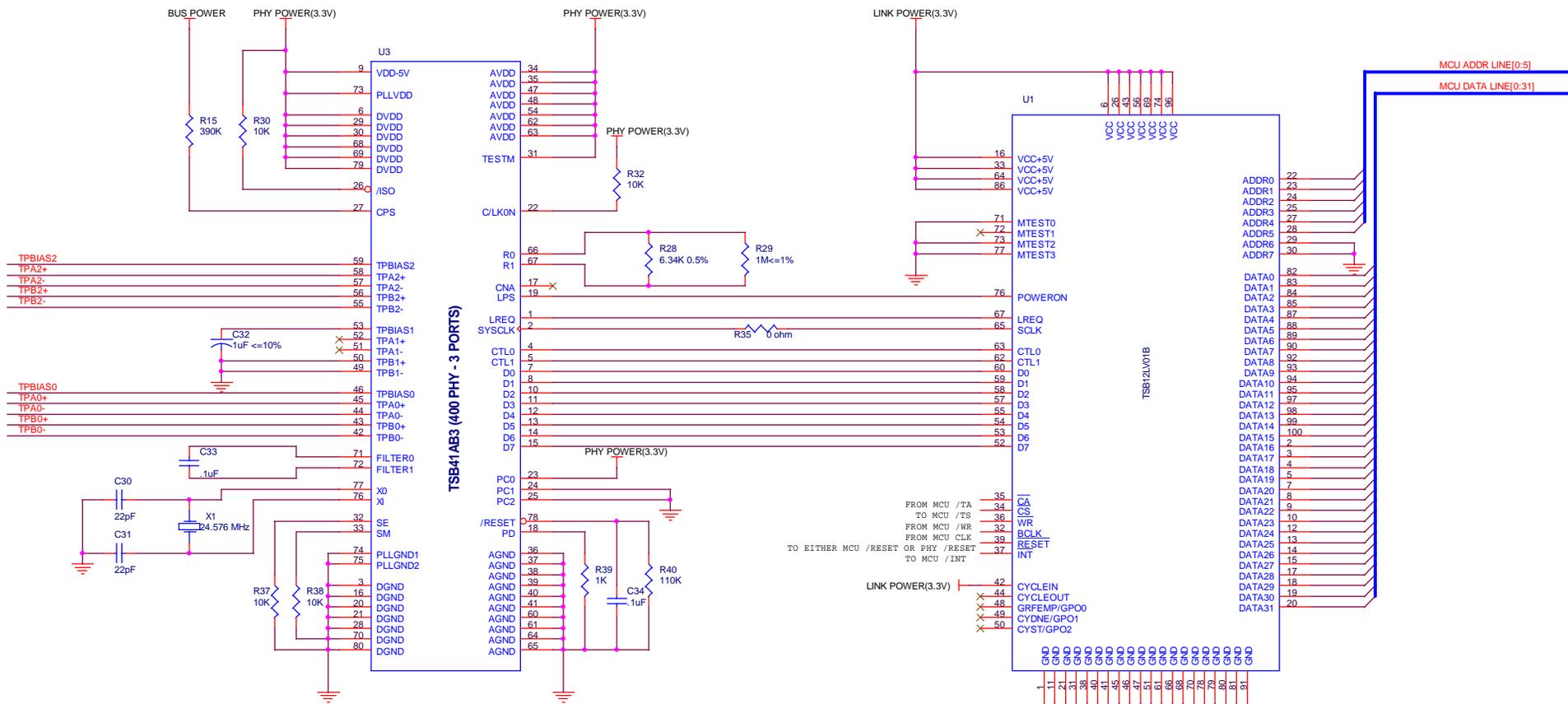
Description	Supplier	Part Number	Package	Quantity	Reference Designator
22 pF 5% Capacitor	Digi-Key	PCC120CNCT-ND	0805	2	C30, C31
220 pF Capacitor	KEMET	C0805C221J5GAC	0805	2	C7, C25
0.001 $\mu$ F Capacitor	KEMET	C0805C102K5RAC	0805	19	C16, C26, C35, C36, C37, C38, C39, C40, C41, C42, C43, C44, C45, C46, C47, C48, C49
0.01- $\mu$ F 10% Capacitor	KEMET	C0805C103K5RAC	0805	8	C5, C6, C17, C23, C24, C27
0.1- $\mu$ F 10% Capacitor	KEMET	C0805C104K5RAC	0805	11	C33, C34, C50, C51, C52, C53, C54, C55, C56, C57, C58
1- $\mu$ F 50 V Capacitor	KEMET	T491A105M016AS	0805	3	C1, C20, C32
3.3- $\mu$ F 50 V Capacitor	KEMET	T491D335K050AS	2816	1	C2
10- $\mu$ F 20% 25-V Capacitor	KEMET	T491D106K025AS	2816	2	C21, C22
100- $\mu$ F 20% 10-V Capacitor	KEMET	T495X107M010AS	2816	2	C3, C4
DIODE	MOTOROLA	MBRS1100T3	1815	1	D1
DIODE	MOTOROLA	MBRS340T3	2824_dio1	1	D2
FUSE, 0.75-A	RayChem	SMD075-2	2920_FUSE	1	F1
1394 R/A Flat Header	MOLEX	53462-0611	Socket_6	2	J1, J2
0- $\Omega$ Resistor	TDK	SLF7032T-681MR16	0805	1	R35
56.2- $\Omega$ 1% Resistor	KOA	RK73H2AT56R2F	0805	8	R1, R2, R5, R6, R9, R10, R11, R12
1-k $\Omega$ 5% Resistor	KOA	RM73B2AT102J	0805	5	R34, R37, R38, R39
5.11k $\Omega$ Resistor	KOA	RK73H2AT5111F	0805	2	R7, R13
6.34-k $\Omega$ 0.5% Resistor1	KOA	RM73H2AT6341D	0805	1	R28
10-k $\Omega$ Resistor	KOA	RM732B2AT103J	0805	5	R30, R32, R36
110-k $\Omega$ 5% Resistor	KOA	RM73B2AT114J	0805	1	R40
390-k $\Omega$ 5% Resistor	KOA	RM73B2AT394J	0805	1	R15

Description	Supplier	Part Number	Package	Quantity	Reference Designator
1-M $\Omega$ 1% Resistor	KOA	RK73H2AT105F	0805	3	R8, R14, R29
Voltage Regulator	National	LM2574HVM-3.3	so14_464	1	U13
LT1117CST-3.3 V	Liner Tech.	LT1117-CST-3.3	sot223	1	U2
1394 3-Port 400-Mbps PHY	TI	TSB41AB3	80-PIN TQFP	1	U3
Link	TI	TSB12LV01B	100-PIN PZ	1	U1
XTAL, 24.576-MHz	FOX	FE-24.576 MHz 50/50/0/+70/15 pF	XTAL_FE	1	X1

## **Appendix B. TSB12LV01B/TSB41AB3 Schematic**



Title		
TSB12LV01B/TSB41AB3 REFERENCE DESIGN		
Size	Document Number	Rev
B		1.0
Date:	Tuesday, September 05, 2000	Sheet 1 of 2



Title			TSB12LV01B/TSB41AB3 REFERENCE DESIGN		
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B					1.0
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