

Performance of MuxIt™ With Different Cable Lengths

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Data Transmission Applications

ABSTRACT

Designers are often faced with the task of moving parallel data from one location to another, over moderate distances, and in the most efficient manner. Over the last few years, a broad spectrum of low-voltage differential signaling (LVDS) serializers have become available in various clock-rate/data-width configurations. This report illustrates the performance of Texas Instruments MuxIt serializer/deserializer devices using different clock-rate/data-widths and different lengths of standard CAT5 UTP cable between the serializer/transmitter and receiver/deserializer. Test results are presented for various widths of parallel data, from 6-bit to 20-bit wide parallel data using the existing, commercially available, MuxIt evaluation module from Texas Instruments. Results are presented graphically showing cable length vs data transfer rate. Detailed BERT results are contained in the Appendix.

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1 Introduction to MuxIt

Transmitting large blocks of parallel data originally required large banks of parallel line drivers and receivers. With the introduction of serializer/deserializer (serdes) devices, such as universal asynchronous receiver/transmitters (UARTs), designers could convert wide parallel data buses to a serial data stream. This allowed smaller, less expensive cables and connectors to be used, and reduced the interference and EMI generated in large cable bundles. The original UARTs allowed 8 parallel bits to be transmitted over a single pair of wires, at speeds approaching 20 Kbps for short distances.

Today, serdes devices are available that can transfer serial data at hundreds of megabits per second (Mbps), but most of these devices have severe constraints (such as number of parallel bits, range of input clocks, distance between serializer to deserializer, etc.) that restrict their use in many applications.

TI developed the MuxIt family to provide a flexible series of serdes devices applicable to a broad range of serialization/deserialization tasks. At present, the MuxIt family consists of three devices introduced at the end of 2000. Additional devices are under development. The three devices available, and used in this report are:

- SN65LVDS150 PLL Frequency Multiplier
- SN65LVDS151 Serializer-Transmitter
- SN65LVDS152 Receiver-Deserializer

The basic operation of the devices and circuit boards is explained in the following paragraphs. If a more thorough understanding of the MuxIt devices or evaluation module (EVM) is desired, the reader can review the datasheets and EVM User's Guide located online and identified in the Reference paragraph at the end of this report.

All results are from tests using the MuxIt EVM. (The MuxIt EVM is commercially available and can be ordered online.) The results show how increased cable length affects bit error rate, using cable lengths of 1m to 30m between the serializer and deserializer.

The results in Figure 1 illustrate the maximum transfer rate using only a short jumper between the serializer and deserializer EVMs. When this jumper is replaced by cabling, and as that cable length is increased, performance should degrade to a point where the link between serializer and deserializer is not longer usable. We determine the maximum data transfer rate for different lengths of cable.

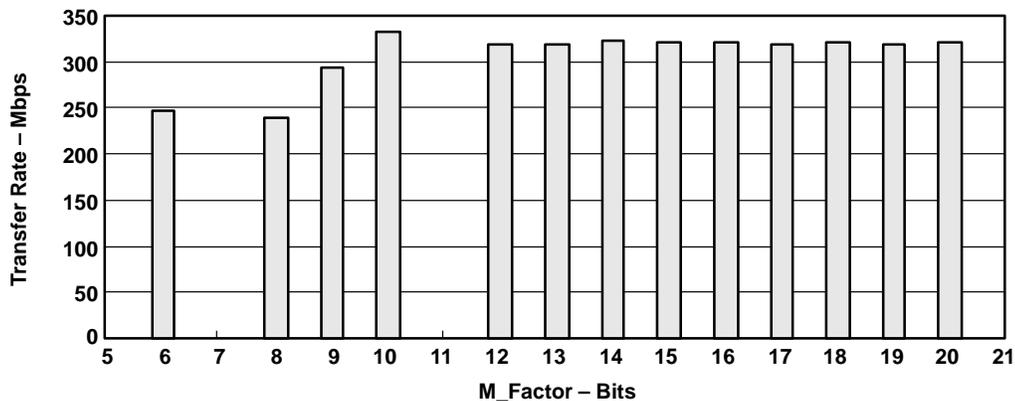


Figure 1. Baseline Data Transfer Rate vs M_Factor Using a 0.1-m Jumper

The transfer rates shown in Figure 1 are determined by multiplying the number of bits being serialized (M_Factor) times the highest input clock frequency for which no bit errors were detected. Note that M_Factors 5, 7, and 11 are not supported by MuxIt devices.

2 Serializer and Deserializer

One of the features of MuxIt devices is their flexibility in terms of the width of data that can be serialized/deserialized. MuxIt devices can be used to handle data from 4-bits wide up to 40-bits wide, transmitting the data using only two twisted pairs. One pair is used to transmit the serialized data while the other pair is for clocking the data. The EVMs allow serialization/deserialization of data up to 20 bits wide.

The MuxIt deserializer performs the opposite function of the serializer. It receives the LVDS signals (CLK and DATA) from the serializer and reconstructs and outputs the same parallel data that was input to the serializer. Again, MuxIt devices support serialization/deserialization of up to 40-bit wide data, but the MuxIt EVMs have been designed to allow evaluation of parallel data up to 20-bits wide.

Simplified block diagrams of the serializer and deserializer EVMs are shown in Figure 2.

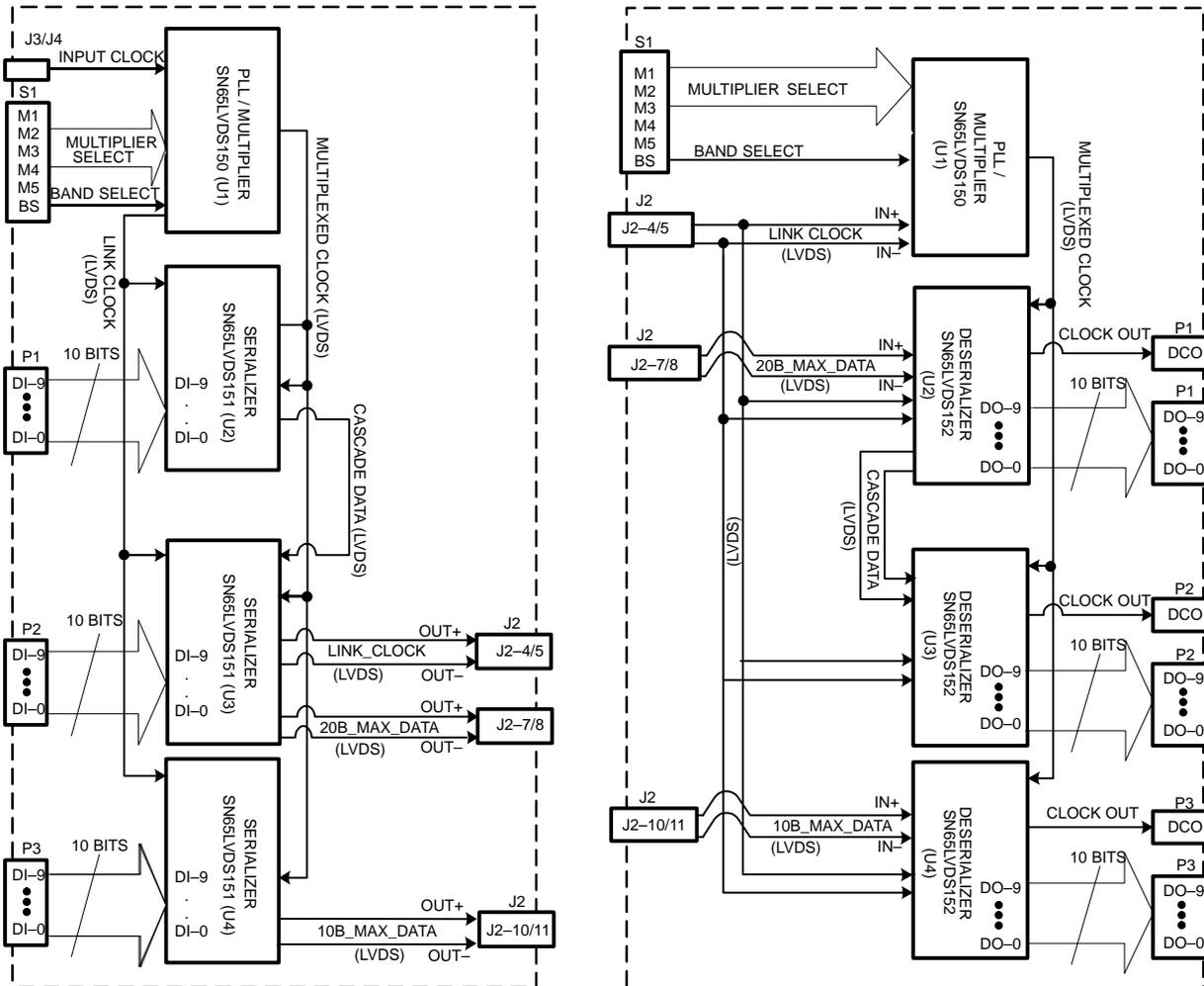


Figure 2. Simplified Block Diagram of the Serializer and Deserializer EVMs

Notice the *Cascade Data* link from U2 to U3 on both the serializer and deserializer. This link allows the 10 serialized data bits from U2 to be combined with the 10 serialized data bits from U3. The *20B_MAX_DATA* signal from U3 contains this 20-bit data stream and will be routed /connected to the deserializer. The other signal of interest is the *LINK CLOCK*, which is also routed/connected to the deserializer. The *LINK CLOCK* signal contains the timing used by the deserializer PLL to correctly convert the serial data back to parallel 20-bit wide data.

As with any data transmission scheme, the quality and length of the interconnecting media can play an important part in determining the overall performance. This report will illustrate how cable length effects performance for different widths of parallel input data.

3 Interconnects and Cables

The LVDS interface used between MuxIt devices complies with the TIA/EIA-644-A standard. The standard specifies the requirements for an electrical layer of a differential (balanced) interface. Although the standard defines a theoretical maximum signaling rate of 1.923 Gbps, this rate can only be achieved across a short trace length on a printed circuit board. As the transmission distance increases, the effects of connectors and cabling reduce this rate. Cable effects can become the primary factor limiting system performance once lengths of tens of meters have been reached.

As mentioned earlier, one key feature of MuxIt is its flexibility. This applies to the extremely wide operating range that it can support. The PLL device (SN65LVDS150) can support input clocks as low as 5 MHz and as fast as 50 MHz. At present there is no other LVDS serdes device available that can support this wide range of input clocks. This feature is important because the MuxIt PLL accepts input reference clocks below 20 MHz, which allows operation over longer cables. Of course, the maximum distance will be dependent on the specific cable used.

Since cable quality contributes strongly to signal quality, cable requirements should be evaluated in detail. One standard, TIA/EIA-568A Commercial Building Telecommunications Cabling Standard, defines the transmission requirements for commercial building telecommunication wiring. It classifies cabling into different categories based upon attenuation and crosstalk losses over frequency. Twisted-pair is classified in different categories, abbreviated CAT X. CAT3 is characterized up to 16 MHz, CAT4 to a maximum of 20 MHz, and CAT5 for 100 MHz and above. Most LVDS applications requiring cabling utilize CAT5 cable. The allowable attenuation vs frequency for CAT5 cable specified in TIA/EIA-568A is shown in Figure 3.

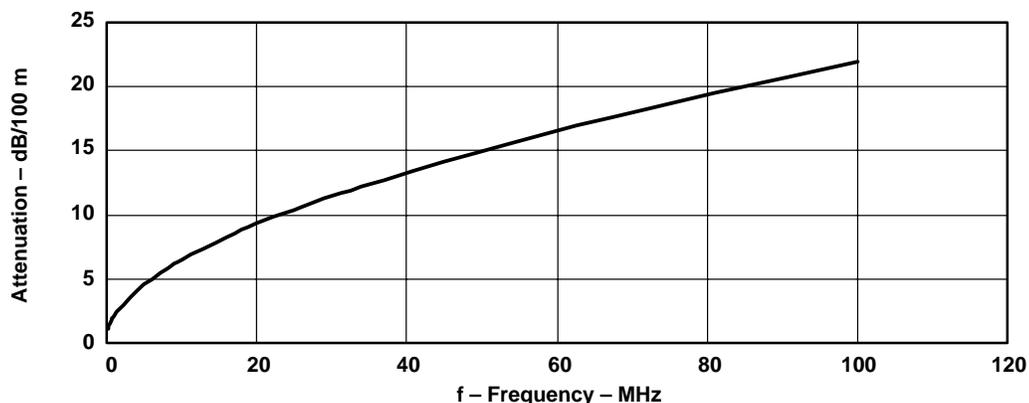


Figure 3. Attenuation vs Frequency for CAT5 Cable

3.1 Cable Selection

The low frequency range of the MuxIt PLL results in its being able to support cable interconnects of several meters. Belden's MediaTwist™ cable (part number 1872A) was selected as the interconnect between serializer and deserializer for this report. This cable was selected for two reasons; 1) its performance with LVDS devices is documented in other TI application reports [see References in Section 7], and 2) it is a commercially available, commonly used, CAT5 cable with good performance/cost characteristics. Specifications for the cable can be found on the web at: <http://ecom.belden.com/>

3.2 Connections

The connectors are part of the transmission line between serializer and deserializer, and in most systems, there is a connector at both cable ends, so care should be taken in selecting connectors that will have a minimum impact on system performance. Connectors should be selected which match the characteristic impedance of the transmission line being used, with a minimum amount of attenuation. The connector used on the MuxIt EVM is a very simple BergStick 12-row female header. Using female headers on the edge of the PWBs allows either a male header (12-pin, .100 mil center, male adapter header) or individual wires (stripped back at each end of the cable) to be inserted into the proper female header. For these tests, both a male-to-male adapter header as well as bare conductors were used. For those tests simulating an extremely short cable, the male-to-male adapter was used, and during the longer cable lengths, the ends of the twisted pair were simply stripped of insulation and the bare conductors inserted into the female headers on the edge of the serializer and deserializer boards.

3.3 Terminations

Interconnection lengths greater than just a few centimeters require that the interconnection be terminated. This termination should match the characteristic impedance of the interconnecting cable. The nominal characteristic impedance of Belden 1872A MediaTwist cable is 100 Ω \pm 20%, and the termination resistors on the deserializer are 100 Ω .

4 Measurements

4.1 Test Setups

The majority of testing was performed using the HP 3-GHz bit error rate tester (BERT).

This is a single channel BERT capable of running from 16.1 MHz up to 3 GHz. Tests were performed by transmitting both pseudo-random binary sequence (PRBS) data and clock through the serializer and deserializer. This means that both data and clock had to be properly recovered to avoid errors. The basic test setup is shown in Figure 4. V_{CC} (power supply not shown) was set to 3.3 Vdc with a common supply used for both PWBs. Eye-pattern measurements were taken of the high-speed serialized data and clock (LVDS signals), as well as the deserializer output. The eye patterns on the output of the deserializer are low speed and appear very clean with extremely low jitter. (see paragraph 5.3) Unfortunately, bit errors cannot be detected in an eye-pattern, which is the reason for performing BERT testing.

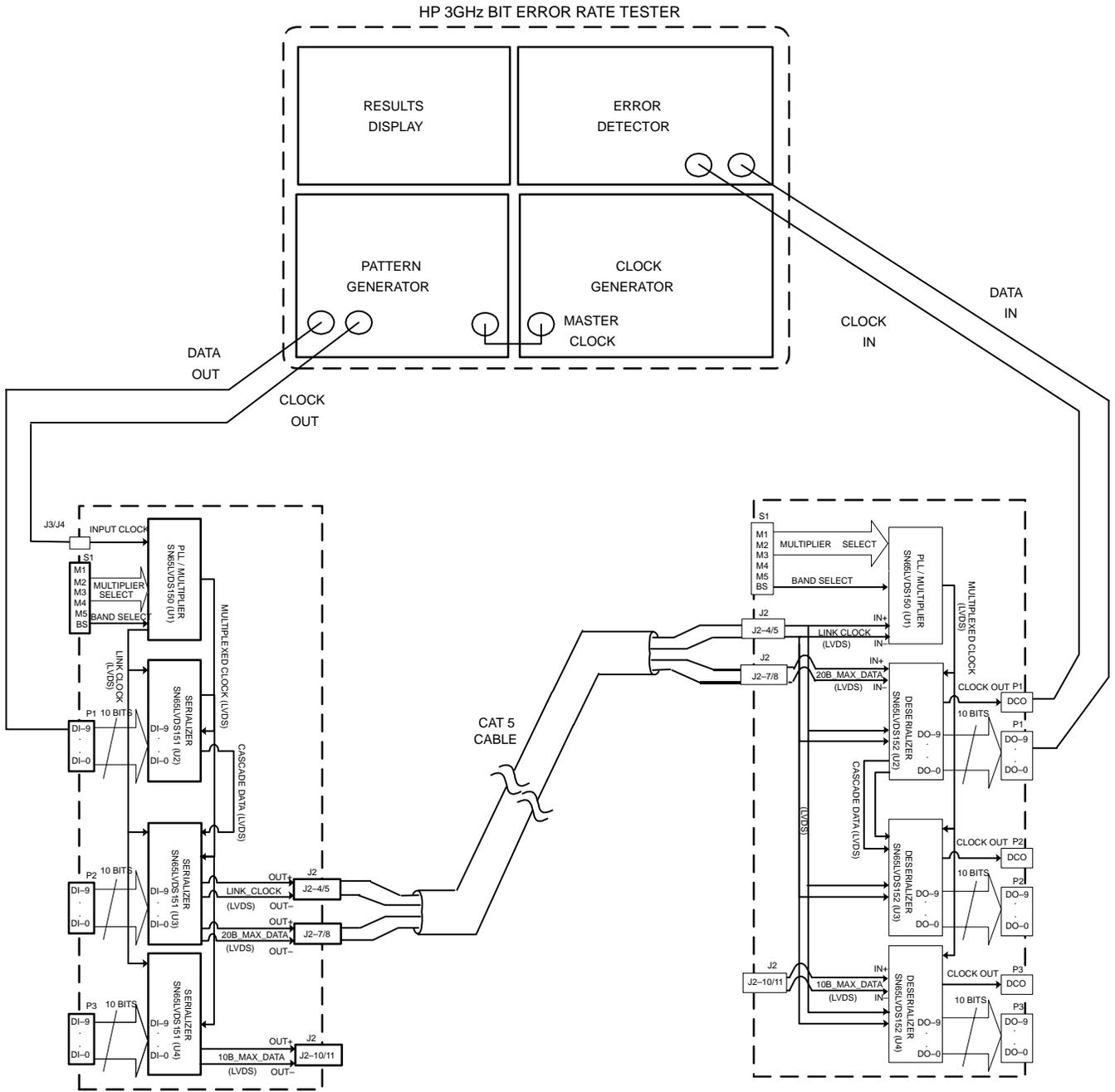


Figure 4. BERT Test Setup Block Diagram

4.2 EVM Configurations

The serializer and deserializer were connected using different lengths of MediaTwist™ cable. The *20_bit_max* LVDS pair and *Link_Clock* signals were connected between the J2 connectors on each board. No other connections between the EVMs were made. During the tests, different multiplication factors (*M_Factors*) were used to simulate different widths of parallel single-ended data being input to the serializer. Unused inputs were set to a logic 0 to provide worst case intersymbol interference (ISI) effects. For example, when the PRBS out of the BERT was a sequence 010 and 10 bits (*M_Factor* = 10) were being transmitted, the serialized *20_bit_max* would contain

```
0000000000 1000000000 0000000000
```

with the BERT PRBS being applied to Bit 0. In addition to configuring the *M_factors* (using onboard switch *S1*), the onboard jumpers were set in the enable position for all functions on the boards. The clock input to the serializer was made using a single-ended input from the BERT. This required that the *Vth* jumper on the serializer PWB be installed to allow the clock reference inverting input (*CRI-*) be set to $V_{cc}/2$.

4.3 BERT Measurements

The BERT equipment can provide outputs in different formats. The results presented here are in standard error ratio format. This ratio is simply the number of wrong data bits detected (bit errors) divided by the total number of data bits received. BERT tests become more accurate as the sample size increases, but increases test time. The BERT *CLK_OUT* could have been routed directly to the BERT *CLK_IN* and not routed through the EVMs. But, by sending the clock through along with the data, any timing, skew, or clock errors would also generate bit errors.

For the BER tests in this report, the measurements were collected after 4 minutes for BERs of 10^{-8} or less (worse performance) and 10 minutes for BERs of 10^{-9} or better. If no errors were detected after 10 minutes, a default value of 10^{-14} was used. Tests were performed by increasing the signaling rate (*Clock_Out* and *Data_Out* from the BERT) incrementally, and recording the BER at each rate. The results of the BERT measurements are summarized by presenting the equivalent data transfer rate obtained. The detailed BER charts for each *M_Factor* are contained in Appendix A.

4.4 Eye-Pattern Measurements

As the BER results will indicate, the system is impacted by cable length between the serializer and deserializer, which requires an examination of the high-speed data link at the deserializer inputs. These results will be presented in standard eye-pattern format.

5 Results

5.1 BERs for Signaling Rate vs *M_Factor* (Data Width)

The initial tests were performed using a jumper between the PWBs, which acts as an extremely short cable. These results are a baseline showing the maximum performance that can be achieved, with performance being limited by the board layout and connector effects. The BER results have been converted to a transfer rate and presented in Figure 5. This shows the maximum *error-free* transfer rate for each *M_Factor*. The detailed BER results are presented in Appendix A.

As expected, these results show that the number of bits being serialized determines the maximum rate those bits can be transmitted. There is a gap between M=10 and M=12 that appears rather large. This is due to two factors: 1) there is no curve for M=11 (it is not supported by the PLL), and 2) this is the point that the cascade data port is used to combine the full 10 bits from device U2 with an additional two data bits from U3 (for the total of 12 bits).

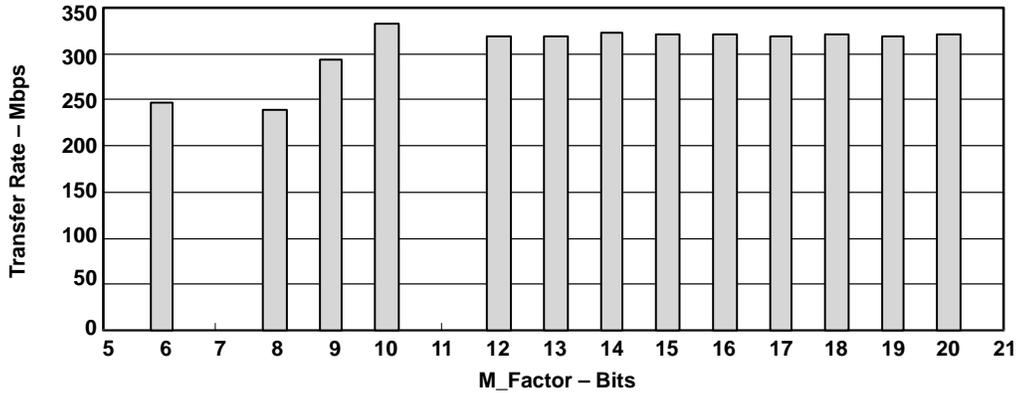


Figure 5. Equivalent Data Transfer Rate vs M_Factor With Jumper Interconnect for Cable Length = 0.1m

Presented in this manner, the ideal case would be for all M_Factor values to result in the same data transfer rate. However, the results indicate that performance of M=6, 8, and 9 is slightly slower than M_Factors of 10 or more. The highest transfer rate was obtained with 10 parallel bits being serialized (M_Factor =10) and the MuxIt serializer taking in the data at 32.5 Mbps on each of the 10 inputs (resulting in a 325 Mbps transfer rate).

5.2 Signaling Rate vs Cable Length

Tests were run with the cable lengths changed to 1-m, 3-m, 10-m, 20-m, and 30-m cables. The maximum transfer rates are shown in Figure 6 through Figure 10 respectively.

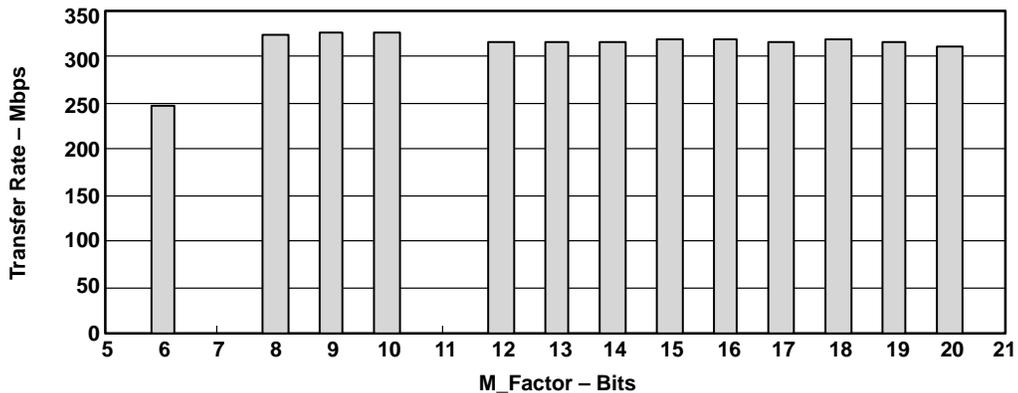


Figure 6. Maximum Data Transfer Rate vs M_Factor for Cable Length = 1 m

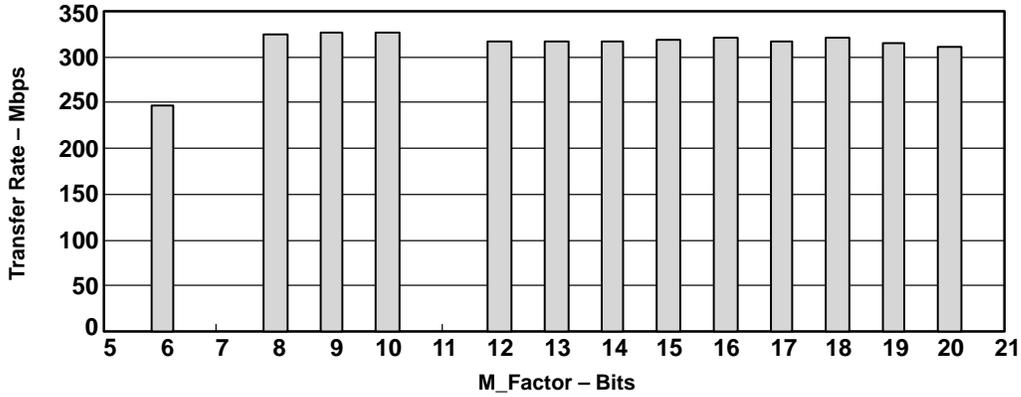


Figure 7. Maximum Data Transfer Rate vs M_Factor for Cable Length = 3 m

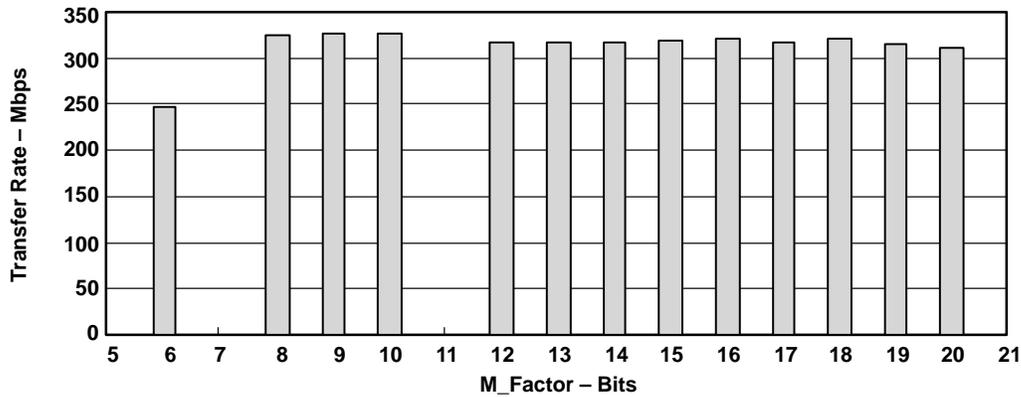


Figure 8. Maximum Data Transfer Rate vs M_Factor for Cable Length = 10 m

The results shown in Figure 6 through Figure 8 are virtually identical. The results did not change as the cable length increased from 1 m to 10 m. Performance degradation could be seen using a 20 m cable as shown in Figure 9.

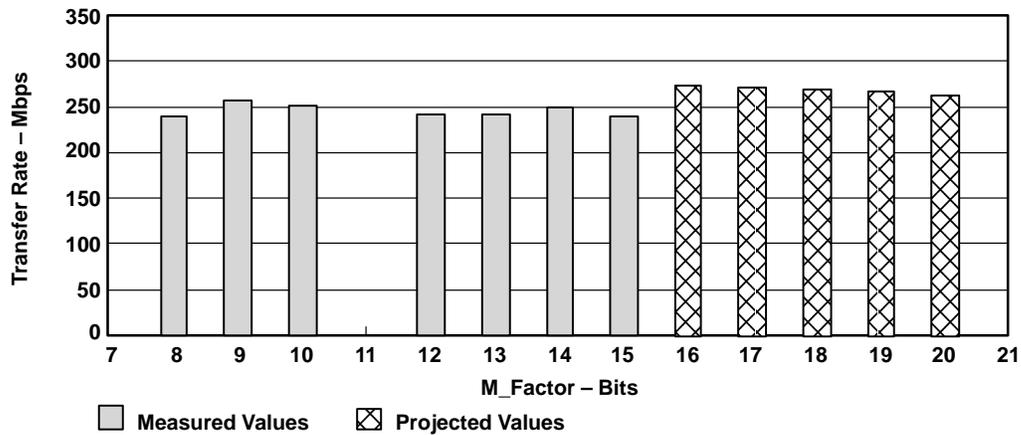


Figure 9. Maximum Data Transfer Rate vs M_Factor for Cable Length = 20 m

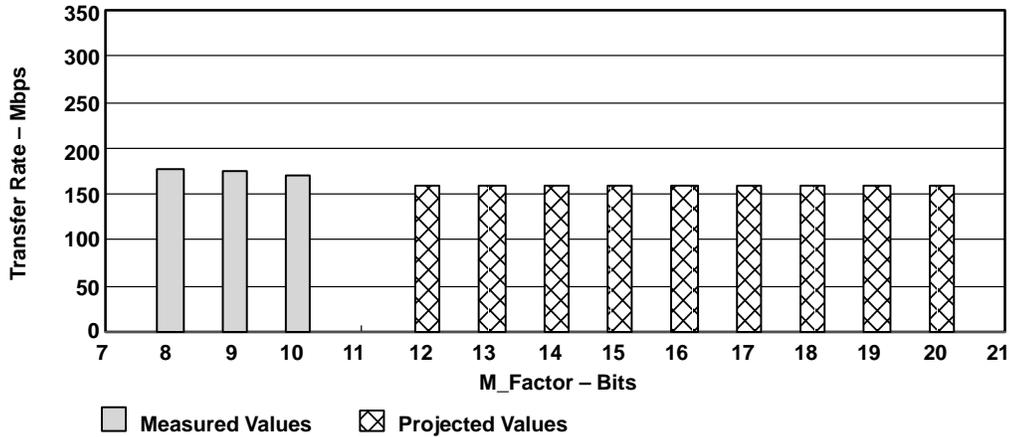


Figure 10. Maximum Data Transfer Rate vs M_Factor for Cable Length = 30 m

The results for 20 m and 30 m cables contain projected values based upon the results obtained for transfer rates using cables up to 10m. It uses the same percentage of degradation from M_Factor =10 to M_Factor =12 measured for the shorter cable lengths, this degradation can be attributed to the cascade performance of the devices themselves and not caused by the cable interface. In other words, as M_Factor changes, the transfer rate remains constant and therefore the cable effects remain constant.

5.3 Eye-Pattern Measurements

Eye-Pattern measurements were taken to determine what observations could be made about maximum signaling rate versus cable length. In Figure 11, the 20-m cable was installed between the serializer and deserializer, and a M_Factor of 12 was selected.

During the BERT measurements, only a single channel was exercised at a time, with all other channels containing a logic 0 bit. As mentioned earlier, this created a worst-case ISI. During the eye-pattern measurements, Bit 1 and Bit 11 were tied to a logic 1. Pseudo-random NRZ data from the BERT was input to Bit 3. Another pattern generator was used to provide PRBS NRZ data to Bit 6. A logic 0 was applied to the remaining inputs bits (2, 4, 5, 7, 8, 9, 10 and 12). The vertical cursor near the center of the figure shows the rising edge of the link clock on Channel 2 of the scope. The corresponding point on the Channel 3 waveform is the rising edge of bit 11 (not bit 1). This is due to the timing of the output signals controlled by the PLL in the SN65LVDS150.

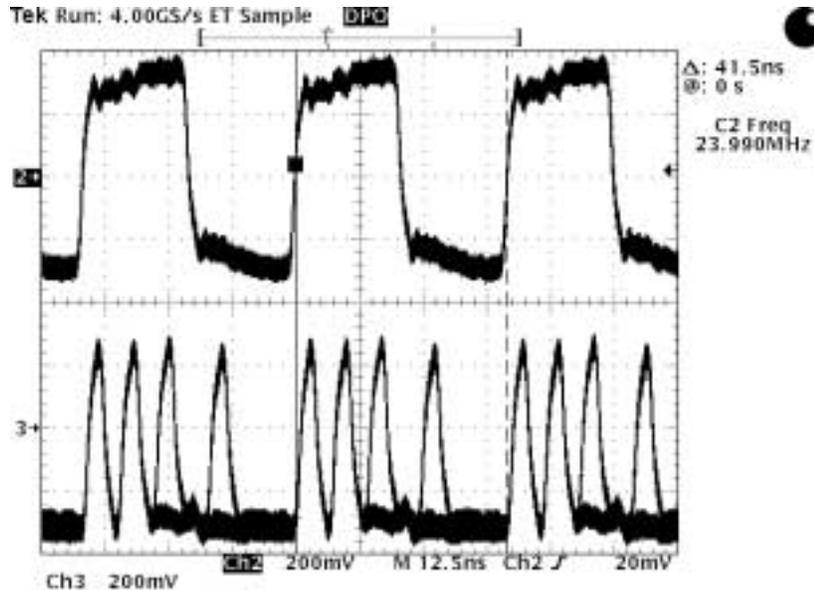


Figure 11. Link Clock and 20_Bit_Max LVDS Signals

It should be noted that the system performance improved when other channels were active, and this confirms that ISI was impacting system performance. During the earlier tests under these conditions, the maximum signaling rate for the 20-m cable and M_Factor =12, was approximately 20.5 Mbps. The reduction of ISI by introducing NRZ data on other channels increased the maximum error-free signaling rate to 23.5 Mbps, roughly a 10% increase in throughput. The LVDS lines were examined as the signaling rate was increased to 24 Mbps to see if any indication could be seen as errors began to occur. The BERT results at 24.0Mbps were 1.1×10^{-4} , yet no visible change was detected by monitoring the LVDS lines using an oscilloscope. However, a phenomenon at the deserializer output was observed as shown in Figure 12. With the oscilloscope display set to infinite persistence, a small duty cycle change in the DCO output was observed. This added approximately 3.5 ns to each falling edge of the DCO clock output. This was the only change that was observed as signaling rate was increased and BER deteriorated from 1×10^{-12} (at 23.5 Mbps) to 1.1×10^{-4} (at 24 Mbps). The bottom trace (oscilloscope Ch. 3) in Figure 12 is the deserializer output from data bit_0, and provides a good example of the limitations of eye-pattern measurements. The eye-pattern indicates a very clean, low jitter output from the deserializer. Unfortunately, it does not indicate that there are errors in the data being output. This is why BER measurements are performed on serdes systems.

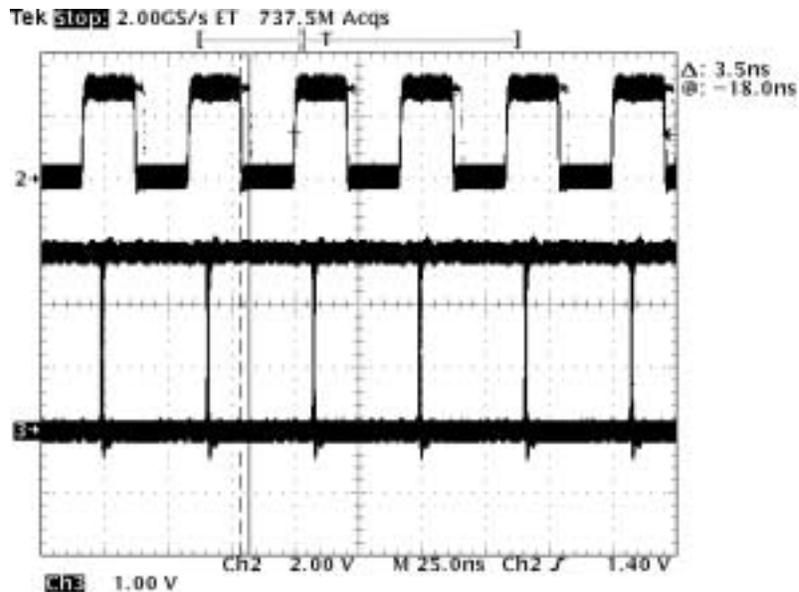


Figure 12. Clock Output (DCO) and Deserializer Output (Data_Out_Bit_0)

6 Conclusion

We have shown that MuxIt performs well using CAT5 cable, as well as the limitations in signaling and transfer rate that come into play as cable length is increased beyond 10 m. MuxIt devices can be used successfully for cable lengths exceeding 10 meters. This has been demonstrated for cable lengths up to 30 m using standard CAT5 cable. Data collection was limited to a maximum cable length to 30 m, but performance beyond that length can be assumed, with a proportional decrease in signaling rate. The practical limitations can be estimated to be approximately 40 m. This is estimated based on the data presented in Figure 13. It shows that the maximum data transfer rate decreases approximately 80 Mbps from 10 m to 20m and decreases an additional 80 Mbps as the cable length is increased from 20 m to 30 m. If it is assumed that another 80 Mbps would be lost going from 30 m to 40 m, then the maximum transfer rate would be in the range of 80 Mbps. This would translate to an input reference clock of 8 MHz for 10-bit wide data and a 6.5 MHz input reference clock for 12-bit data. This is approaching the minimum allowable input frequency to the PLL. Performance using a 20-bit input, with a system bandwidth (transfer rate) of 80 Mbps, would not work because the reference input required would be $(80 \text{ Mbps}/20 \text{ inputs})$ 4 MHz, which is less than the minimum specified input clock of 5 MHz.

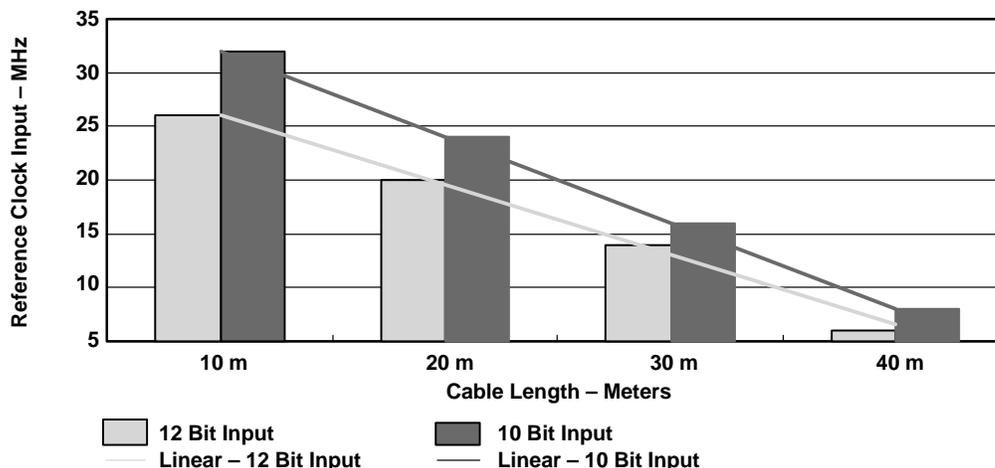


Figure 13. Range of Input Clock vs Cable Length

Finally, system performance presented here was obtained from the MuxIt evaluation module. System designers can use the layout and signal routing information contained in that manual as guidelines in the layout of their specific circuit boards.

This extremely wide range of performance is only possible due the wide operating bandwidth of the MuxIt PLL. As cable lengths increase, MuxIt can support reference clock inputs as slow as 5 MHz. No other product presently available provides either this wide range of PLL inputs, or the ability to select the width of the parallel data into the serdes system. Products that require higher frequency reference clock inputs, of 40 MHz or more, may not work in applications requiring long runs of CAT5 cable.

7 References

1. Data Sheet for the SN65LVDS150, *MuxIt PLL Frequency Multiplier*
2. Data Sheet for the SN65LVDS151, *MuxIt Serializer-Transmitter*
3. Data Sheet for the SN65LVDS152, *MuxIt Receiver-Deserializer*
4. *The MuxIt Data Transmission System Applications, Examples, and Design Guidelines*, Application Report (literature number SLLA093), Dec 2000
5. *MuxIt_Evaluation_Module_EVM_User's_Guide* (literature number SLLU023), Jan 2001
6. *MEDIATWIST™ – 5: 1872A Specification Rev 6*, Belden Technical Paper, Dec 1999
7. *Performance Of LVDS With Different Cables*, Application Report (literature number SLLA053), Aug 1999
8. *High-Speed Giga-Bit Data Transmission Across Various Cable Media at Various Lengths and Data Rate*, Application Report (literature number SLLA091), Nov 2000
9. *Measuring Crosstalk in LVDS Systems*, Application Report (literature number SLLA064), Jan 2000

Appendix A

BERT measurements were performed and recorded for each cable length and M_Factor. The results of the detailed BERT measurements are contained here for reference. These results were used to generate the transfer rate graphs contained in the body of the report.

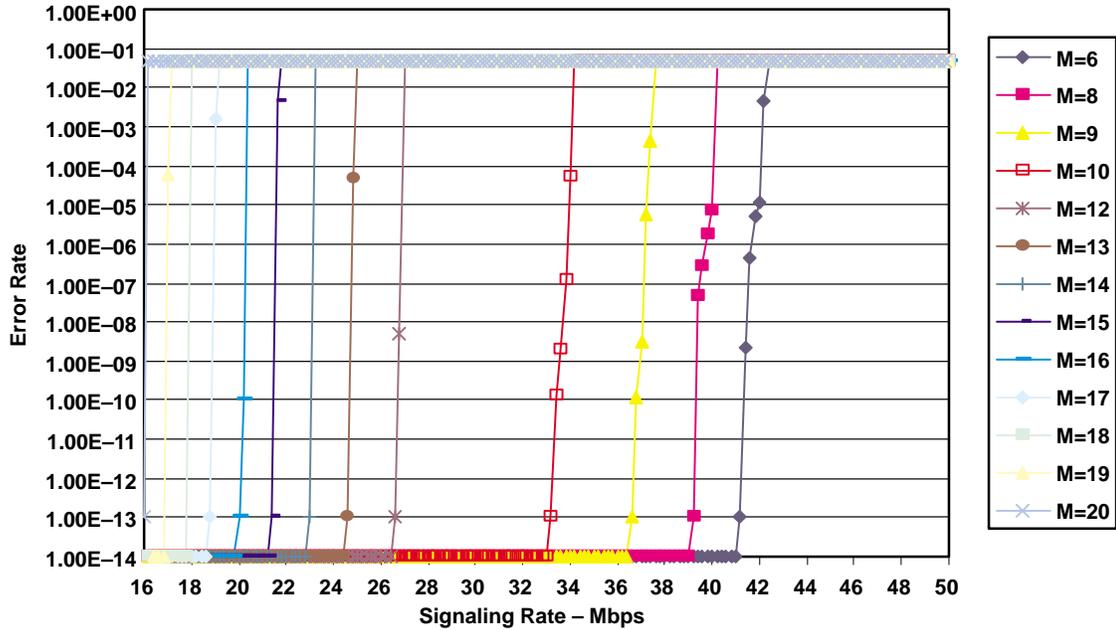


Figure A-1. BER vs Signaling Rate for Various M_Factors for a Jumper Interconnect

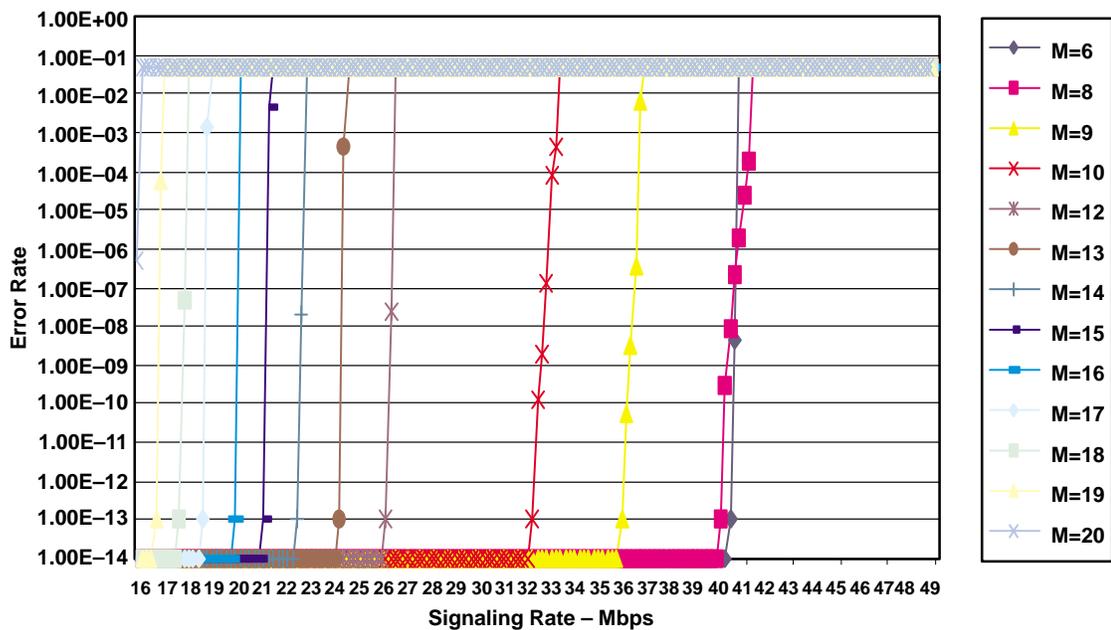


Figure A-2. BER vs Signaling Rate for Various M_Factors With 1-m Cable

During tests with M_Factor=6, the failure mode appeared to be loss of clock input to the BERT, indicating that the upper limit of the deserializer DCO had been reached.

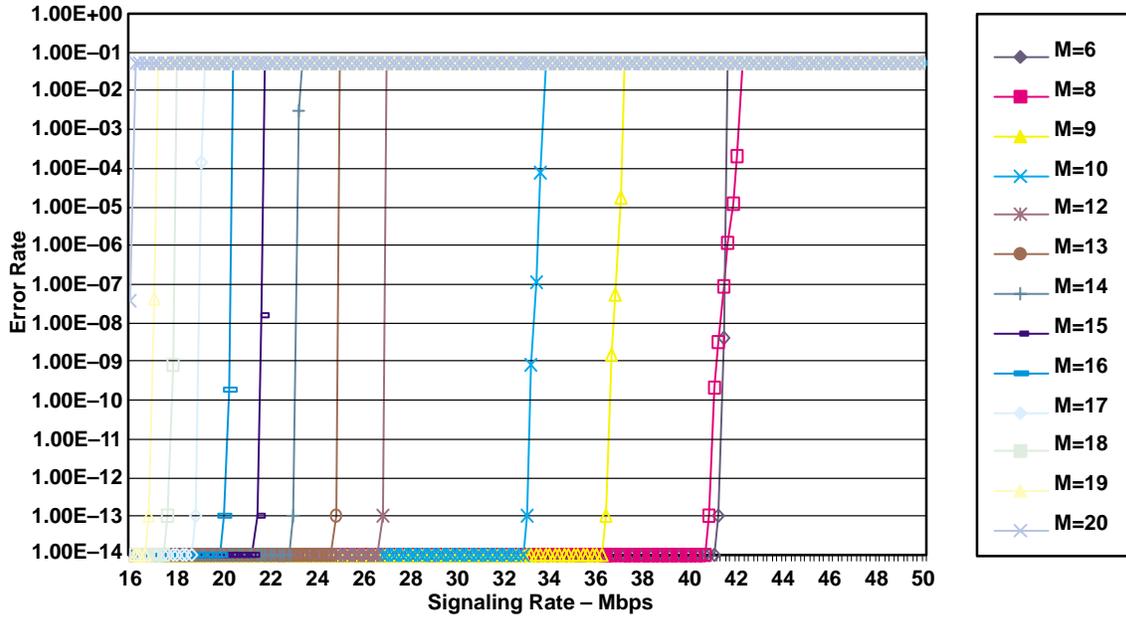


Figure A-3. BER vs Signaling Rate for Various M_Factors With 1-m Cable

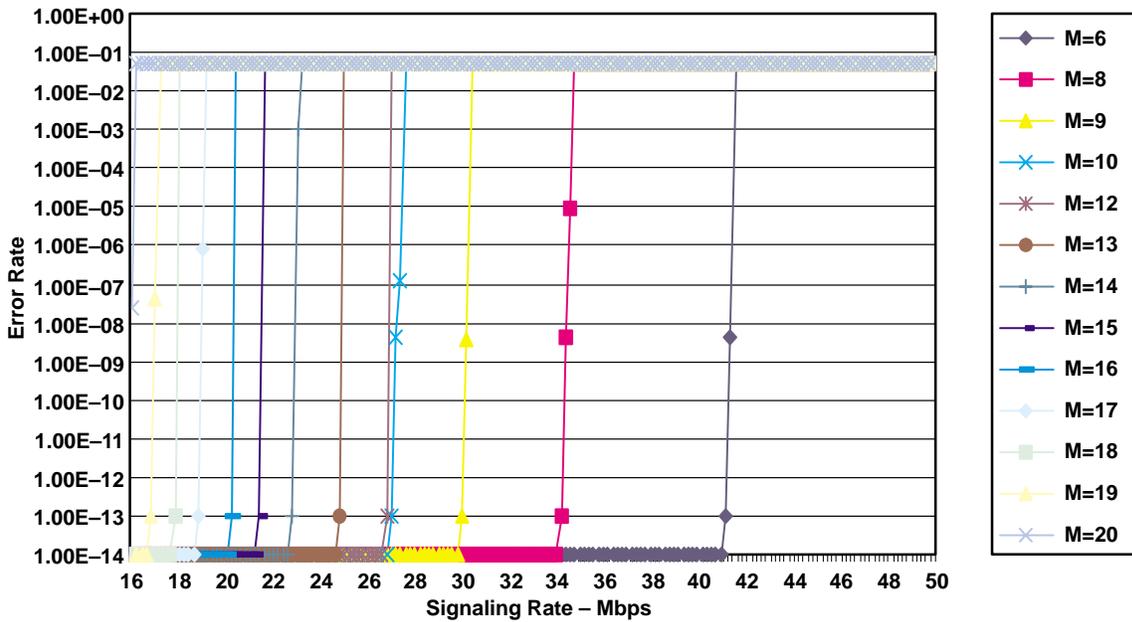


Figure A-4. BER vs Signaling Rate for Various M_Factors With 10-m Cable

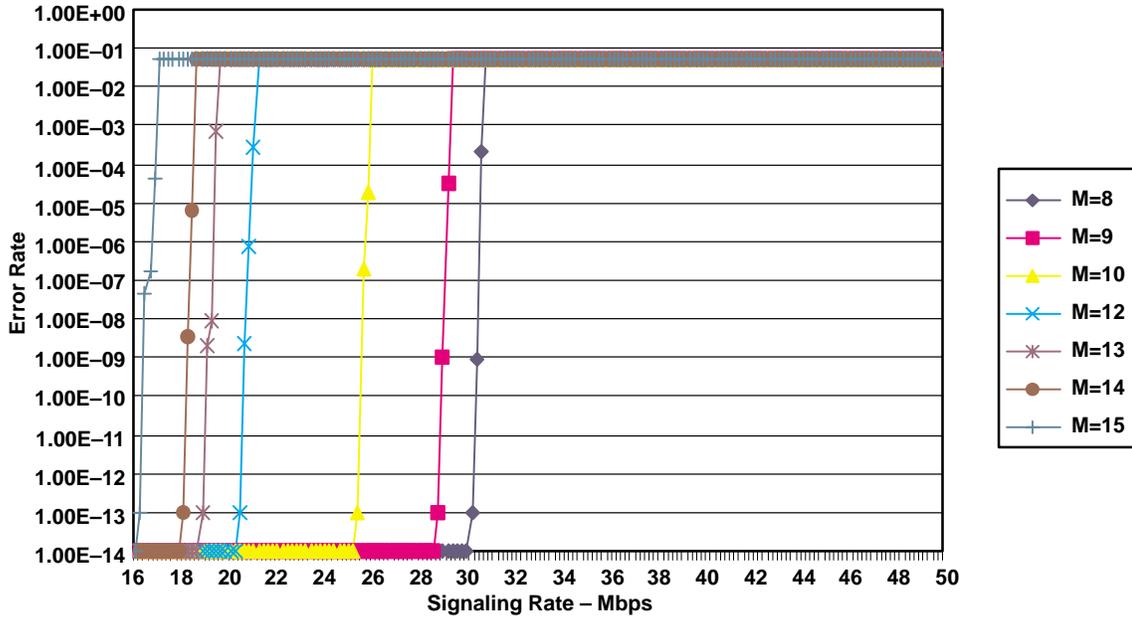


Figure A-5. BER vs Signaling Rate for Various M_Factors With 20-m Cable

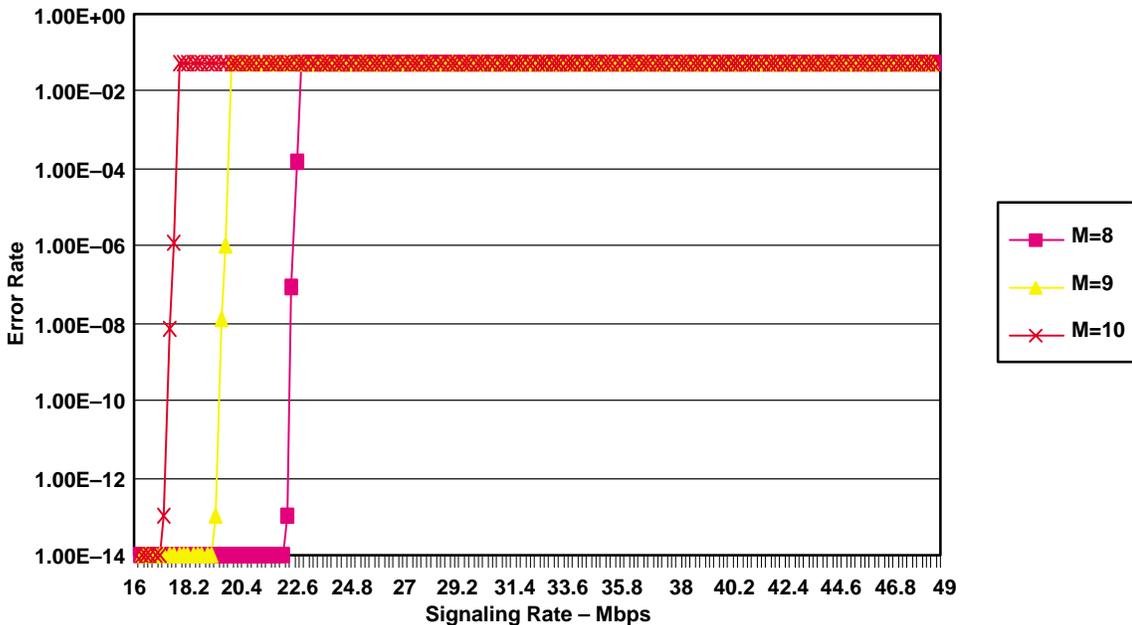


Figure A-6. BER vs Signaling Rate for Various M_Factors With 30-m Cable

Clearly, using 10-m cable lengths or longer directly effected the maximum achievable signaling rate. Examining higher multiplication factors with longer cables would have been interesting, but the 16.09 Mbps limitation of the test equipment made that not possible.

Another way to examine these results is to look each individual M_Factor and plot the performance of each cable. This can be achieved by taking the individual M_Factor curves from Figure A2 through Figure A6, plotting them for each M_Factor, and discussing the results with each of the following figures.

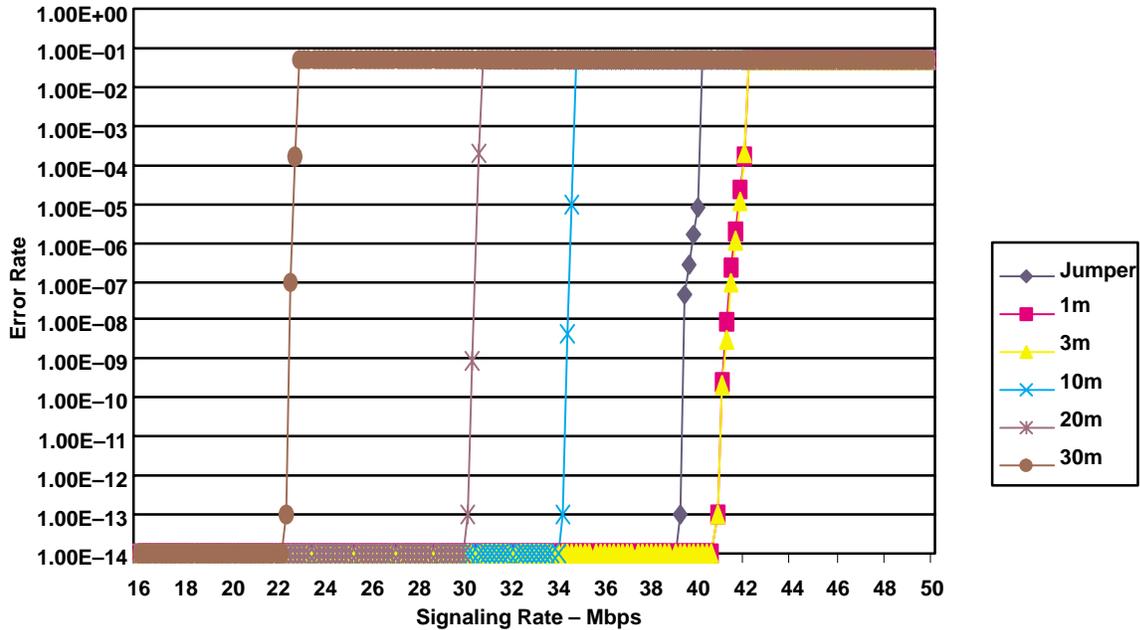


Figure A-7. BER vs Signaling Rate for Various Cable Lengths (M_Factor = 8)

Notice that the 1-m and 3-m cables slightly outperform the jumper. This is similar to the results obtained when measuring cable length vs signaling rate tests and during multi-drop tests that are contained in application reports SLLA053, *Performance of LVDS With Different Cables* and SLLA054, *LVDS Multidrop Connections*. The reason for this is that small perturbations in the transmission line, board traces, connectors, and termination resistors can all have a combined effect that reflects back to the driver and returns down the transmission line. Performance with even short lengths of cable improves as the cable acts to attenuate these reflections and reduced their effect of system performance. However, as the cable length increases past this 1-to 3-m length, the negative effects of longer cable come into play. Line capacitance, attenuation, crosstalk, and skin effect all begin to reduce system performance. This should be consistent regardless of the specific multiplier used.

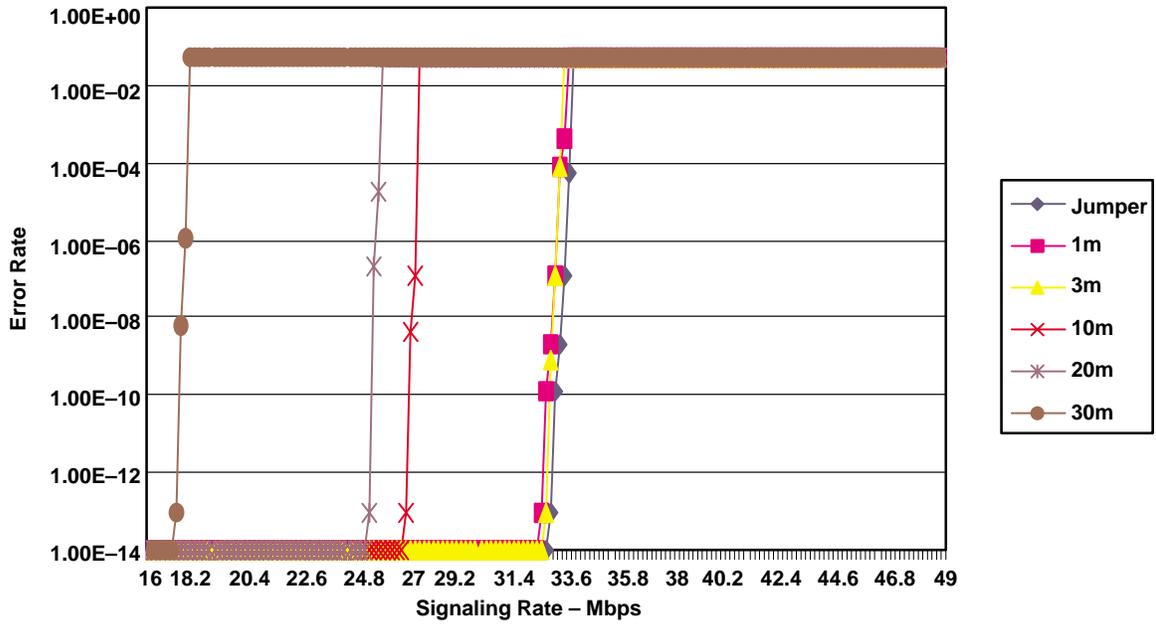


Figure A-8. BER vs Signaling Rate for Various Cable Lengths (M_Factor = 10)

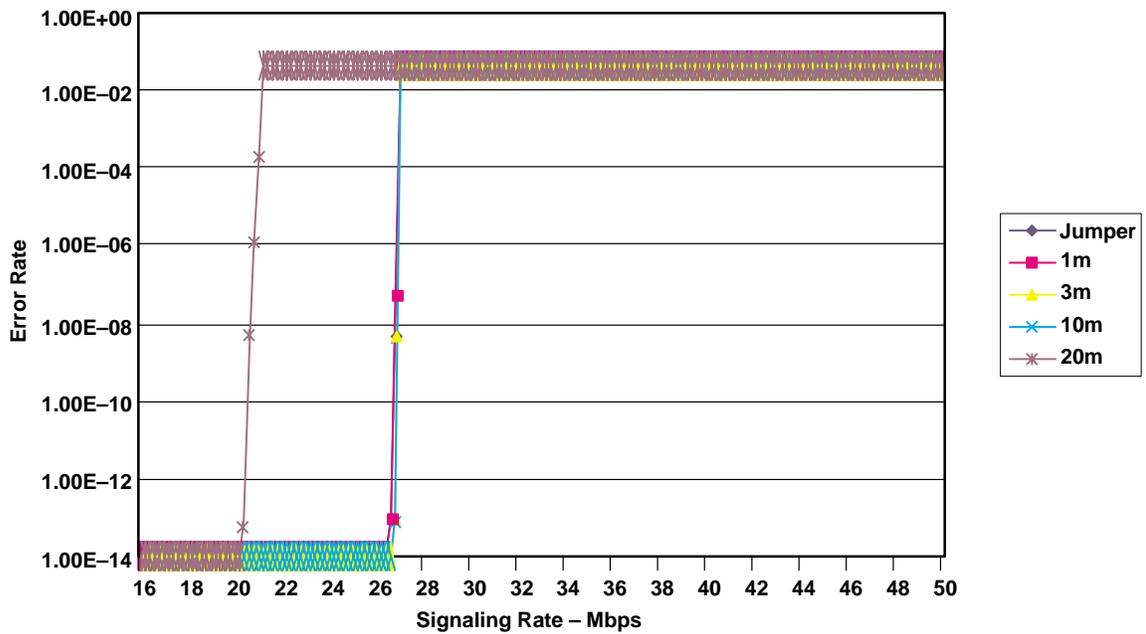


Figure A-9. BER vs Signaling Rate for Various Cable Lengths (M_Factor = 12)

The results contained in Figure A–9 show very little difference using cables of 10 m or less. Figure A–10 contains an expanded view of the shorter cable lengths to see what the detailed effects and difference in cable lengths are.

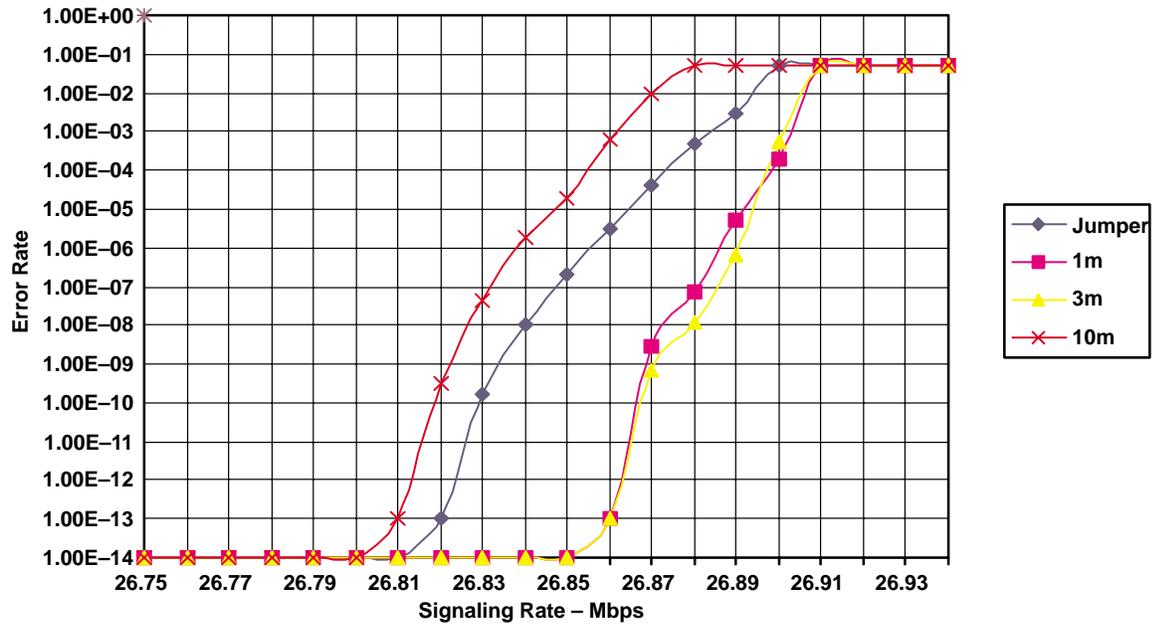


Figure A–10. Expanded View of BERT Results (M_Factor = 12)

The results shown in Figure A–10 show that performance using cable lengths of up to 10 m has very little impact, but the performance using 20 m is off this expanded view, which indicates that performance degrades quickly as cable length is increased beyond 10 m.

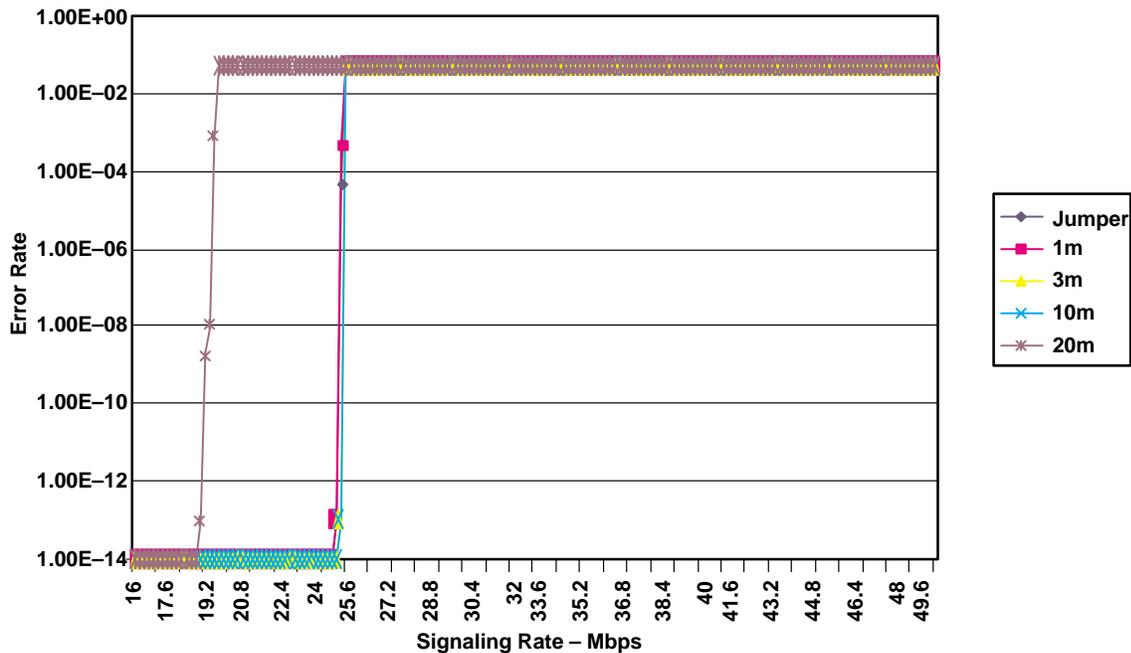


Figure A–11. BER vs Signaling Rate for Various Cable Lengths (M_Factor = 13)

Again, the data in Figure A–11 shows that performance using cable lengths up to 10 m has little impact on system signaling rate. At 20 m, the maximum rate has dropped to approximately 18 Mbps. BERT results using other M_Factors are presented in the following charts.

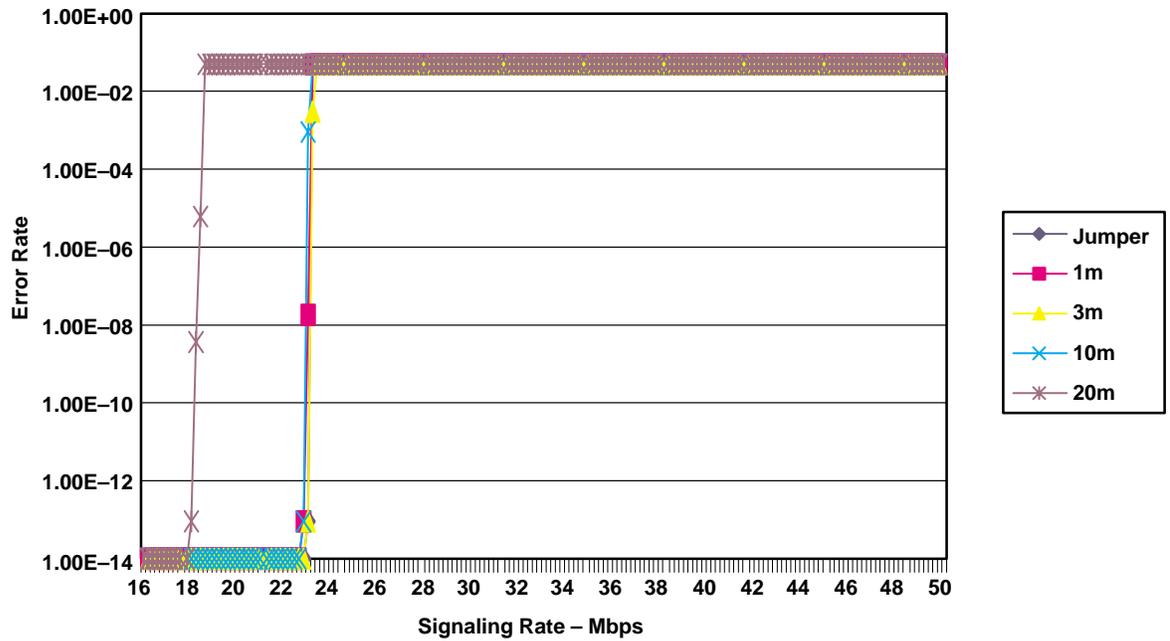


Figure A–12. BER vs Signaling Rate for Various Cable Lengths (M_Factor = 14)

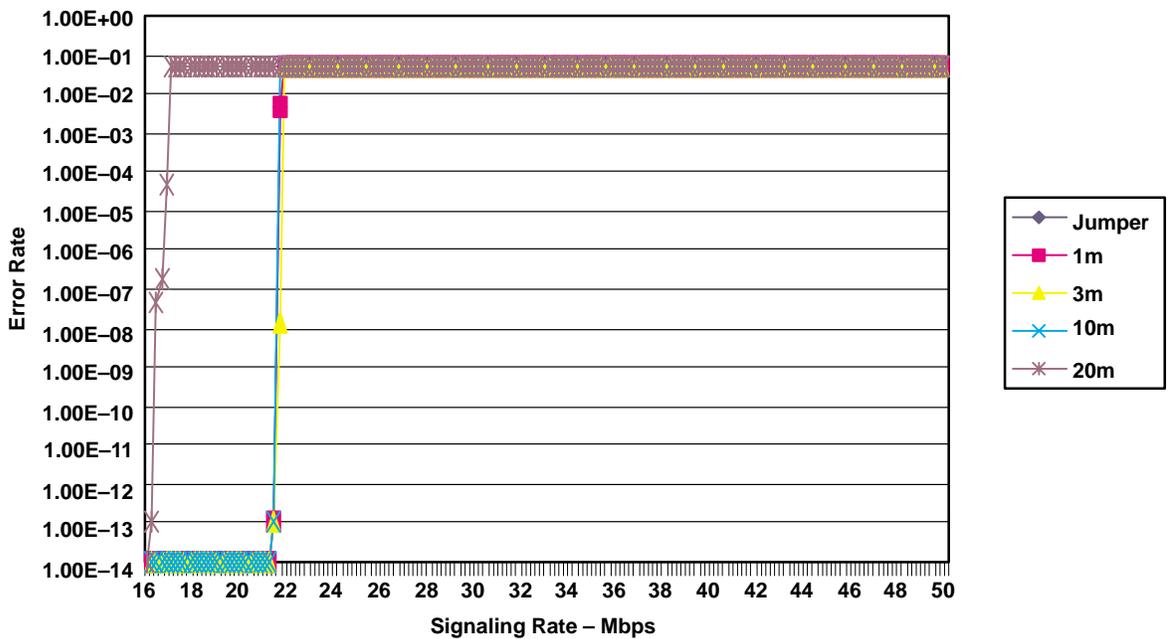


Figure A–13. BER vs Signaling Rate for Various Cable Lengths (M_Factor = 15)

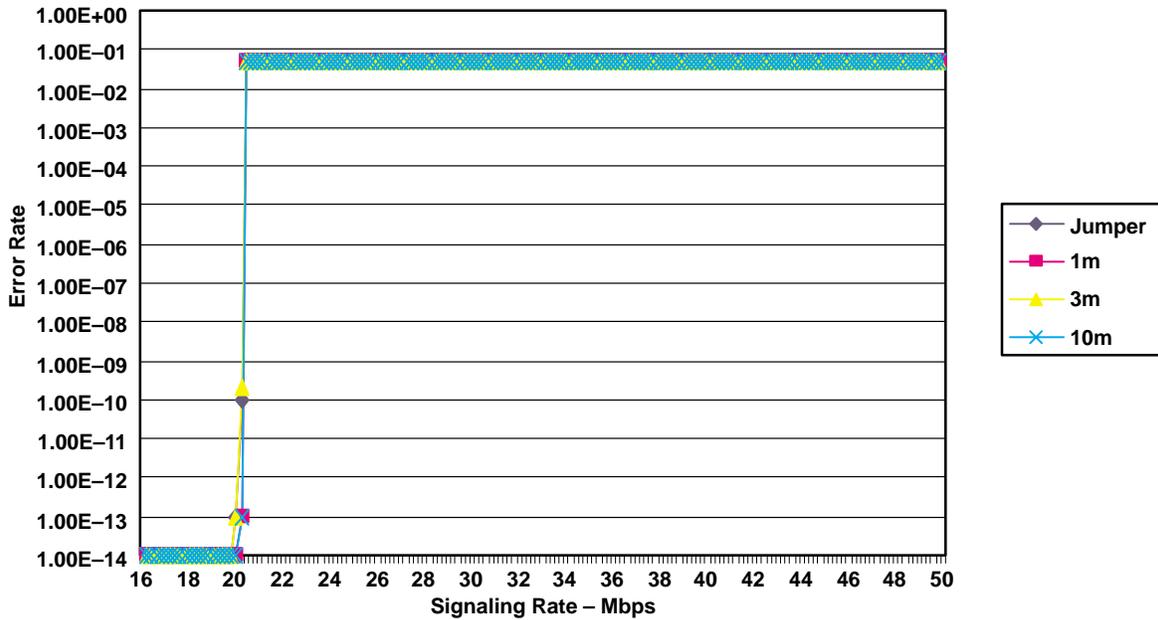


Figure A-14. BER vs Signaling Rate for Various Cable Lengths (M_Factor = 16)

When sending 16 bits (M_Factor = 16) and using the 20 m cable, the maximum signaling rate has dropped to below 16.092 Mbps and cannot be measured. Based on the results for M=14 and M=15 obtained earlier, it can be estimated that 20 m cable performance would be between 14 Mbps and 15 Mbps.

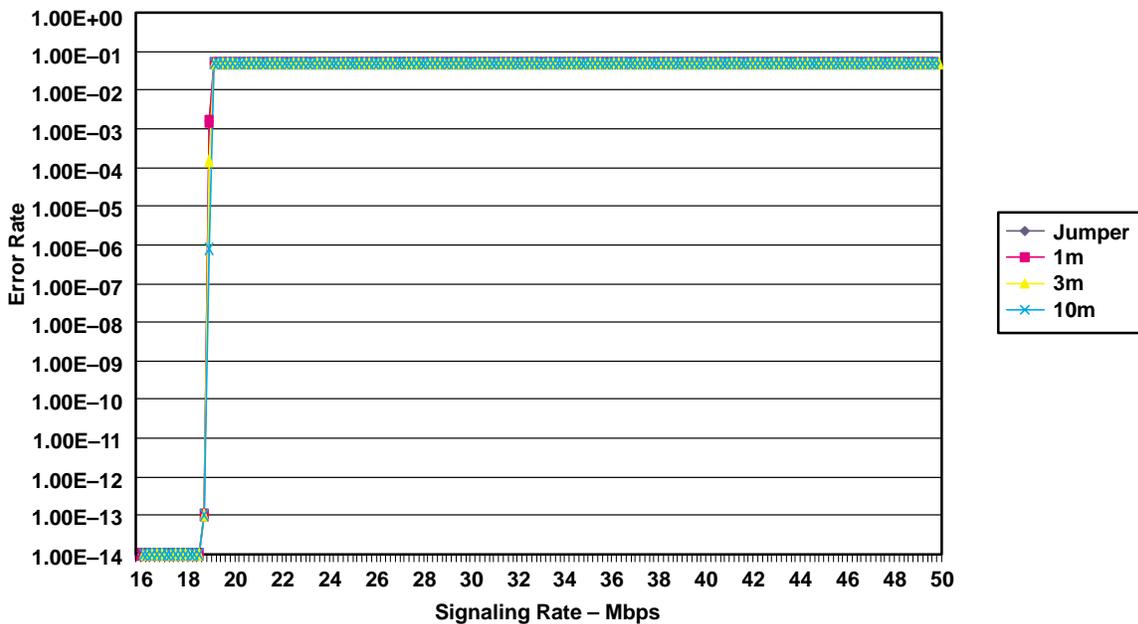


Figure A-15. BER vs Signaling Rate for Various Cable Lengths (M_Factor = 17)

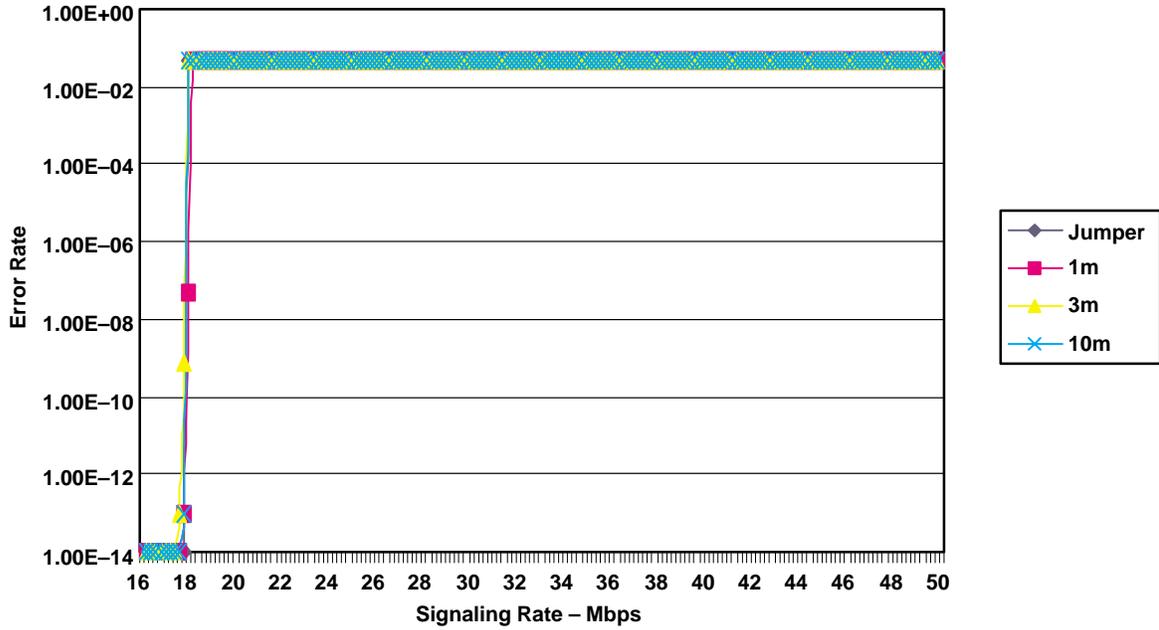


Figure A-16. BER vs Signaling Rate for Various Cable Lengths (M_Factor = 18)

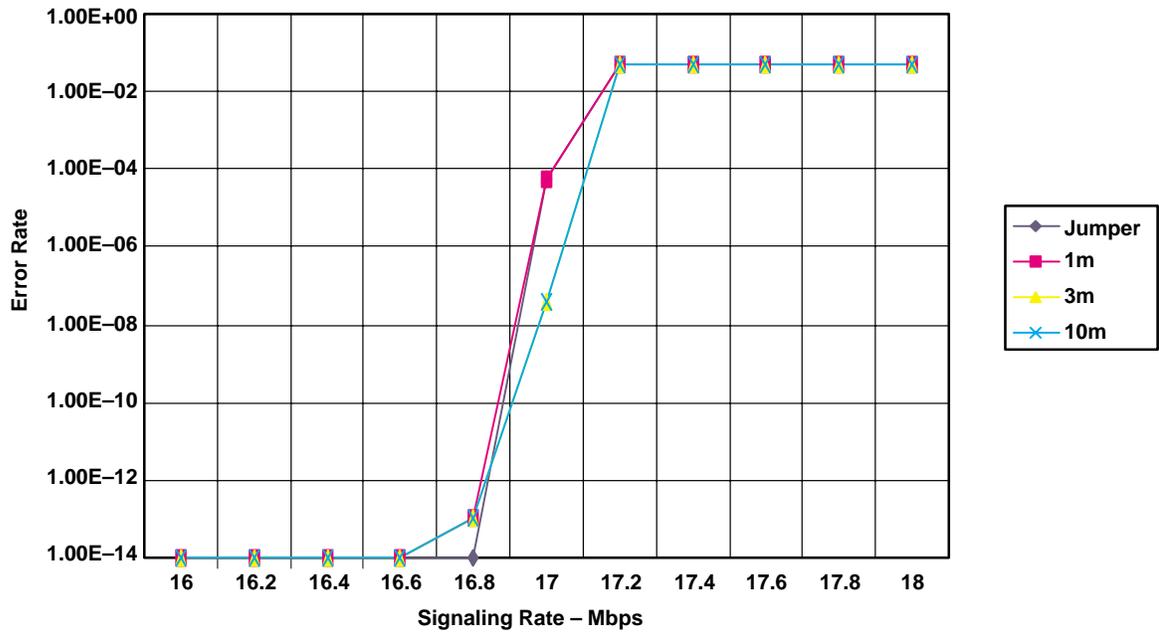


Figure A-17. Expanded BERT Results (M_Factor = 19)

One of the difficulties that occurred during measurements using the higher M_Factors, was that even small signaling rate changes, for example, 50 kHz, would have a large effect on BERT results. This was caused by the fact that the multiplier factor determines the signaling rate on the LVDS lines. For example, when using an M_Factor =8, a 100 Kbps increase in input data rate correlates to an increase of 800 Kbps on the serialized LVDS data lines between serializer and deserializer. When using an M_Factor of 20, this same 100 Kbps change correlates to a 2 Mbps change in the signaling rate on the LVDS lines. The net result is a loss of resolution at higher M_Factors. This means less data points could be taken, and measurement inaccuracy doubled in comparison to low multiplication factors (M_Factor = 10 or less).

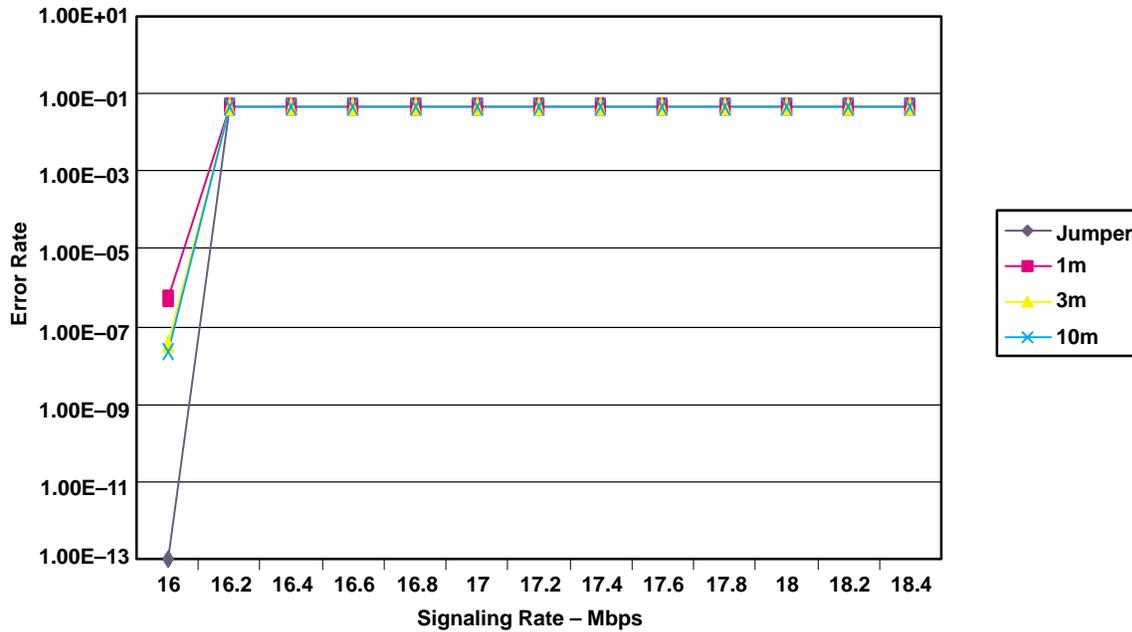


Figure A-18. Expanded BERT Results (M_Factor = 20)

The results with an M_Factor of 20 were right at the minimum input rate of the BERT. The resolution was insufficient to draw any conclusion. The results presented here are only the single-point BERT results that were obtained with the minimum input data rate of 16.092 Mbps applied to the serializer.

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