

SN65LVCP114 Guidelines for Skew Compensation

Communications Interface

ABSTRACT

Channel to channel skew in high speed data paths must be controlled to ensure robust system performance. Skew can arise from the integrated circuit, package or the circuit board. This application note provides information on channel to channel skew compensation of the SN65LVCP114.

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Introduction

Today's leading edge serial interconnect standards have some very demanding requirements on a copper link's ability to deliver usable output waveforms while achieving jitter, ISI, attenuation, reflection, crosstalk, and skew requirements. In the past, at lower data rates, circuit designers had the luxury of implementing channel links with large skew budgets; but with today's higher data transmission speeds much less time is available between clocking events and designers must take care to align data edges.

PCB Material Selection

Signal propagation delay depends, in part, on dielectric constant (£r) of the PCB material. A dielectric material can be assigned a dielectric constant that is related to the force of attraction between two opposite charges separated by a distance in a uniform medium. Each PCB substrate can have a different relative dielectric constant. The dielectric constant compares the effect of capacitance of a capacitor using that material as a dielectric, compared to a similar capacitor which has a vacuum as its dielectric. The dielectric constant affects the impedance of a transmission line. Also a signal will propagate faster in PCB designed with materials that have a lower dielectric constant.

FR-4 is the most widely used dielectric material in PCBs, and has a dielectric constant between 4.1 and 4.5. Table 1 shows the dielectric constant of a sample of materials.

Material	Dielectric Constant (Er)	Loss Tangent
DE156	4.0	0.02
GETEK	3.6	0.009
FR408HR	3.68	0.0092
IS680 3.33	3.33	0.003
IS680 2.8	2.8	0.0025

Table 1. Dielectric Constant and Loss Tangent Values for Different Materials¹

¹ www.isola-group.com



Transmission Line

Many different structures of trace routing are possible on a PCB; two common structures are show on Figure 1 and 2. A microstrip has one reference, often a ground plane, and these elements are separated by a dielectric. A stripline has two references, often multiple ground planes, and are surrounded with the dielectric.

Microstrip Transmission Line Layout

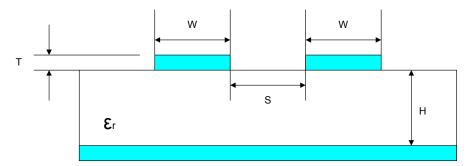


Figure 1. Microstrip Structure

Stripline Transmission Line Layout

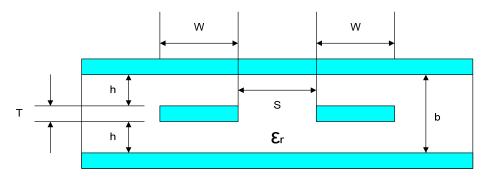


Figure 2. Stripline Structure



Propagation Delay

Propagation delay is the time required for a signal to travel from one point to another. Transmission line propagation delay is a function of the dielectric constant of the material.

Microstrip Propagation Delay Equation (ps/in):

$$t_{PD}$$
 (microstrip) = 85 $\sqrt{0.475\varepsilon_r + 0.67}$

Figure 3. Microstrip Propagation Delay Equation

Stripline Propagation Delay Equation (ps/in):

$$t_{PD}$$
 (stripline) = 85 $\sqrt{\varepsilon_r}$

Figure 4. Stripline Propagation Delay Equation

SN65LVCP114 Inter-Pair Skew

Inter-pair skew is the difference between the fastest and slowest pairs in the link. Its control becomes critical when a link uses a separate clock line (e.g. non-PLL based devices) which must be synchronized accurately in relation to the data lines to correctly sample the data. Serial links have clocks embedded with the data stream and thus do not have tight restrictions on Inter-pair skew.

In order to optimize the overall package size, the SN65LVCP114 package substrate signal trace lengths are not matched, refer to Table 1. To ensure timing alignment for all channels per port, both the substrate trace length plus the PCB trace length for each signal must be matched to meet the trace length skew tolerance for all signals within the clock domain.



Channel	Skew (ps)
AIN0	49.6
AIN1	34.8
AIN2	4.7
AIN3	0.0
BIN0	0.0
BIN1	16.3
BIN2	29.2
BIN3	40.7
CIN0	0.0
CIN1	2.8
CIN2	6.4
CIN3	3.7
AOUT0	23.9
AOUT1	10.5
AOUT2	17.4
AOUT3	0.0
BOUT0	0.0
BOUT1	4.8
BOUT2	18.5
BOUT3	15.4
221172	
COUT0	3.4
COUT1	11.8
COUT2	9.2
COUT3	0.0

Table 2. SN65LVCP114 Expected Channel Skew per Port

A procedure for optimizing inter-pair skew for SN65LVCP114 is provided below.

- 1. Route signals following proper high speed layout techniques.
- 2. Match all high speed trace length channels per port.
- 3. Use microstrip or stripline equations, Figures 3 or 4 respectively, to calculate the trace length deltas based on Table 2.
 - a. Table 3, below, shows an example using the microstrip equations and an effective dielectric constant of 3.66 to calculate the trace lengths.
- 4. Calculate the compensated trace length by adding the matched trace length from step 2 with the trace length deltas calculated in step 3.
 - a. Table 4 shows an example for output port C using microstrip, effective dielectric constant of 3.66, and an original trace length match (step 2) of 4,000mils.



Microstrip Recommended Trace Delay Addition					
Channel	Skew (ps)	Inches	Millimeters	Mils	Microns
AIN0	49.6	0.376	9.550	376.001	9550.435
AIN1	34.8	0.264	6.701	263.807	6700.708
AIN2	4.7	0.036	0.905	35.629	904.981
AIN3	0.0	0.000	0.000	0.000	0.000
BULLO			2 2 2 2		
BIN0	0.0	0.000	0.000	0.000	0.000
BIN1	16.3	0.124	3.139	123.565	3138.550
BIN2	29.2	0.221	5.622	221.356	5622.433
BIN3	40.7	0.309	7.837	308.533	7836.748
CIN0	0.0	0.000	0.000	0.000	0.000

CIN1	2.8	0.021	0.539	21.226	539.137
CIN2	6.4	0.049	1.232	48.516	1232.314
CIN3	3.7	0.028	0.712	28.048	712.432
AOUT0	23.9	0.181	4.602	181.178	4601.923
AOUT1	10.5	0.080	2.022	79.597	2021.765
AOUT2	17.4	0.132	3.350	131.904	3350.354
AOUT3	0.0	0.000	0.000	0.000	0.000
DO1170			2.222		
BOUT0	0.0	0.000	0.000	0.000	0.000
BOUT1	4.8	0.036	0.924	36.387	924.236
BOUT2	18.5	0.140	3.562	140.242	3562.158
BOUT3	15.4	0.117	2.965	116.742	2965.256
COUTO	3.4	0.026	0.655	25.774	654.667
COUT1	11.8	0.089	2.272	89.452	2272.079
COUT2	9.2	0.070	1.771	69.742	1771.452
COUT3	0.0	0.000	0.000	0.000	0.000

Table 3. SN65LVCP114 Skew Compensation Example (Er = 3.66)

Channel	Skew (ps)	Skew (Mils)	Trace Length (Mils)	Compensated Trace Length (Mils)
COUT0	3.4	25.774	4000	4025.77
COUT1	11.8	89.452	4000	4089.45
COUT2	9.2	69.742	4000	4069.74
COUT3	0.0	0.000	4000	4000.00

Table 4. SN65LVCP114 Skew Compensation Example (Er = 3.66)



Summary

This application note provides guidance for inter-pair skew compensation of the SN65LVCP114 channels when used with a non-PLL based device.

For any concerns, a question can be submitted in the TI E2E Community forum (e2e.ti.com) under the High Speed Interface section in the Interface forum.

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