

# **DRV592 H-Bridge Evaluation Module**

## User's Guide

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#### **EVM WARNINGS AND RESTRICTIONS**

It is important to operate this EVM within the supply voltage range of 2.8 V to 5.5 V.

Exceeding the specified supply range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the supply range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 125°C. The EVM is designed to operate properly with certain components above 125°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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### **Preface**

#### How to Use This Manual

This document contains the following chapters:

Chapter 1—Introduction
Chapter 2—Operating Instructions

Related Documentation From Texas Instruments
DRV592 data sheet (literature number SLOS390).

#### **FCC Warning**

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

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## **Chapter 1**

## Introduction

This chapter provides an overview of the Texas Instruments (TI) DRV592VFP high-efficiency H-Bridge evaluation module. It includes a list of EVM features, a brief illustrated description of the module, and a list of EVM specifications.

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1.1	Feature Highlights1-2
1.2	Description
1.3	EVM Specifications

#### 1.1 Feature Highlights

The	The DRV592VFP evaluation module includes the following features:			
	User-defined operation with full output filter			
	High efficiency			
	Small solution size			
	Low supply current in active and shutdown modes			
	LEDs and test points for fault monitoring			
	Jumpers for selecting device options			
	Easy connections for inputs, outputs, and power supply			

#### 1.2 Description

The DRV592VFP H-Bridge evaluation module is a complete power stage solution. It consists of the TI DRV592VFP H-Bridge IC along with a few discrete passive components required for operation. It also includes jumpers for configuring the features of the device, LEDs and test points for fault monitoring, and a full output filter that may be easily modified. The 5-way jacks for the inputs, outputs, and power supply provide for ease of connection to any system, from an existing design to a bread-boarded prototype.

#### 1.3 EVM Specifications

Supply voltage range, V <sub>DD</sub>	2.8 V to 5.5 V
Supply current, I <sub>DD</sub>	3.1 A max

1-2 Introduction

## Chapter 2

## **Operating Instructions**

Follow the steps in this chapter to quickly prepare the DRV592VFP EVM for use.

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2.1	Precautions
2.2	Operating Instructions List

#### 2.1 Precautions

**Power Supply Input Polarity and Maximum Voltage** 

Always ensure that the polarity and voltage of the external power connected  $V_{DD}$  power input connector J8 is correct. Overvoltage or reverse-polarity power applied to this terminal can damage the evaluation module.

#### 2.2 Operating Instructions List

Figure 2–1. Top View

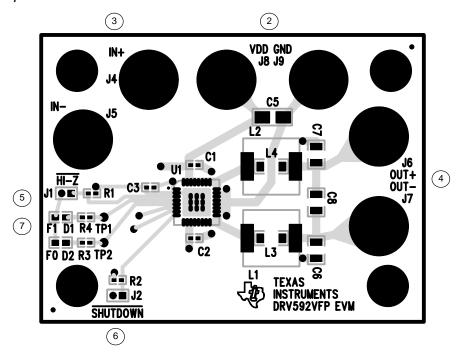


Table 2-1. Typical Jumper Settings

J1 (HI-Z)	J2 (SHUTDOWN)		
ON	ON		

#### Power supply

- 1) Ensure that all external power sources are set to OFF.
- Connect a 2.8-V to 5.5-V power supply to J8 (V<sub>DD</sub>) and J9 (GND), taking care to observe proper polarity.

#### Inputs and outputs

 Connect a TTL-compatible PWM signal to J4 (IN+) and/or J5 (IN-). The IN+ terminal controls the OUT+ voltage while the IN- terminal controls the OUT- voltage.

The input frequency range may be from 0 Hz (dc) to 1 MHz.

4) Connect a load across J6 (OUT+) and J7 (OUT-). The polarity of the connection depends on the operation of the input signal. As the duty cycle at IN+ becomes greater than the duty cycle at IN-, the voltage at OUT+ increases, causing current to flow from OUT+ to OUT-. Similarly, as the duty cycle at IN+ decreases lower than IN-, the voltage at OUT-increases, causing current to flow from OUT- to OUT+.

For example, consider the load to be a TEC element and the PWM input signal to be the output of a temperature control circuit. In this example, as temperature increases the output duty cycle of the temperature control circuit increases. The TEC element must therefore be connected with the anode at OUT+ and the cathode at OUT- to ensure that the TEC element cools when the temperature increases.

#### ■ Evaluation module jumpers, LEDs, and test points

5) Jumper J1 (HI-Z) should be ON for normal operation.

When J1 is ON, the device operates normally. When J1 is off, the outputs are turned off and become high impedance (2  $k\Omega$ ) nodes.

6) Jumper J2 (SHUTDOWN) must be ON for normal operation. (Remove J2 to place the DRV592VFP in shutdown mode.)

If an external shutdown control signal is to be used, it must be connected to the right-hand pin of J2 (which is connected to resistor R2). The control signal must be TTL-compatible; a logic high provides normal operation, a logic low places the DRV592VFP in shutdown.

7) The LED D1 lights if FAULT1 (labeled F1 on the EVM) is active and LED D2 lights if FAULT0 (labeled F0 on the EVM) is active. If external fault monitoring is to be used, test point TP1 is connected to FAULT1 and test point TP2 is connected to FAULT0. The pins and test points go low when a fault is present, lighting the LEDs. The faults are shown in the table below. Refer to the DRV592 data sheet (SLOS390) for additional information on the fault indicators.

Table 2-2. Fault Indicators

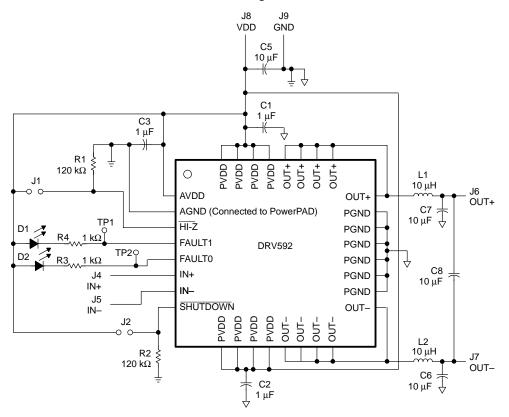
FAULT1	FAULT0	
0 0 Overcurrent		Overcurrent
0	1	Undervoltage
1	0	Overtemperature
1	1	Normal operation

#### ☐ Power up

8) Verify correct voltage, input polarity, and set the external power supply to ON. The EVM begins operation.

#### 2.2.1 DRV592VFP EVM Schematic

Figure 2–2. DRV592VFP EVM Schematic Diagram



#### 2.2.2 DRV592VFP EVM Bill of Materials

Table 2-3. DRV592VFP EVM Bill of Materials

Reference	Description	Size	Qty.	MFG	Part #	Vendor/#
C1-C3	Capacitor, ceramic, 1 μF, ±10%, X5R, 6.3 V	0603	3	Panasonic	ECJ1VB0J105K	Digi-Key/ PCC1915CT-ND
C5-C8	Capacitor, ceramic, 10 μF, ±10%, X5R, 16 V	1210	4	Panasonic	ECJ-4YB1C106K	Digi-Key/ PCC2169CT-ND
R1, R2	Resistor, chip, 120 k $\Omega$ , 1/16 W, 1%	0603	2	Phycomp	9C06031A1203F KHFT	Digi-Key/ 311-120KHCT-ND
R3, R4	Resistor, chip, 1 kΩ, 1/16 W, 1%	0603	2	Phycomp	9C06031A1001F KHFT	Digi-Key/ 311-1.00KHCT-ND
D1, D2	LED, red, 2 V, 140° view angle	0805	2	Lumex	SML-LXT0805IW	Digi-Key/ 67–1552–2–ND
L1, L2	Inductor, SMT, 10 $\mu$ H, 0.026 m $\Omega$ DCR (typical), 4.4 A max dc current		2	Sumida	CDRH104R-100	Harvey King/ CDRH104R-100
L3, L4	Chip bead (not assembled)	1806	2			
J1, J2	Header, 2 position	2 mm	2	Norcomp	2163-2-01-P2	Digi-Key/ 2163S-02-ND
	Shunts	2 mm	3	3M	953170-00	Digi-Key/ 953170-00
TP1, TP2	Test points		2			Farnell/240-333
IN-, IN+, V <sub>DD</sub> , GND, OUT+, OUT- (J4-J9)	Uninsulated binding post with knurled thumb, nut-grounded type		6	Johnson Components	111-2223-001	Digi-Key/J587-ND
	Standoffs	4–40	4			Digi-Key/534-1804
U1	DRV592, 32-pin quad flatpack		1	TI	DRV592VFP	TI/DRV592VFP

#### 2.2.3 DRV592VFP EVM PCB Layers

Figure 2–3. Top Layer

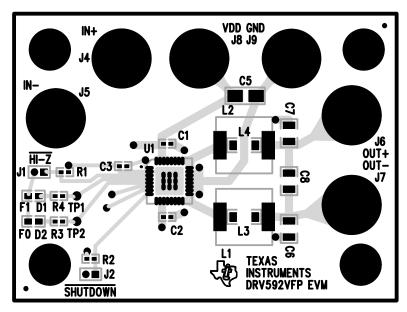


Figure 2-4. Bottom Layer

