Application Report
SLUA245 - July 2000

Synchronizing a PFC Controller from a Downstream Converter's Gate Drive

Michael O'Loughlin *Power Supply Control Products*

ABSTRACT

Due to pending line harmonic requirements at higher power levels, power factor correction (PFC) is required in some ac-to-dc off-line power converter applications. This type of power converter can be designed with two cascaded power stages similar to the configuration in Figure 1. The first stage is a boost converter that converts the ac voltage to dc voltage with PFC. The output voltage of the boost stage might be as high as 385 V to meet the universal line requirements of 85 V_{RMS} to 265 V_{RMS}. The second power stage is a forward converter that steps down the boost voltage. These designs often require two PWM controllers, one for each power stage. In some cases it is beneficial to synchronize the PFC controller with the step down converter's controller, for example, when the UCC3817 is properly synchronized with the down stream converter, it reduces the ripple current up to 40% through the boost capacitor[1]. Some of these controllers do not provide the internal circuitry to synchronize the oscillator. Most of the controllers, however, do provide access to the oscillator ramp, which can be synchronized with external circuitry. The purpose of this application report is to describe how to synchronize a PFC controller's oscillator in similar power systems to Figure 1 using the down stream converters gate drive.

Contents

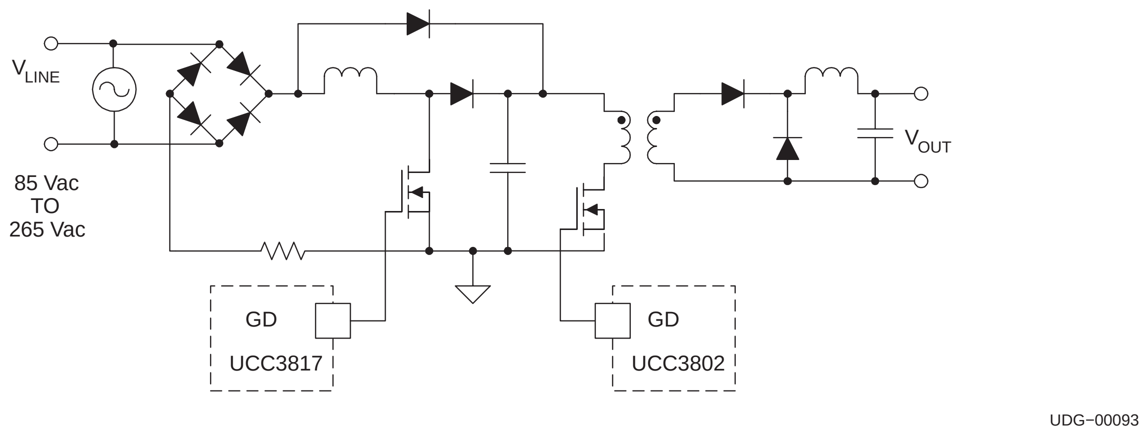

Figure 1. Two-Stage Power System

1 Internal Oscillator of a PFC or PWM Control Integrated Circuit

In order to synchronize the PFC controller's oscillator properly, it is necessary to have a basic understanding of the internal circuitry that creates the oscillator's saw-tooth waveform. Generally PWM and PFC controllers generate the oscillator's waveform through a current source to charge an external timing capacitor (CT) and a hysteretic comparator that controls the charging and discharging of the timing capacitor. It is this internal comparator that monitors the ramp voltage, which can be used to synchronize the oscillator. Figure 2A shows a functional schematic of the PFC controller's internal oscillator.

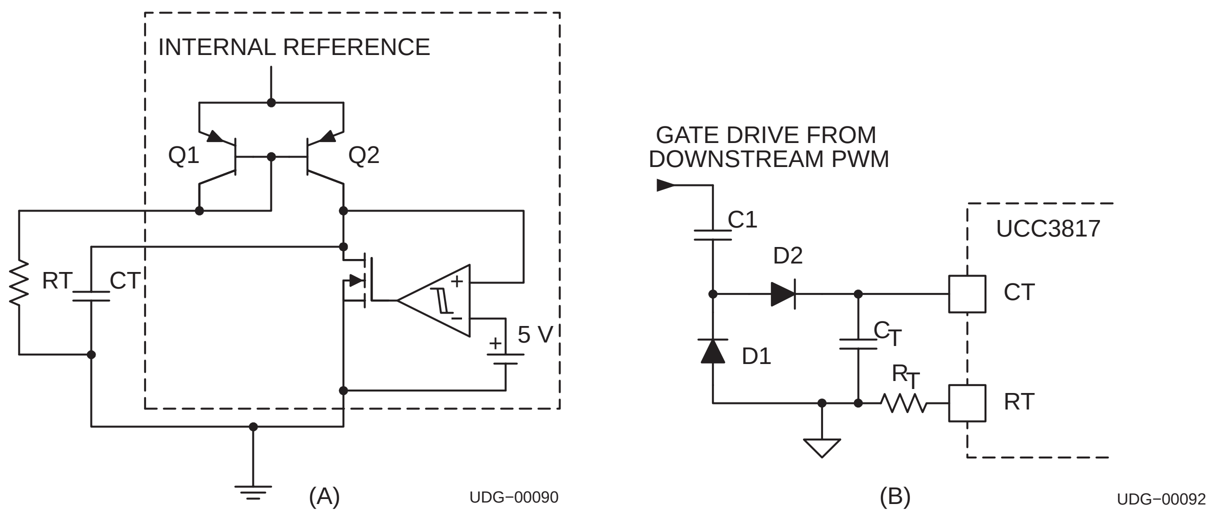

Figure 2. Internal Oscillator for a PFC Controller (A) and Synchronization Circuitry (B)

2 Synchronization Circuit

Synchronization of the PFC controller's oscillator with the downstream converter's oscillator in a two-stage power system can be accomplished with three external components. These components consist of two diodes and one capacitor. Figure 2B shows a schematic of the synchronization circuitry. Note that the downstream converter must use a traditional trailing-edge PWM to ensure proper synchronization. A description of leading edge PWM can be found in the UCC3817 data sheet[1].

3 Theory of Operation

The gate drive of the downstream converter provides the clock signal to synchronize the PFC's oscillator. Components C1, C_T, and diode D2 form a voltage divider that adds a synchronization pulse to the oscillator ramp when the gate drive of the downstream converter transitions from low to high. The added voltage pulse trips the internal comparator signaling the oscillator's circuitry to discharge C_T. When the gate drive transitions from high to low, the gate discharges C1 through the gate drive and diode D1 resetting the circuit. Diode D2 blocks the discharge current of C1 to ensure a clean oscillator saw-tooth waveform during circuit reset. For more detailed information on how this synchronization circuit works, see the gate drive and oscillator waveforms in Figure 3 and the synchronization circuitry of Figure 2B. At time t0, the gate drive transitions from low to high causing a voltage pulse to be added to the oscillator's ramp through the voltage divider created by C1, C_T, and D2. At time t1, the internal peak comparator is tripped, discharging C_T. The timing capacitor continues to discharge until the oscillators valley is reached at time t2 where the oscillator's comparator turns off allowing the timing capacitor to begin charging for the next ramp cycle. The synchronization circuit is reset at time t3 where C1 is discharged through the gate drive and diode D1.

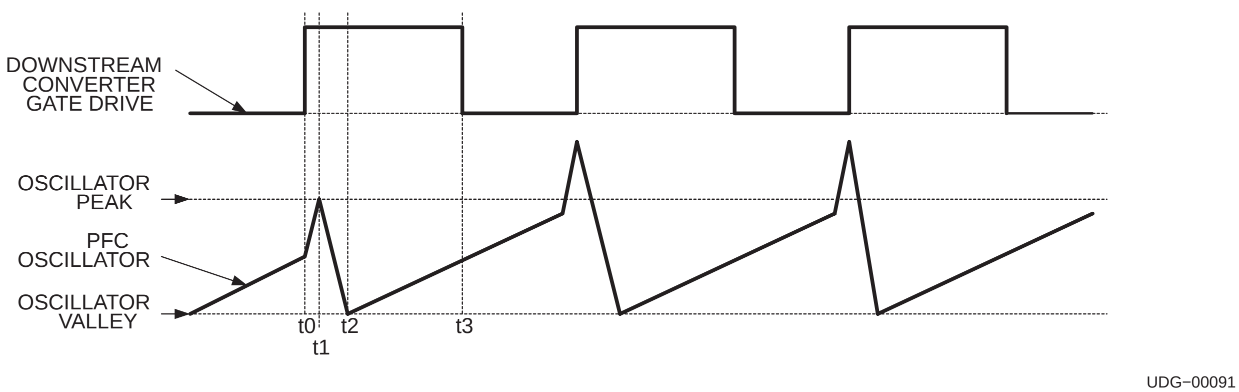

Figure 3. Timing Waveforms

4 Design Example

In this design example, the UCC3817 power factor controller was designed to be synchronized from the gate drive of a UCC3802 controller. These devices could be used for a two-stage power system similar to the one represented in Figure 1. For proper synchronization, it is important to select the UCC3817 timing components to set up the oscillator to run at a frequency that is 20−30% less than the UCC3802's oscillator. The timing components for R_T and C_T were selected for the oscillator of the UCC3802 to be operating at 100 kHz. The UCC3817 components were selected for an oscillator frequency of 80 kHz. The UCC3817 data sheet lists the following equation to select the timing components for the controller's oscillator[1]. An 820-pF capacitor was selected for C_T, requiring a resistor of roughly 11 kΩ for R_T.

$$f = \frac{0.6}{R_T \times C_T} \tag{1}$$

To select the proper components for the synchronization circuit it is important to know how accurate the UCC3817's oscillator frequency is and how much the peak voltage and amplitude of the ramp will vary. The data sheet for the UCC3817[1] specifies the oscillator frequency at 100 kHz can vary ±15%. The oscillator's frequency in this example could be running at a frequency anywhere between 68 kHz and 92 kHz. The data sheet states that the PFC controller's oscillator peak voltage can vary from 4.5 V to 5.5 V, while the ramp amplitude can vary from 3.5 V to 4.5 V. The following equation is used to estimate the magnitude of the voltage pulse required for synchronization, where variable $V_{MAX\_RAMP\_PEAK}$ represents the maximum oscillator ramp peak voltage and V_{VALLEY} represents the ramp's valley voltage. The ramp valley voltage for the PFC controller is roughly 1 V. $V_{MIN\_RAMP\_AMP}$ represents the minimum oscillator ramp amplitude. Variable f_{SYNC} is the desired synchronization frequency generated from the UCC3802 controller's gate drive. Variable f_{MIN_OSC} represents the minimum oscillator frequency of the PFC controller, which for this design is roughly 68 kHz. The calculation estimated that V_{PULSE} needs to be roughly 2.2 V for this design.

$$V_{PULSE} = V_{MAX\_RAMP\_PEAK} - \left[\frac{V_{MIN\_RAMP\_AMP} \times f_{MIN\_OSC}}{f_{SYNC}} + V_{VALLEY}\right] \tag{2}$$

Once the voltage pulse has been estimated and the diodes used for synchronization have been selected, the following equation is used to estimate the required capacitance needed for C1. The diodes used in this circuit are Fairchild 1N914 and were selected for their low capacitance of 4 pF. For this design 25-V ceramic capacitors with a tolerance of ±10% were used. In the calculation for C1, the variable V_{D2} is the forward voltage drop of the diodes selected. The 1N914 has a forward voltage drop of approximately 0.7 V. It is important to know the maximum gate drive voltage to properly set the voltage divider. The maximum gate drive voltage is represented by ($V_{VCC3802}$–V_{SAT}). $V_{VCC3802}$ is the variable for the UCC3802 supply voltage and for this design was set to 10 V. V_{SAT} is the saturation voltage of the UCC3802 gate drive, the data sheet states that this parameter is approximately 0.4 V maximum at 20 mA of load current[2]. The capacitance required for C1 was roughly 330 pF.

$$C1 = \frac{V_{PULSE} \times C_T}{\left(V_{VCC3802} - V_{SAT} - V_{D2} - V_{PULSE}\right)} \tag{3}$$

The waveform in Figure 4 shows the oscillator saw-tooth waveform of the UCC3817 with a R_T of 11 kΩ and a C_T of 820 pF without synchronization. The oscillator was designed for a frequency of 80 kHz ±15%. The waveform shows the oscillator operating within the design goal at approximately 70 kHz.

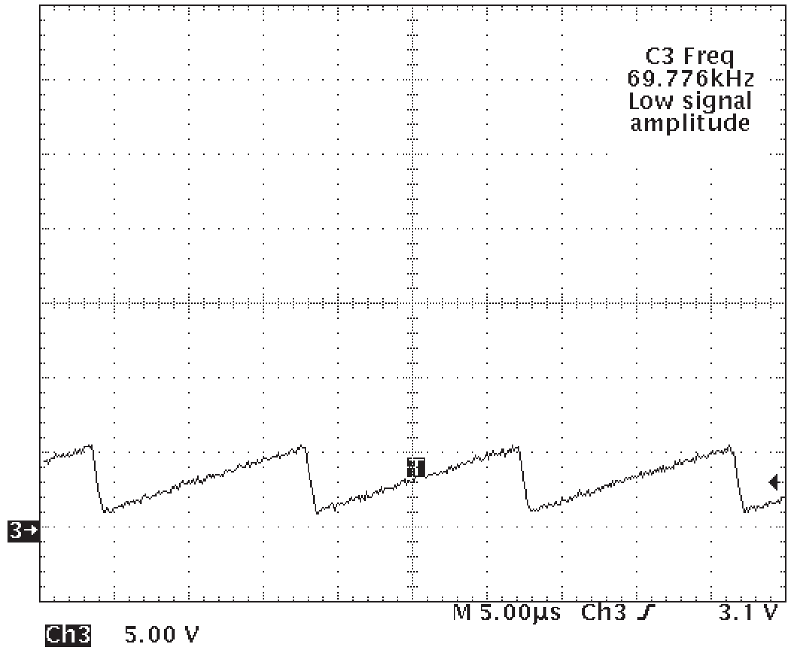

Figure 4. UCC3817 Oscillator Waveform Without Synchronization

Figure 5 shows the gate drive and oscillator waveforms of the UCC3802 and the oscillator waveform of the UCC3817 when properly synchronized with the circuit presented in Figure 2B. Channel 1 is the gate drive waveform and Channel 2 is the oscillator waveform from the UCC3802 and Channel 3 is the oscillator waveform from the UCC3817. The waveform shows the UCC3817's oscillator synchronized to the UCC3802's oscillator at a frequency of approximately100 kHz.

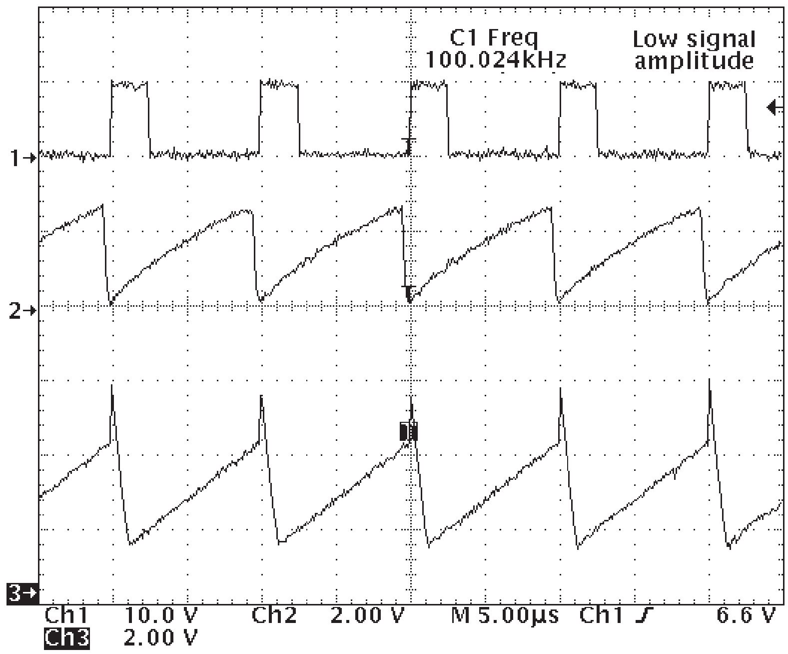

Figure 5. UCC3802 Oscillator Waveform with Synchronization

References

1. UCC3817 *BiCMOS Power Factor Preregulator*, Texas Instruments, Literature No. SLUS395
2. UCC3802 *Low-Power BiCMOS Current-Mode PWM*, Texas Instruments, Literature No. SLUS270

Acknowledgements

The author would like to thank John Bottrill for his contributions to this work.

IMPORTANT NOTICE

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265