



UCC5672 SCSI Low Voltage Differential Multimode (LVD)/ Multimode Single-Ended (MSE) Evaluation Board and List of Materials

User's Guide

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SCSI Interface Products

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1 Introduction

The UCC5672 is a high-performance 9-line LVD/MSE terminator designed to provide the lowest possible capacitance and the lowest possible temperature drift. It is designed for 3.3 volt, or 5 volt systems and operates over the range of 2.7 V to 5.25 V.

The evaluation board should be used at the end of the cable, or as a plug terminator at the end of the cable. Active terminators should be used at both ends of the cable. Generally, demo cards are used between the controller, the cable and at the last device. If they are used as a plug terminator, the second connector becomes a stub affecting the capacitance load on the bus. Termination can be disabled on the demo card allowing the evaluation board to be part of the bus path.

The evaluation board can be used to test the Unitrode/TI terminator versus drive or controller termination. The demo board demonstrates how the Unitrode/TI termination can assist in solving bus problems.

The evaluation board layout shows the UCC5672 9-line LVD SCSI termination with a separate disconnect for the high byte data (Switch 2). The low byte data control is controlled from (Switch 1). Termination must be disabled on all devices except the devices at each end of the cable.

The 9-line terminators automatically detect the bus mode by placing 1.3 V on the differential sense line, then monitoring the differential sense line through an RC filter, (R1) and (C5) provides noise filtering. The internal digital delay of 100 ms to 400 ms delays the switching of the terminator to meet the SPI-3 specification. If the differential sense line is below 0.5 V, the terminator senses single-ended operation (SE) and switches to single-ended termination. If the differential sense line is between 0.7 V and 1.9 V, the terminators are in LVD mode. If the differential sense line is above 2.4 V, the terminator is in the disconnected high-impedance mode. The demo board can not be used in a high-voltage differential (HVD) system.

The connector pinout is defined in SPI-2, SPI-3 and SPI-4.

The layout of the evaluation board is an example of how to match the length and loading of the lines. Every line has a feedthrough connection to the terminator, the surface mount connector requires a feedthrough on one side of every line. This is not as critical on this two-sided board since there is no inner layer capacitance on the feedthroughs. With a multilayer board, one extra feedthrough is more capacitance imbalance than allowed. The clearance holes on the inner layers are enlarged to compensate.

The key indicators of signal integrity are the rising and falling edges of the signals. The REQ and ACK signals are the highest speed signals. Ultra3/Ultra160 reflections can be 4 or more bit times from the switch point.

LVD signals must transition at least 60 mV beyond the zero crossing, some receivers require at least 1/4 the signal in the opposite polarity to switch at high speeds (see the SPI-3 and SPI-4 receiver masks). If the signals do not reach the correct amplitude, check the system impedance. It should be above 85-Ω differential when all the devices are installed on the bus.

Reflections can be isolated by the reflection time. Signal round-trip time is normally 10 nanoseconds per meter on cables with standard PVC insulation. Reflections from older devices or bad cables can cause major problems, older designs paid little attention to capacitance and balancing stub lengths. Long stubs and capacitance cause reflection problems. With the introduction of the Ultra160, the SCSI bus needs to be treated like parallel transmission lines. The lines must be matched in length and circuit capacitance.

2 Features

The UCC5672-EVM SCSI evaluation module includes:

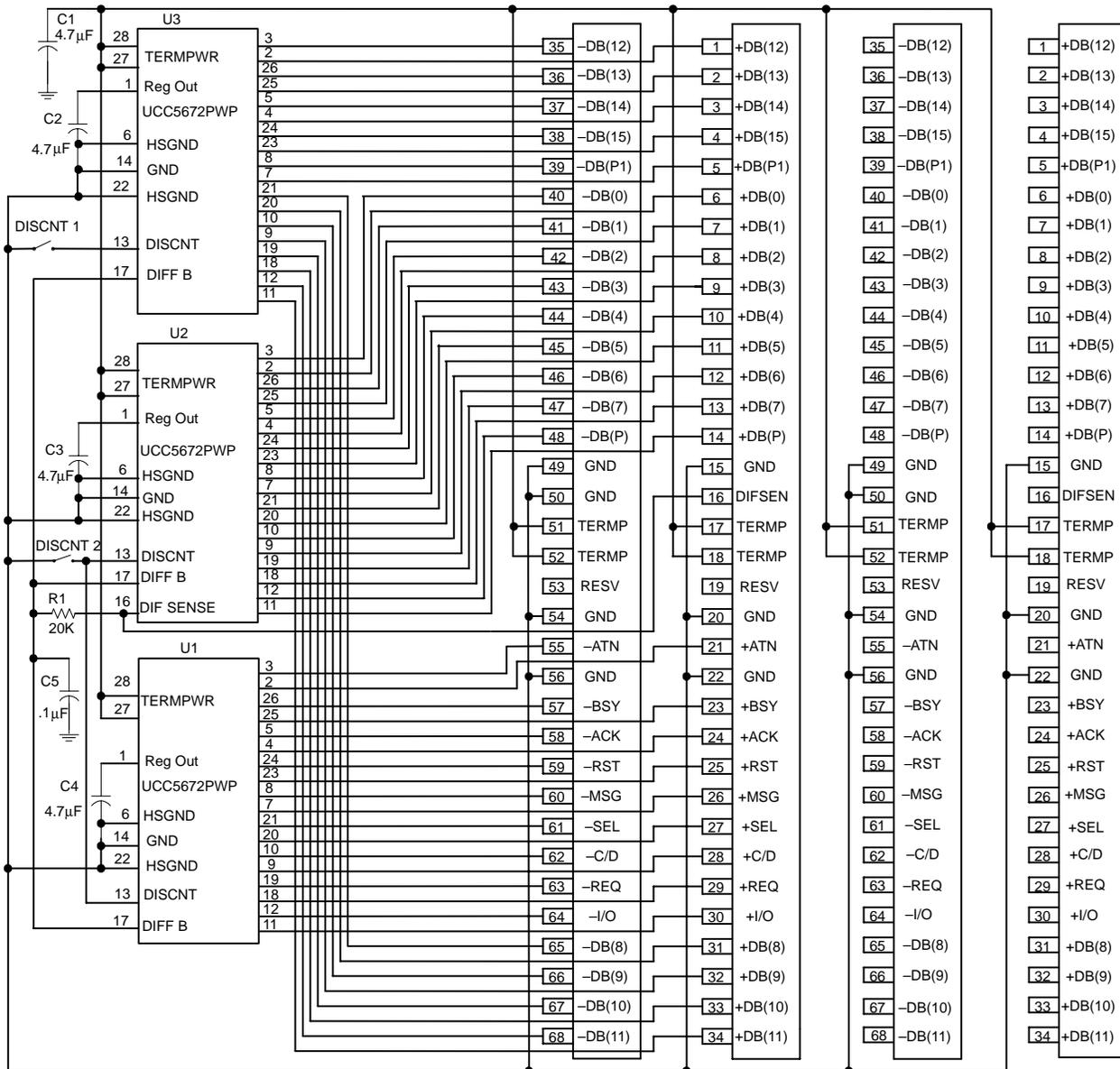
- Auto selection multimode single-ended or low-voltage differential termination
- 2.7 V to 5.25 V operation
- Differential failsafe bias
- Built-in SPI-3 mode change filter/ delay
- Meets SPI, SPI-2(Ultra2), SPI-3(Ultra3/Ultra160) and SPI-4(Ultra320) standards
- Supports active negation
- 3 pF channel capacitance

3 Description

The UCC5672 low-voltage differential (LVD) and multimode single-ended (MSE) terminator is both a single-ended terminator and a low-voltage differential terminator. The low-voltage differential is a requirement for the higher speeds and is the only way to have adequate skew budgets.

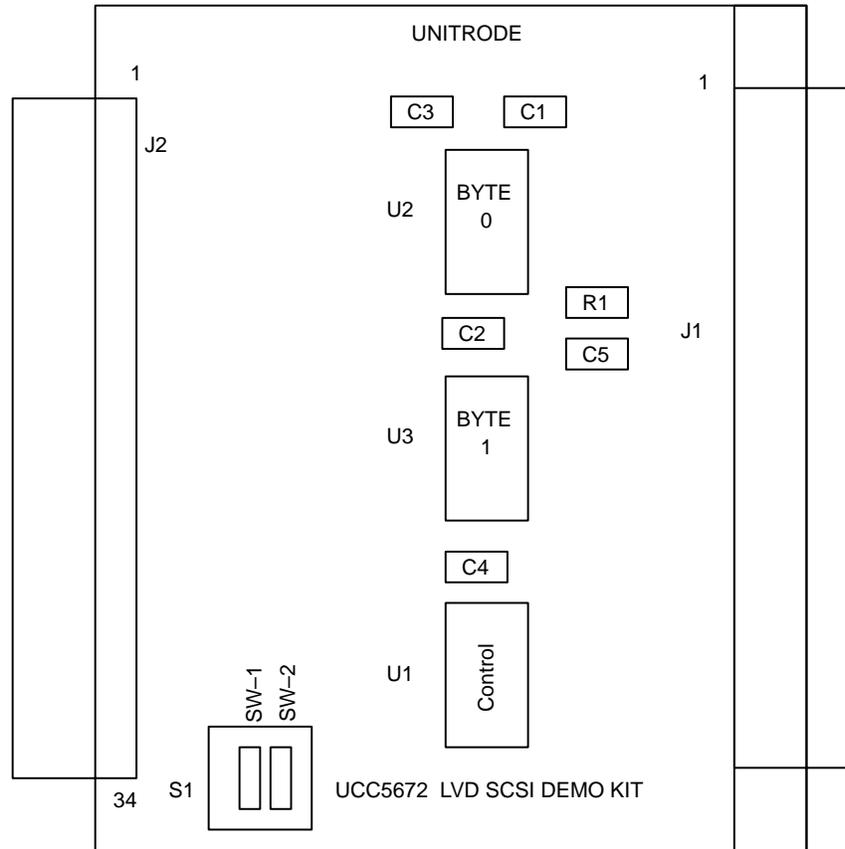
The automatic mode select feature switches the terminator between single-ended MSE or LVD SCSI termination, depending on the devices attached. If the bus is in high-voltage differential mode, the terminator lines transition into a high-impedance state.

The UCC5672 is SPI-4, SPI-3, SPI-2, and SPI compliant. This device is offered in a 28-pin TSSOP package to minimize the footprint. The UCC5672 is also available in a 36-pin MWP package.



NOTE: Enlarge the ground area and use all heat sink pins to conduct heat away from the UCC5672.

Figure 1. Evaluation Module Schematic



UDG-98152

Figure 2. UCC5672 Evaluation Board Layout

4 Parts List

Table 1. UCC5672 Bill of Materials

REFERENCE	QTY	DESCRIPTION	MANUFACTURER	PART NUMBER
U1, U2, U3	3	IC, SCSI Multimode LVD/SE 9 Line Terminator	Unitrode/TI	UCC5519PWP
R1	1	Resistor, 1/8W SMT 1206 1%	Panasonic	ERJ-8ENF-2002V
C5	1	Capacitor, 0.1 μ F 50 V X7R 1206 10%	Panasonic	ECU-V1H104KBW
C1, C2, C3, C4	4	Capacitor, 4.7 μ F 10 V A Case 10%	Panasonic	ECS-T1AY475R (TE Series)
J2	1	Connector, 68 Pin Straddle Mount	Honda (Male)	PCS-XE68MTCGI
J1	1	Connector, 68 Pin Right Angle Receptical Header	AMP (Female)	787394-7 (Amplimite-SCSI-2)
S1	1	Switch, DIP Low Profile SMT(SPST)	C&K	SD02HOSK Tape Sealed (SD Series)

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