

# **TPS50601A-SP dual regulator evaluation module (EVM)**

This user's guide contains background information for the TPS50601A-SP as well as support documentation for the TPS50601A-SP evaluation module (TPS50601ASPEVM-D). Also included are the performance specifications, the schematics, and the bill of materials for TPS50601ASPEVM.

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## **Trademarks**

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## 1 Introduction

### 1.1 Background

The TPS50601A-SP dc/dc converter is designed to provide up to a 6-A output in single phase operation.

The TPS50601A-SP implements split-input power rails with separate input voltage inputs for the power stage and control circuitry rated for 3 V to 6.3 V. The TPS50601A-SP provides both inputs, but it was designed and tested using the PVIN connected to VIN. Rated input voltage and output current range for the evaluation module are given in [Table 1](#). This evaluation module is designed to demonstrate features of TPS50601A-SP as well as provide flexibility so input, output capacitors, and output inductors (as well as other components such as frequency adjust, output voltage, and compensation components) can be modified to meet their needs when designing with the TPS50601A-SP regulator. The switching frequency is externally set at a nominal 100 kHz. TPS50601A-SP will operate with switching frequency of 100-kHz to 1-MHz range. For the EVM, 100 kHz was selected as it would provide higher efficiency. The high-side and low-side MOSFETs are incorporated inside the TPS50601A-SP package along with the gate drive circuitry. The low drain-to-source on-resistance of the MOSFET allows the TPS50601A-SP to achieve high efficiencies and helps keep the junction temperature low at high output currents. The compensation components are external to the integrated circuit (IC), and an external divider allows for an adjustable output voltage. Additionally, the TPS50601A-SP provides adjustable slow start, tracking, and undervoltage lockout inputs.

**Table 1. Input Voltage and Output Current Summary of TPS50601ASPEVM**

EVM	INPUT VOLTAGE RANGE	OUTPUT CURRENT RANGE
TPS50601ASPEVM	VIN = 4.45 V to 6.3 V (VIN start voltage = 4.5-V NOM)	0 A to 6 A



**Figure 1. TPS50601ASPEVM Board**

## 1.2 Performance Specification Summary

A summary of the TPS50601ASPEVM performance specifications is provided in [Table 2](#). Specifications are given for an input voltage of  $V_{IN} = 5$  V and an output voltage of 2.5 V, unless otherwise specified. The TPS50601ASPEVM is designed and tested for  $V_{IN} = 4.5$  V to 6.3 V with the  $V_{IN}$  and  $PV_{IN}$  pins connect together with the J1 jumper. The ambient temperature is 25°C for all measurements, unless otherwise noted.

**Table 2. TPS50601ASPEVM Configuration**

SPECIFICATION	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IN}$ voltage range ( $PV_{IN} = V_{IN}$ )		4.5	5	6.3	V
$V_{IN}$ start voltage			4.5		V
$V_{IN}$ stop voltage			3.5		V
Output voltage set point			2.49		V
Output current range	$V_{IN} = 4.5$ V to 6.3 V	0		6	A

## 1.3 Modifications

These evaluation modules are designed to provide access to the features of the TPS50601A-SP. Some modifications can be made to this module. The layout of EVM is designed to make it easy for customer to modify the configuration to meet their needs and adjust for different input, output capacitors, and output inductors.

### 1.3.1 Output Voltage Set Point

The output voltage is set by the resistor divider network of R21 and R22. R21 is fixed at 10 kΩ. To change the output voltage of the EVM, it is necessary to change the value of resistor R22. Changing the value of R22 can change the output voltage above 0.804 V. The value of R22 for a specific output voltage can be calculated using [Equation 1](#).

$$R_{22} = \frac{V_{REF} \times R_{21}}{(V_{OUT} - V_{REF})}$$

where

- $V_{REF} = 0.804$  V
- (1)

[Table 3](#) lists the R22 values for some common output voltages. The values given in [Table 3](#) are standard values, not the exact value calculated using [Equation 1](#).

**Table 3. Output Voltages Available**

Output Voltage (V)	R22 Value (kΩ)
1.2	20
1.8	8.06
2.5	4.7
3.3	3.2

### 1.3.2 Maximum Duty Cycle Limit

The TPS50601A-SP can operate at high duty cycle up to 100%. As we approach 100% duty cycle, via reduction in input voltage, feedback will ensure that high side MOSFET is kept on. This will result in  $V_{out}$  equal to  $V_{in}$  less the circuit drops.

### 1.3.3 Slow-Start Time

The slow-start time can be adjusted by changing the value of C1. Use [Equation 2](#) to calculate the required value of C1 for a desired slow-start time.

$$C_1(\text{nF}) = \frac{T_{ss}(\text{ms}) \times I_{ss}(\mu\text{A})}{V_{ref}(\text{V})} \quad (2)$$

The EVM is set for a slow-start time of 4 ms using  $C_1 = 0.01 \mu\text{F}$  and  $I_{ss} = 2 \mu\text{A}$ .

### 1.3.4 Adjustable UVLO

The undervoltage lockout (UVLO) can be adjusted externally using R13 and R15. The EVM is set for a start voltage of 4.6 V and a stop voltage of 4.3 V using  $R13 = 10 \text{ k}\Omega$  and  $R15 = 3.4 \text{ k}\Omega$  at no load conditions. Use [Equation 3](#) and [Equation 4](#) to calculate required resistor values for different start and stop voltages. When output is loaded, this results in increase in ripple current on PVIN. In order to minimize the effect of PVIN ripple on enable, capacitor  $C5 = 0.1 \mu\text{F}$  is installed across R15. Thus R13/C5 behaves as an RC filter.

$$R6 = \frac{V_{START} \left( \frac{V_{ENFALLING}}{V_{ENRISING}} \right) - V_{STOP}}{I_p \left( 1 - \frac{V_{ENFALLING}}{V_{ENRISING}} \right) + I_h} \quad (3)$$

$$R7 = \frac{R1 \times V_{ENFALLING}}{V_{STOP} - V_{ENFALLING} + R6(I_p + I_h)}$$

where

- $I_h = 3 \mu\text{A}$ ,  $I_p = 6.1 \mu\text{A}$ ,  $V_{ENRISING} = 1.14 \text{ V}$ ,  $V_{ENFALLING} = 1.11 \text{ V}$
- (4)

Nominal start voltage is 4.5 V and worse case start voltage is 4.6 V. Nominal stop voltage is 4.3 V and worse case stop voltage 4 V.

## 2 Input Voltage Rails

The EVM is designed to accommodate different input voltage levels for the power stage and control logic. During normal operation, the PVIN and VIN inputs are connected together using a jumper across J1. The single input voltage is supplied at J2 (PVIN+) and J5 (GND). If desired, these input voltage rails may be separated by removing the jumper across J2. Two input voltages must then be provided at both J2 (PVIN), J3 (GND) and J11 (VIN) J15 (GND).

## 3 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS50601A-SP evaluation module. The section also includes test results typical for the evaluation module and covers efficiency, output voltage regulation, load transients, output ripple, input ripple, loop characteristics and start-up.

### 3.1 Input/Output Connections

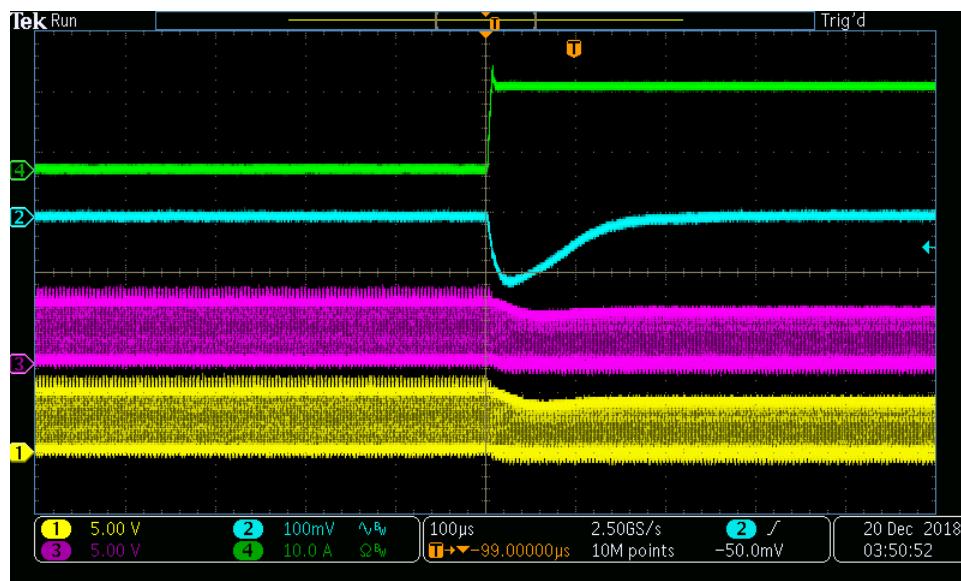
The TPS50601ASPEVM is provided with input/output connectors and test points as shown in [Table 4](#). A power supply capable of supplying 18 A must be connected to J7 through a pair of 16-AWG wires. The jumper across J1 must be in place. See [Section 2](#) for split-input voltage rail operation. The load must be connected to J8/J10 through a pair of 16-AWG wires. The maximum load current capability must be 6 A. Wire lengths must be minimized to reduce losses in the wires. Test-point TP4 provides a place to monitor the  $V_{IN}$  input voltages with TP14 providing a convenient ground reference. TP17 is used to monitor the output voltage with TP24 as the ground reference.

**Table 4. EVM Connectors and Test Points**

Reference Designator	Function
J2	PVIN input voltage banana plug (see <a href="#">Table 2</a> for PVIN range).
J5	PVIN(GND) input voltage banana plug.
J11	VIN input voltage connector. Not normally used.
J1	PVIN to VIN jumper. Normally closed to tie VIN to PVIN for common rail voltage operation.
J3	2-pin header for enable. Connect EN to ground to disable, open to enable.
J6/J7	Connecting phase 1 output to phase 2 output for Dual Operation.
J8	VOUT, 2.5 V at 6 A maximum for Single EVM.
TP6	PVIN test point at PVIN connector.
TP14	GND test point at PVIN connector.
TP4	VIN test point at VIN connector.
J4	Cold nose probe to monitor Switch/Phase node.
J9	Cold nose probe to monitor output voltage/ripple.
TP21	Output voltage test point at VOUT connector.
TP24	GND test point at VOUT connector.
TP3	PWRGD test point.

### 3.2 Load Transients

Figure 2 shows the TPS50601ASPEVM response to load transients. The current step is from 3 mA to 5 A of maximum rated load at 5-V input. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.



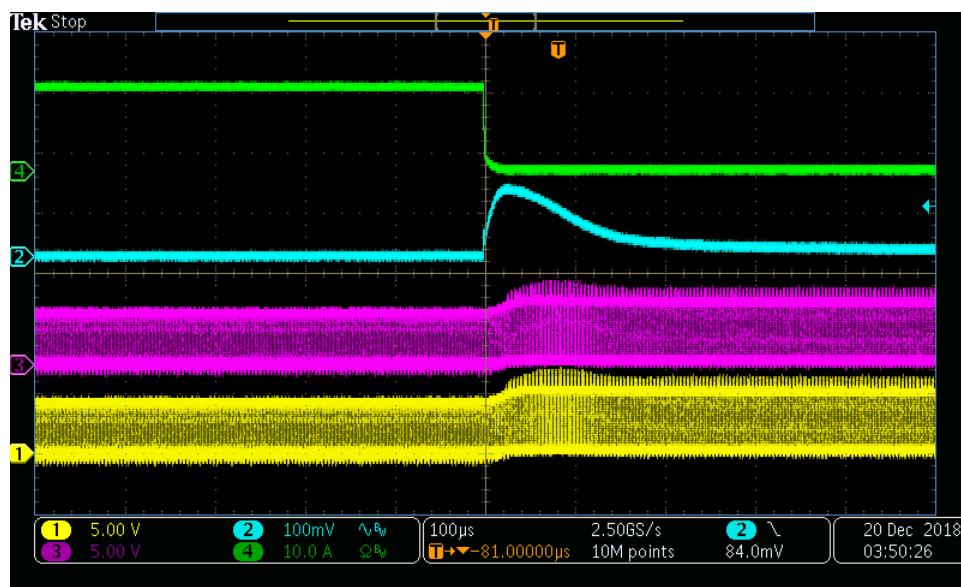
Ch1 = PH Node 1

Ch2 = Output Voltage

Ch3 = PH Node 2

Ch4 = Output Load

Figure 2. TPS50601ASPEVM Positive Load Step



Ch1 = PH Node 1

Ch2 = Output Voltage

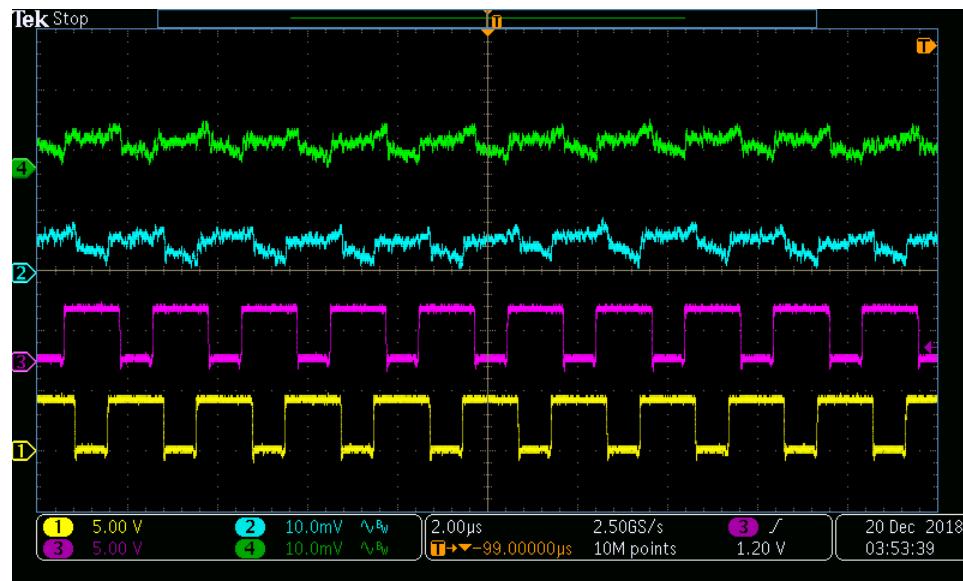
Ch3 = PH Node 2

Ch4 = Output Load

Figure 3. TPS50601ASPEVM Negative Load Step

### 3.3 Output Voltage Ripple

**Figure 4** shows the TPS50601ASPEVM output voltage ripple. The output current is the rated full load of 6 A and VIN = 5 V. The ripple voltage is measured at J9 with oscilloscope bandwidth limited to 20 MHz. Note that C20 0.1- $\mu$ F capacitor is installed close to J9 to help suppress high-frequency noise.



Ch1 = PH Node 1

Ch2 = Output Voltage 1

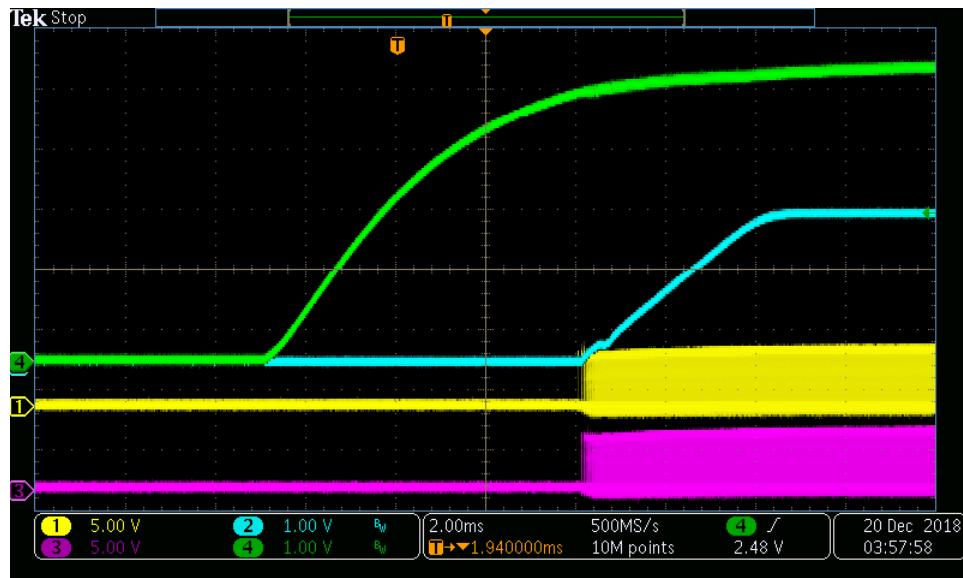
Ch3 = PH Node 2

Ch4 = Output Voltage 2

**Figure 4. TPS50601ASPEVM Output Ripple**

### 3.4 Powering Up

[Figure 5](#) and [Figure 6](#) show the start-up waveforms for the TPS50601ASPEVM. In [Figure 5](#), the output voltage ramps up as soon as the input voltage reaches the UVLO threshold as set by the R13 and R15 resistor divider network. In [Figure 6](#), the input voltage is initially applied and the output is inhibited by using a jumper at J3 to tie EN to GND. When the jumper is removed, EN is released. When the EN voltage reaches the enable-threshold voltage, the start-up sequence begins and the output voltage ramps up to the externally set value of 2.5 V. The input voltage for these plots is 5 V and the load is 12 A.

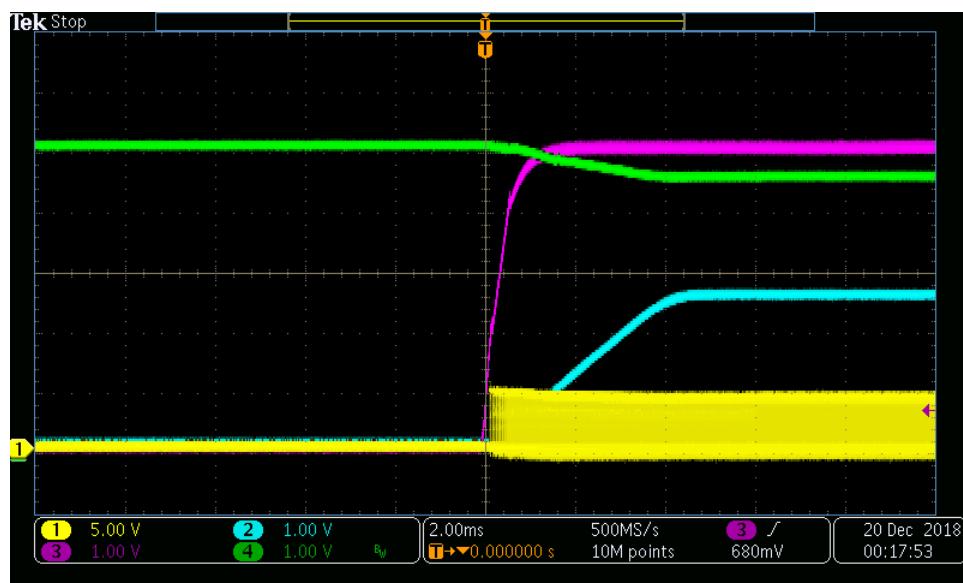


Ch1 = PH Node 1

Ch2 = Output Voltage

Ch3 = PH Node 2

Ch4 = Input Voltage

**Figure 5. TPS50601ASPEVM Start-Up Relative to  $V_{IN}$** 

Ch1 = PH Node 1

Ch2 = Output Voltage

Ch3 = PEN Pin

Ch4 = Output Voltage 2

**Figure 6. TPS50601ASPEVM Start-up Relative to Enable**

### 3.5 Loop Characteristics

Figure 7 shows the TPS50601ASPEVM loop-response characteristics. Gain and phase plots are shown for VIN voltage of 5 V. Load current for the measurement is 12 A.

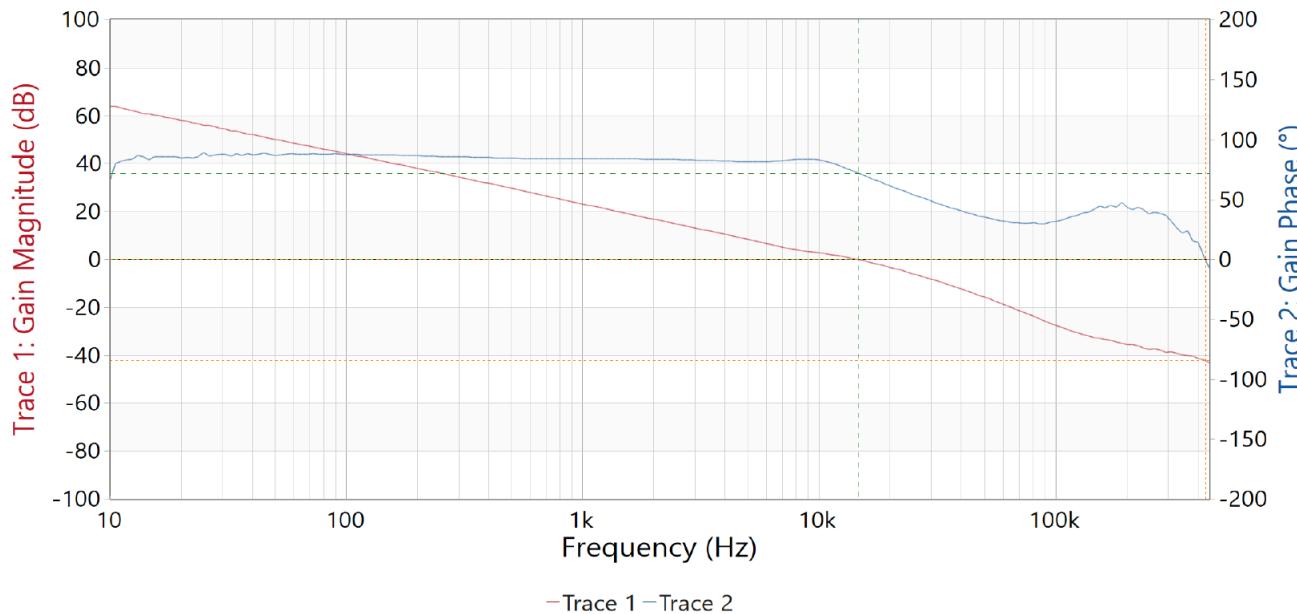


Figure 7. TPS50601ASPEVM Complete Loop Response

## 4 Board Layout

This section provides a description of the TPS50601ASPEVM, board layout, and layer illustrations.

### 4.1 Layout

The board layout for the TPS50601ASPEVM is shown in [Figure 8](#) through [Figure 12](#). The top-side layer of the EVM is laid out in a manner typical of a user application. The top, bottom, and internal layers are 2-oz copper.

The top layer contains the main power traces for PVIN, VIN, VOUT, and VPHASE. On the top layer are power and ground connections of the TPS50601ASPEVM. TPS50601A-SP IC is mounted on the top layer with thermal pad and pin 1 (analog ground) of TPS50601A-SP connected to the second layer, the ground plane. The third layer has signal traces. The top side ground traces are connected to the bottom and internal ground planes with multiple vias placed around the board. Vias directly under the TPS50601A-SP device provide a thermal path from the top-side ground plane to the bottom-side ground plane and connecting to layer 3 (analog ground).

The input decoupling capacitors (C8, C9, C10, C11, C12, C3, C4) are all located as close to the IC as possible. In addition, the voltage set-point resistor divider components are also kept close to the IC. The voltage divider network ties to the output voltage at the point of regulation. Hooks are placed allowing the user to run bode plots on the unit by replacing R19 with a 50- $\Omega$  resistor. For the TPS50601ASPEVM, an additional input bulk capacitor may be required, depending on the EVM connection to the input supply. Critical analog circuits such as the voltage set point divider, frequency set resistor, slow start capacitor and compensation components are terminated to analog ground using a wide ground trace separate from the power ground pour. Analog ground is connected to power ground.

TPS50601ASPEVM PCB is made larger than required to provide flexibility for the customer to add additional capacitors on both input and output as well as replace output inductors to meet their system needs.

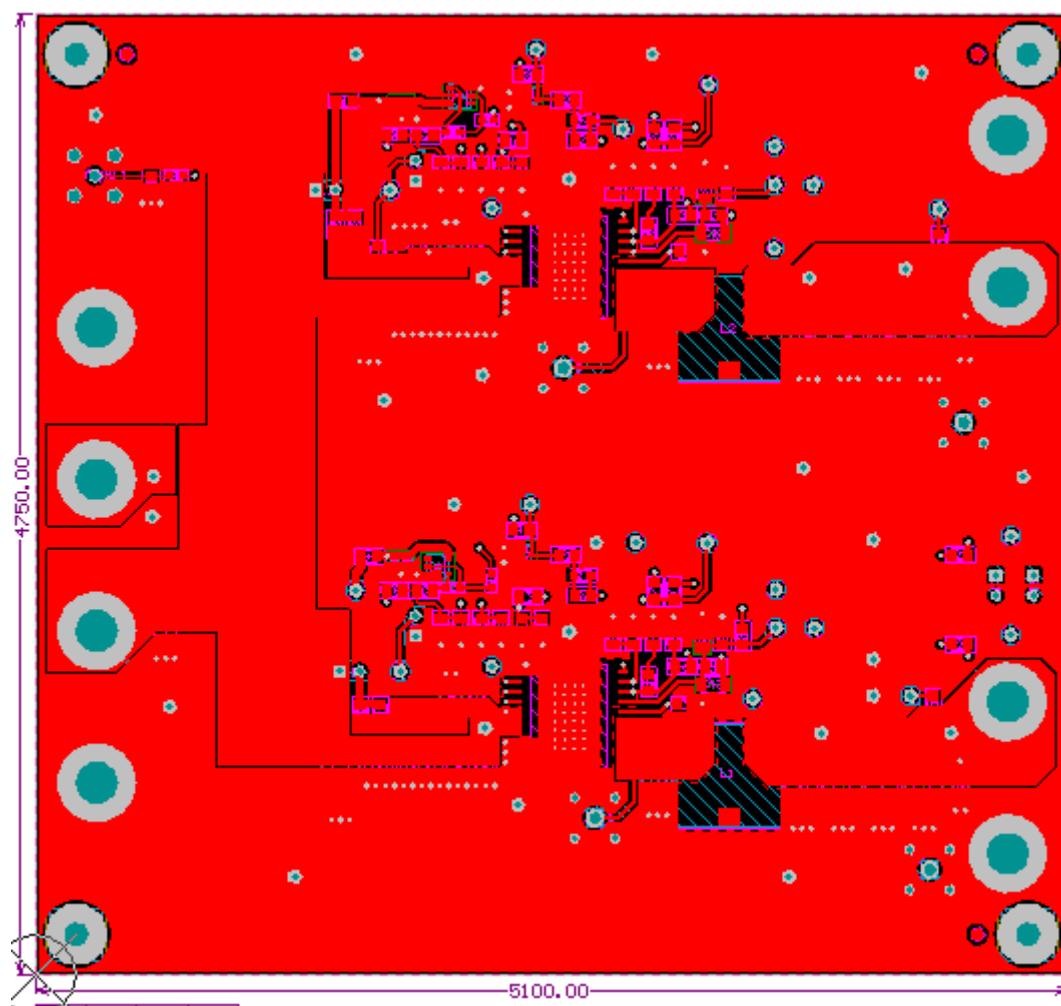


Figure 8. TPS50601ASPEVM Top-Side Layer 1

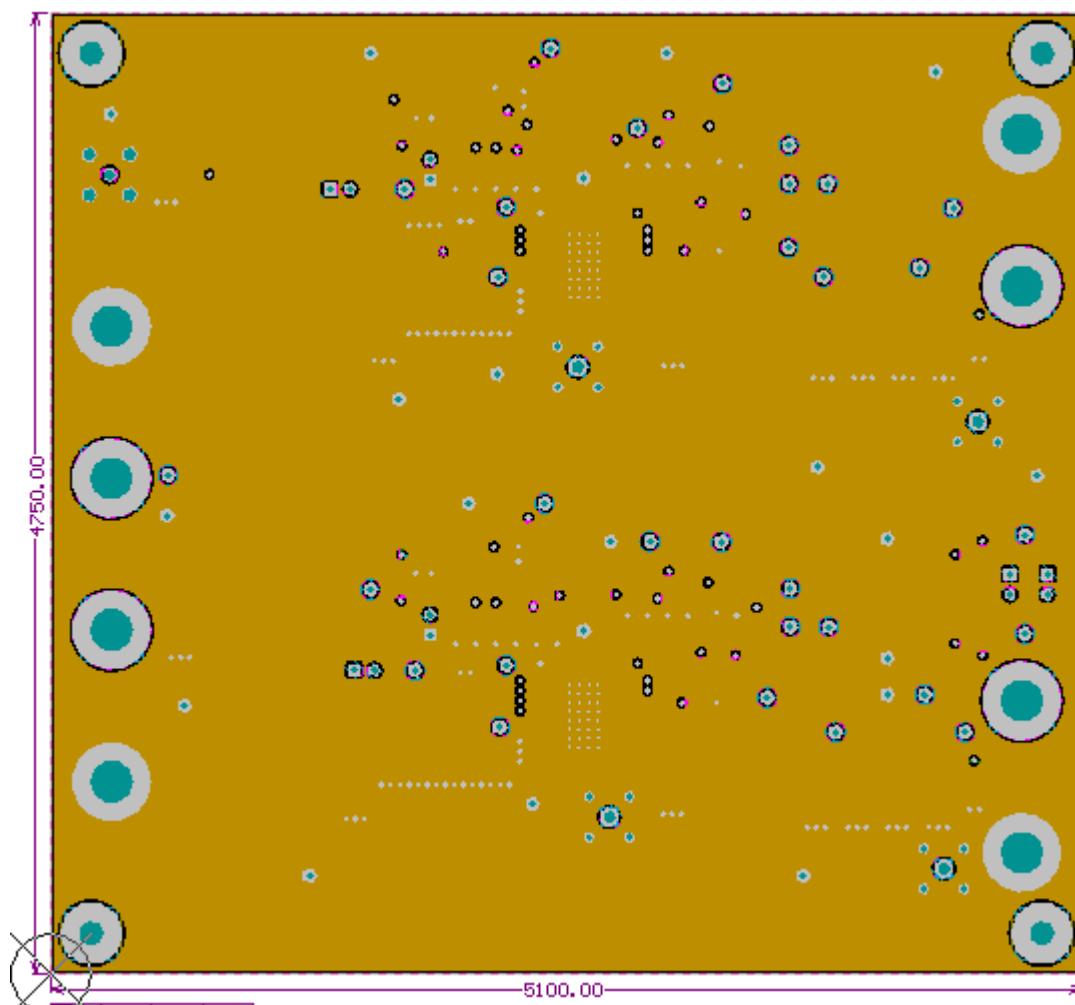


Figure 9. TPS50601ASPEVM Layer 2

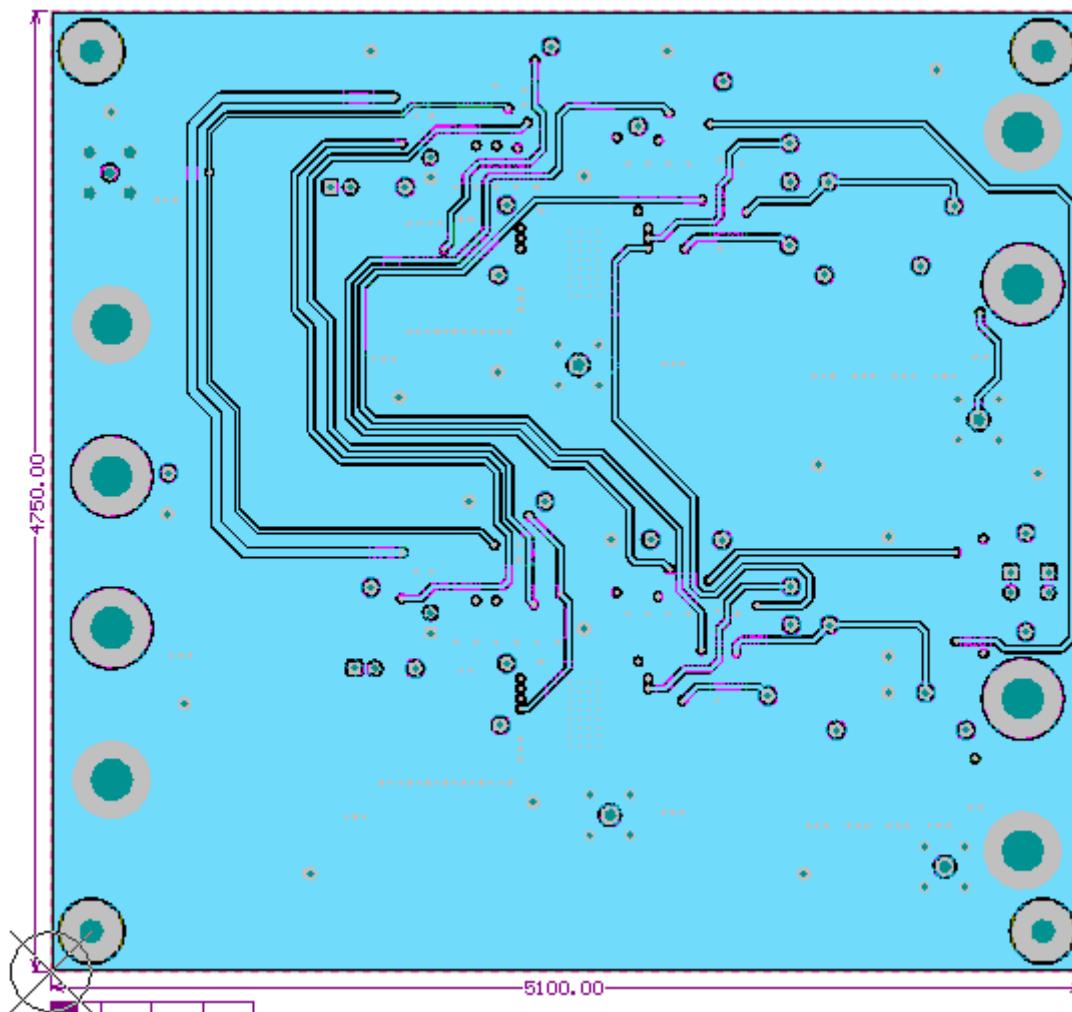


Figure 10. TPS50601ASPEVM Layer 3

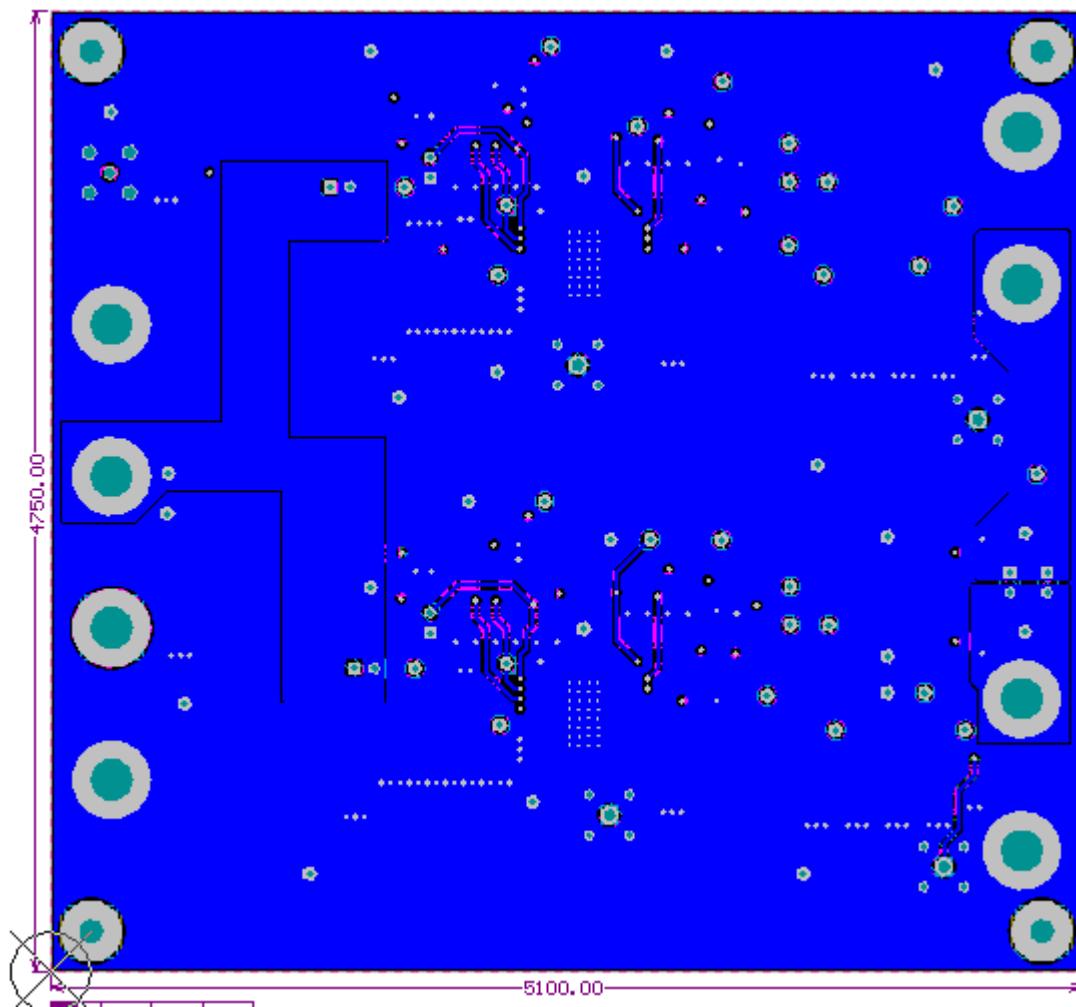


Figure 11. TPS50601ASPEVM Bottom-Side Layer 4

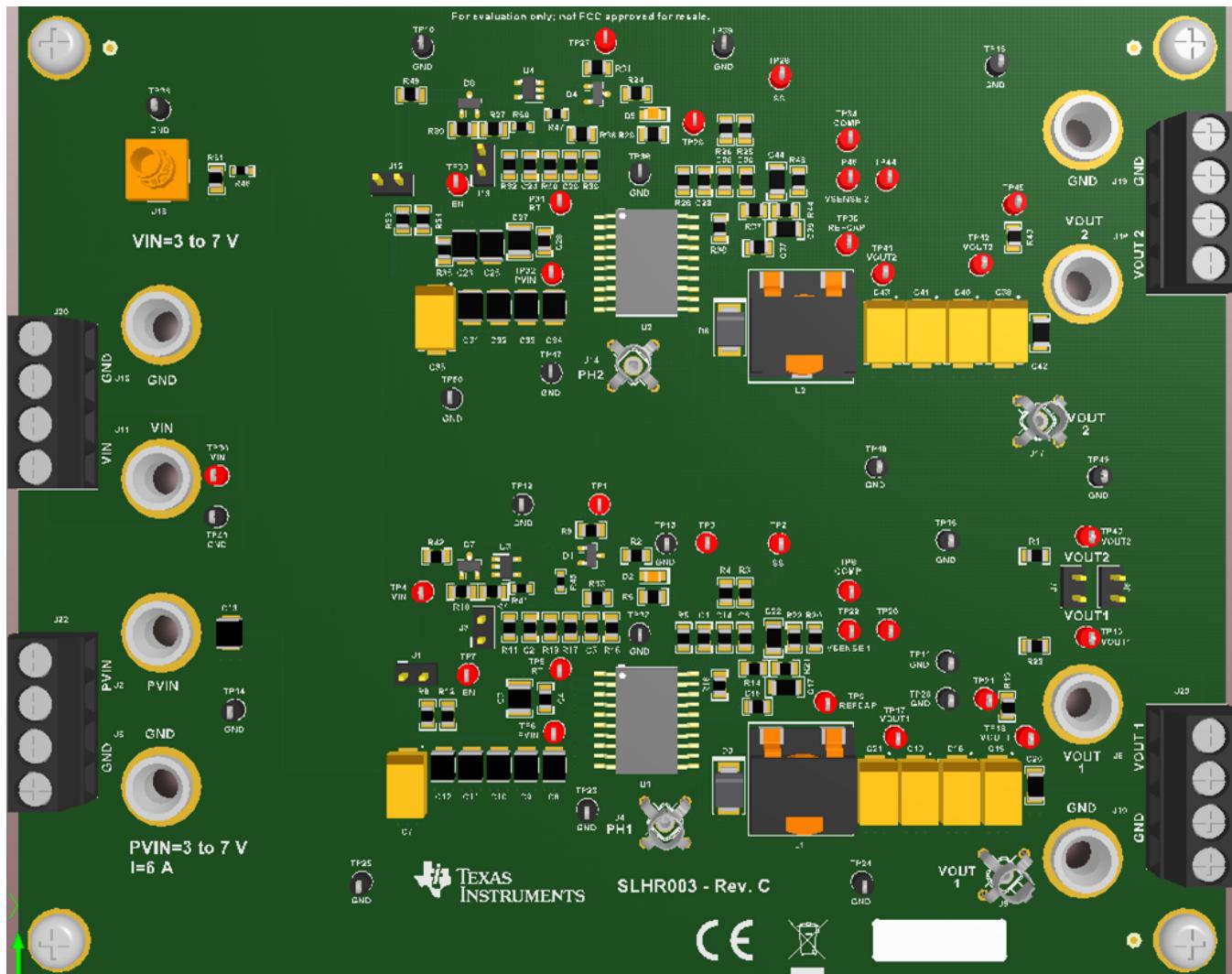


Figure 12. TPS50601ASPEVM Assembly

## 5 Schematic and Bill of Materials

### 5.1 Schematic

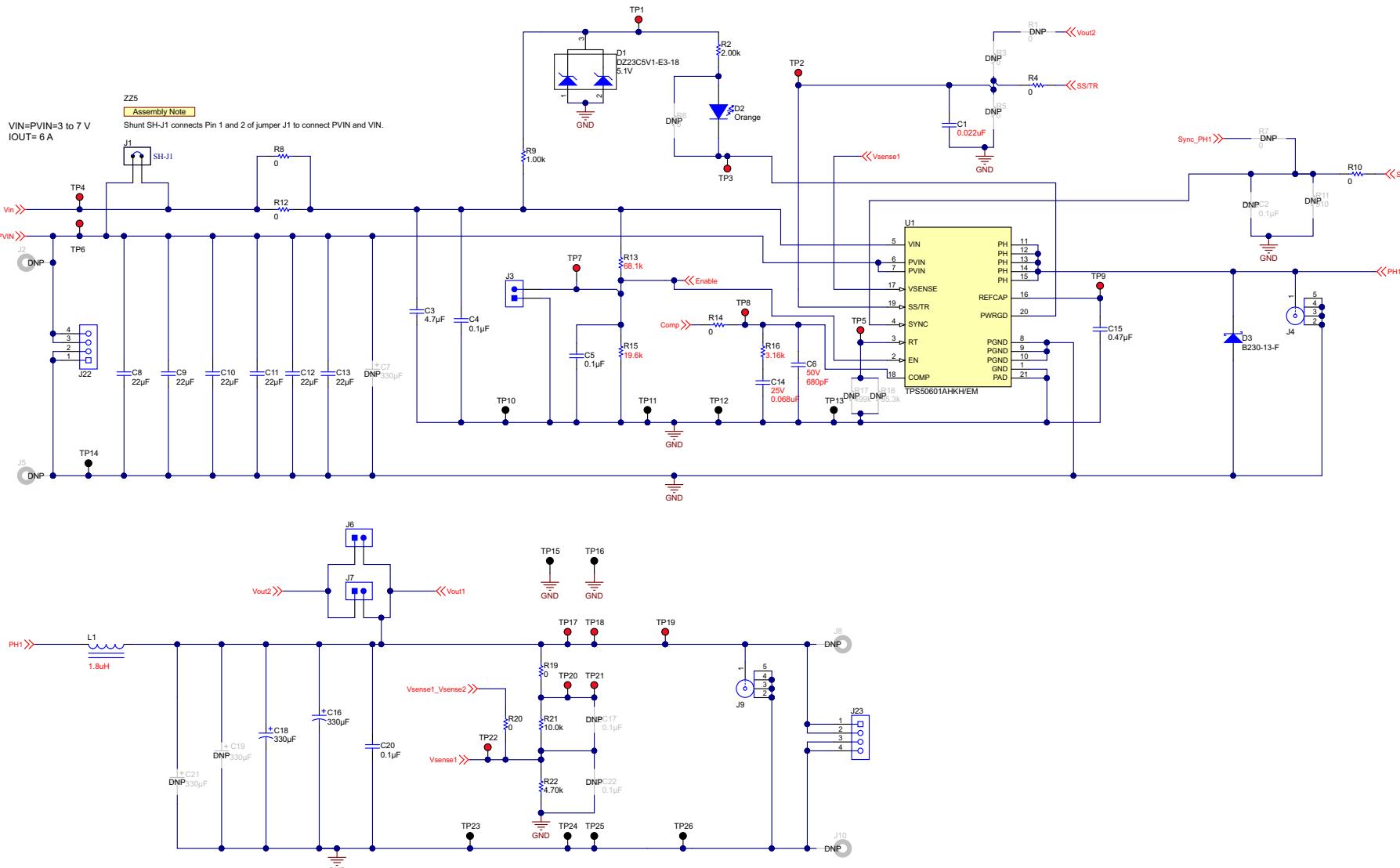
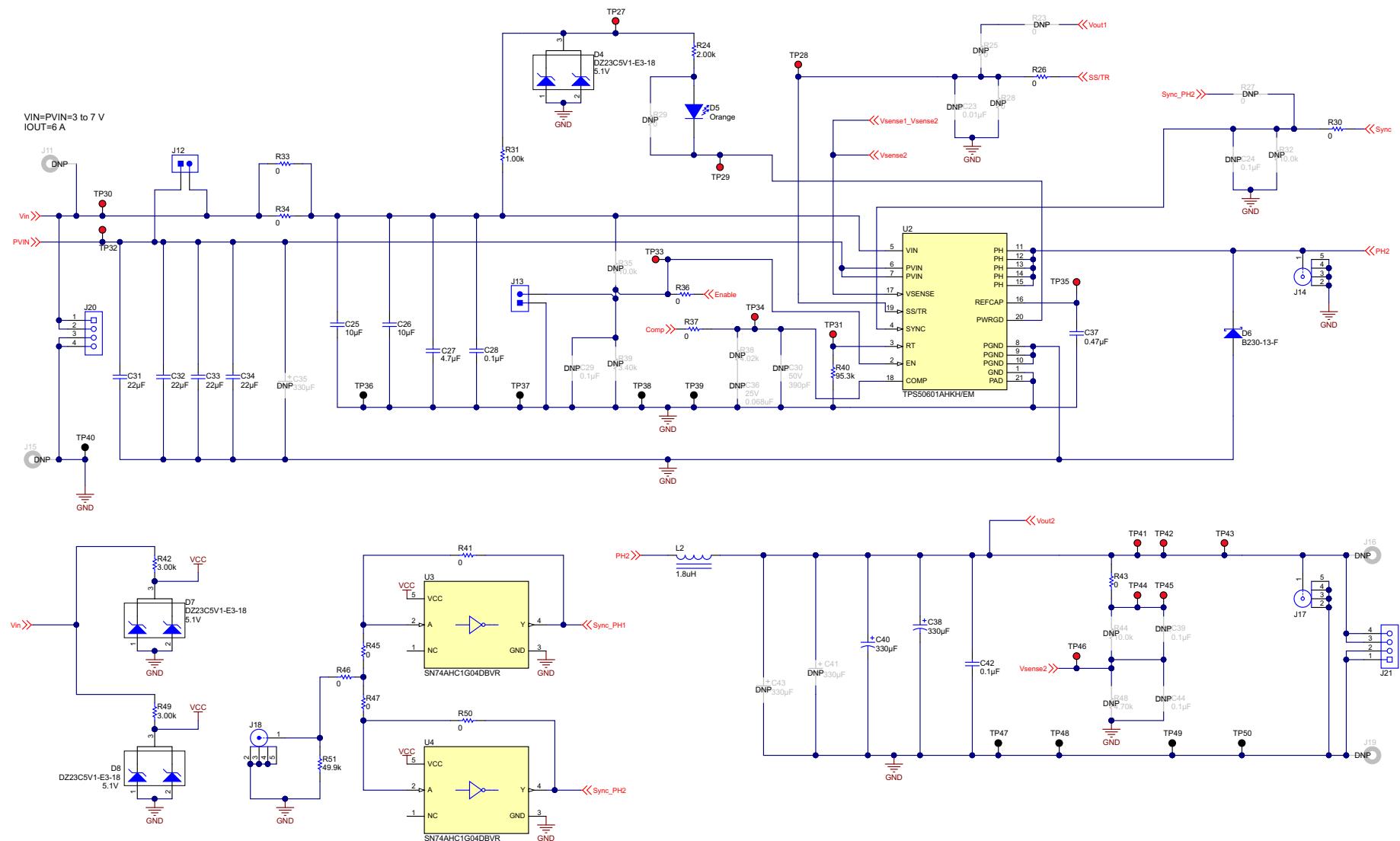


Figure 13. Master Schematic



**Figure 14. Slave Schematic**

## 5.2 Bill of Materials

**Table 5. Bill of Materials**

Item #	Designator	Quantity	Value	PartNumber	Manufacturer	Description	PackageReference
1	!PCB1	1		SLHR003	Any	Printed Circuit Board	
2	C1	1	0.022uF	08051C223KAT2A	AVX	CAP, CERM, 0.022 uF, 100 V, +/- 10%, X7R, 0805	0805
3	C3, C27	2	4.7uF	C1210C475K8RACTU	Kemet	CAP, CERM, 4.7 $\mu$ F, 10 V, +/- 10%, X7R, 1210	1210
4	C4, C5, C28	3	0.1uF	08055C104JAT2A	AVX	CAP, CERM, 0.1 $\mu$ F, 50 V, +/- 5%, X7R, 0805	0805
5	C6	1	680pF	08055A681JAT2A	AVX	CAP, CERM, 680 pF, 50 V, +/- 5%, COG/NP0, 0805	0805
6	C8, C9, C10, C11, C12, C13, C31, C32, C33, C34	10	22uF	C3225X7R1C226K250AC	TDK	CAP, CERM, 22 $\mu$ F, 16 V, +/- 10%, X7R, 1210	1210
7	C14	1	0.068uF	GRM219R71E683KA01D	MuRata	CAP, CERM, 0.068 $\mu$ F, 25 V, +/- 10%, X7R, 0805	0805
8	C15, C37	2	0.47uF	C2012X7R1H474K125AB	TDK	CAP, CERM, 0.47 $\mu$ F, 50 V, +/- 10%, X7R, 0805	0805
9	C16, C18, C38, C40	4	330uF	T530X337M010ATE006	Kemet	CAP, Tantalum Polymer, 330 $\mu$ F, 10 V, +/- 20%, 0.006 ohm, 7343-43 SMD	7343-43
10	C20, C42	2	0.1uF	C1206C104J5RACTU	Kemet	CAP, CERM, 0.1 $\mu$ F, 50 V, +/- 5%, X7R, 1206	1206
11	C25, C26	2	10uF	12103C106KAT2A	AVX	CAP, CERM, 10 $\mu$ F, 25 V, +/- 10%, X7R, 1210	1210
12	D1, D4, D7, D8	4	5.1V	DZ23C5V1-E3-18	Vishay-Semiconductor	Diode, Zener, 5.1 V, 300 mW, AEC-Q101, SOT-23	SOT-23
13	D2, D5	2	Orange	LTST-C170KFKT	Lite-On	LED, Orange, SMD	LED_0805
14	D3, D6	2	30V	B230-13-F	Diodes Inc.	Diode, Schottky, 30 V, 2 A, SMB	SMB
15	H1, H2, H3, H4	4		NY PMS 440 0025 PH	B_and_F Fastener Supply	Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	Screw
16	H5, H6, H7, H8	4		1902C	Keystone	Standoff, Hex, 0.5" L #4-40 Nylon	Standoff
17	J1, J3, J6, J7, J12, J13	6		TSW-102-07-G-S	Samtec	Header, 100mil, 2x1, Gold, TH	2x1 Header
18	J4, J9, J14, J17	4		131-5031-00	Tektronix	Compact Probe Tip Circuit Board Test Points, TH, 25 per	TH Scope Probe
19	J18	1		901-144-8RFX	Amphenol RF	SMA Straight Jack, Gold, 50 Ohm, TH	SMA Straight Jack, TH
20	J20, J21, J22, J23	4		39544-3004	Molex	Terminal Block, 4x1, 5.08mm, TH	4x1 Terminal Block
21	L1, L2	2	1.8uH	SER1360-182KLB	Coilcraft	Inductor, Shielded E Core, Ferrite, 1.8 $\mu$ H, 13 A, 0.0026 ohm, AEC-Q200 Grade 3, SMD	SER1360

**Table 5. Bill of Materials (continued)**

Item #	Designator	Quantity	Value	PartNumber	Manufacturer	Description	PackageReference
22	LBL1	1		THT-14-423-10	Brady	Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	PCB Label 0.650" H x 0.200" W
23	R2, R24	2	2.00k	CRCW08052K00FKEA	Vishay-Dale	RES, 2.00 k, 1%, 0.125 W, 0805	0805
24	R4, R8, R10, R12, R14, R19, R20, R26, R30, R33, R34, R36, R37, R43	14	0	CRCW08050000Z0EA	Vishay-Dale	RES, 0, 5%, 0.125 W, 0805	0805
25	R9, R31	2	1.00k	CRCW08051K00FKEA	Vishay-Dale	RES, 1.00 k, 1%, 0.125 W, 0805	0805
26	R13	1	68.1k	CRCW080568K1FKEA	Vishay-Dale	RES, 68.1 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	0805
27	R15	1	19.6k	CRCW080519K6FKEA	Vishay-Dale	RES, 19.6 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	0805
28	R16	1	3.16k	CRCW08053K16FKEA	Vishay-Dale	RES, 3.16 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	0805
29	R21	1	10.0k	RG2012P-103-B-T5	Susumu Co Ltd	RES, 10.0 k, 0.1%, 0.125 W, 0805	0805
30	R22	1	4.70k	RG2012P-472-B-T5	Susumu Co Ltd	RES, 4.70 k, 0.1%, 0.125 W, 0805	0805
31	R40	1	95.3k	CRCW080595K3FKEA	Vishay-Dale	RES, 95.3 k, 1%, 0.125 W, 0805	0805
32	R41, R45, R46, R47, R50	5	0	CRCW06030000Z0EA	Vishay-Dale	RES, 0, 5%, 0.1 W, 0603	0603
33	R42, R49	2	3.00k	ERJ-6ENF3001V	Panasonic	RES, 3.00 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	0805
34	R51	1	49.9k	CRCW080549K9FKEA	Vishay-Dale	RES, 49.9 k, 1%, 0.125 W, 0805	0805
35	SH-J1	1	1x2	SPC02SYAN	Sullins Connector Solutions	Shunt, 100mil, Flash Gold, Black	Closed Top 100mil Shunt
36	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP17, TP18, TP19, TP20, TP21, TP22, TP27, TP28, TP29, TP30, TP31, TP32, TP33, TP34, TP35, TP41, TP42, TP43, TP44, TP45, TP46	30		5000	Keystone	Test Point, Miniature, Red, TH	Red Miniature Testpoint
37	TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP23, TP24, TP25, TP26, TP36, TP37, TP38, TP39, TP40, TP47, TP48, TP49, TP50	20		5001	Keystone	Test Point, Miniature, Black, TH	Black Miniature Testpoint
38	U1, U2	2		TPS50601AHKH/EM	Texas Instruments	Radiation Hardened 3.0- to 6.3-V Input, 6-A Synchronous Buck Converter, HKH0020A (CFP-20)	HKH0020A
39	U3, U4	2		SN74AHC1G04DBVR	Texas Instruments	SINGLE SCHMITT-TRIGGER INVERTER GATE, DBV0005A (SOT-5)	DBV0005A
40	C2, C24, C29	0	0.1uF	08055C104JAT2A	AVX	CAP, CERM, 0.1 $\mu$ F, 50 V, +/- 5%, X7R, 0805	0805

**Table 5. Bill of Materials (continued)**

Item #	Designator	Quantity	Value	PartNumber	Manufacturer	Description	PackageReference
41	C7, C19, C21, C35, C41, C43	0	330uF	T530X337M010ATE006	Kemet	CAP, Tantalum Polymer, 330 $\mu$ F, 10 V, +/- 20%, 0.006 ohm, 7343-43 SMD	7343-43
42	C17, C22, C39, C44	0	0.1uF	C1206C104J5RACTU	Kemet	CAP, CERM, 0.1 $\mu$ F, 50 V, +/- 5%, X7R, 1206	1206
43	C23	0	0.01uF	GRM216R71H103KA01D	MuRata	CAP, CERM, 0.01 $\mu$ F, 50 V, +/- 10%, X7R, 0805	0805
44	C30	0	390pF	GRM2165C1H391JA01D	MuRata	CAP, CERM, 390 pF, 50 V, +/- 5%, COG/NPO, 0805	0805
45	C36	0	0.068uF	GRM219R71E683KA01D	MuRata	CAP, CERM, 0.068 $\mu$ F, 25 V, +/- 10%, X7R, 0805	0805
46	FID1, FID2, FID3	0		N/A	N/A	Fiducial mark. There is nothing to buy or mount.	Fiducial
47	J2, J5, J8, J10, J11, J15, J16, J19	0		575-4	Keystone	Standard Banana Jack, Uninsulated, 5.5mm	Keystone_575-4
48	R1, R3, R5, R6, R7, R23, R25, R27, R28, R29	0	0	CRCW08050000Z0EA	Vishay-Dale	RES, 0, 5%, 0.125 W, 0805	0805
49	R11	0	910	CRCW0805910RJNEA	Vishay-Dale	RES, 910, 5%, 0.125 W, AEC-Q200 Grade 0, 0805	0805
50	R17	0	499k	RG2012P-4993-B-T5	Susumu Co Ltd	RES, 499 k, 0.1%, 0.125 W, 0805	0805
51	R18	0	95.3k	CRCW080595K3FKEA	Vishay-Dale	RES, 95.3 k, 1%, 0.125 W, 0805	0805
52	R32, R35	0	10.0k	CRCW080510K0FKEA	Vishay-Dale	RES, 10.0 k, 1%, 0.125 W, 0805	0805
53	R38	0	4.02k	CRCW08054K02FKEA	Vishay-Dale	RES, 4.02 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805	0805
54	R39	0	3.40k	CRCW08053K40FKEA	Vishay-Dale	RES, 3.40 k, 1%, 0.125 W, 0805	0805
55	R44	0	10.0k	RG2012P-103-B-T5	Susumu Co Ltd	RES, 10.0 k, 0.1%, 0.125 W, 0805	0805
56	R48	0	4.70k	RG2012P-472-B-T5	Susumu Co Ltd	RES, 4.70 k, 0.1%, 0.125 W, 0805	0805

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