

AN-1312 SCANSTA111/SCANSTA112 Scan Bridge Timing

ABSTRACT

This application report contains the timing information for both the SCANSTA111 and the SCANSTA112.

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1 Introduction

The term Scan Bridge is used in this application report to refer to either of these devices.

When multiple devices are connected to a local scan port (LSP) of a Scan Bridge, there are delays associated with the Scan Bridge and with the LSP scan chain that must be considered during timing analysis. Because of the propagation delay through the Scan Bridge and the delay through the devices on the LSP, the backplane TCK is delayed as it propagates through the LSP scan chain.

2 Operation

In the JTAG Test Access Port (TAP), data is clocked in on the rising edge of the Test Clock (TCK) line. The synchronous inputs are the Test Mode Select (TMS) and Test Data In (TDI) lines. Data is clocked out on the falling edge of the TCK line. The synchronous output is the Test Data Out (TDO) line.

In normal application of the JTAG TAP, the TCK line is routed to all the devices in the scan chain in parallel. This minimizes the skew between the clock edges seen from one device versus those seen from another. All the devices in the scan chain set their TDO outputs at approximately the same time, when they detect the falling edge of the TCK line. All the devices in the scan chain read their TMS and TDI inputs at approximately the same time, when they detect the rising edge of the TCK line.

A block diagram of the JTAG application with a single TAP is shown in [Figure 1](#).

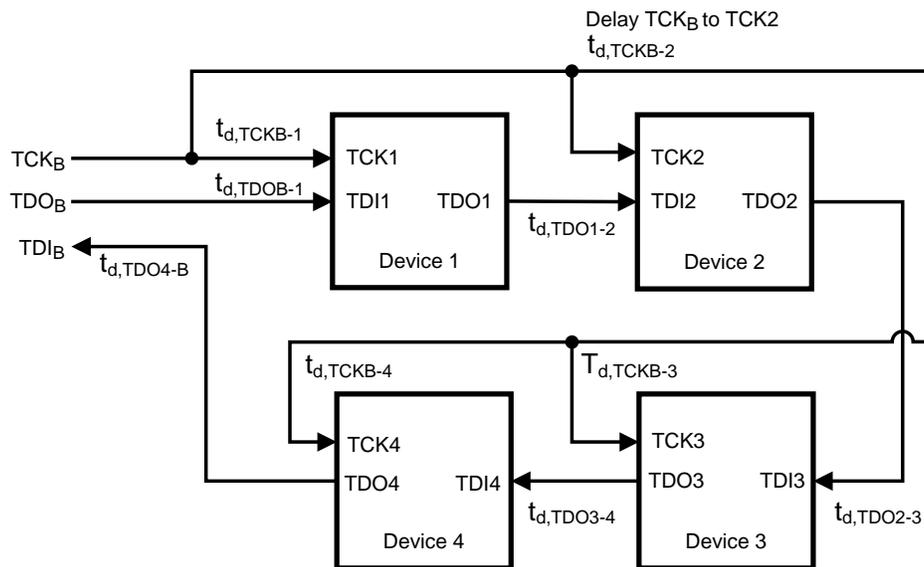


Figure 1. Block Diagram of JTAG Application With a Single TAP

When a Scan Bridge is used to partition the JTAG TAP, the Scan Bridge is inserted between the backplane TAP and the LSPs. This changes the timing of the data and clocks in the scan chain. A partial block diagram of a scan chain partitioned using a Scan Bridge is shown in [Figure 2](#). Note that in the partitioned scan chain the TCK_B line is not connected to the devices on the LSP scan chain.

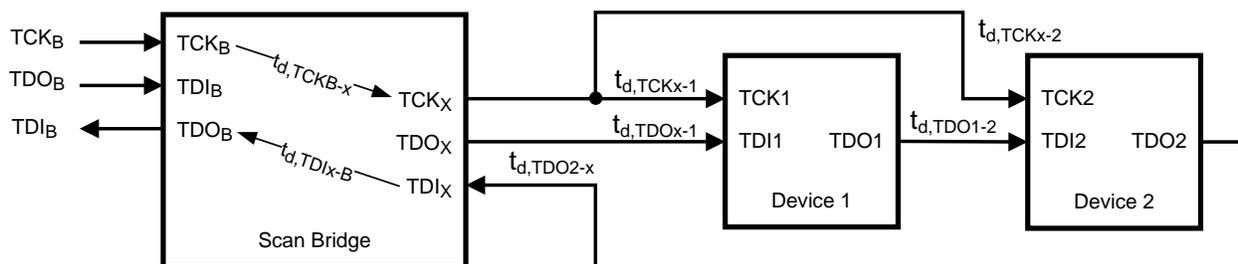


Figure 2. Block Diagram of JTAG Application With the Scan Chain Partitioned Using a Scan Bridge

Figure 3 shows a timing diagram for a simple scan chain like that shown in Figure 1. The propagation delays shown for the TCK signals are exaggerated for clarity. For a simple scan chain like this, the source of the propagation delays on the TCK line is the transmission delay induced by the board connections. For an FR-4 board, a trace length of six inches induces a propagation delay of about 1 ns.

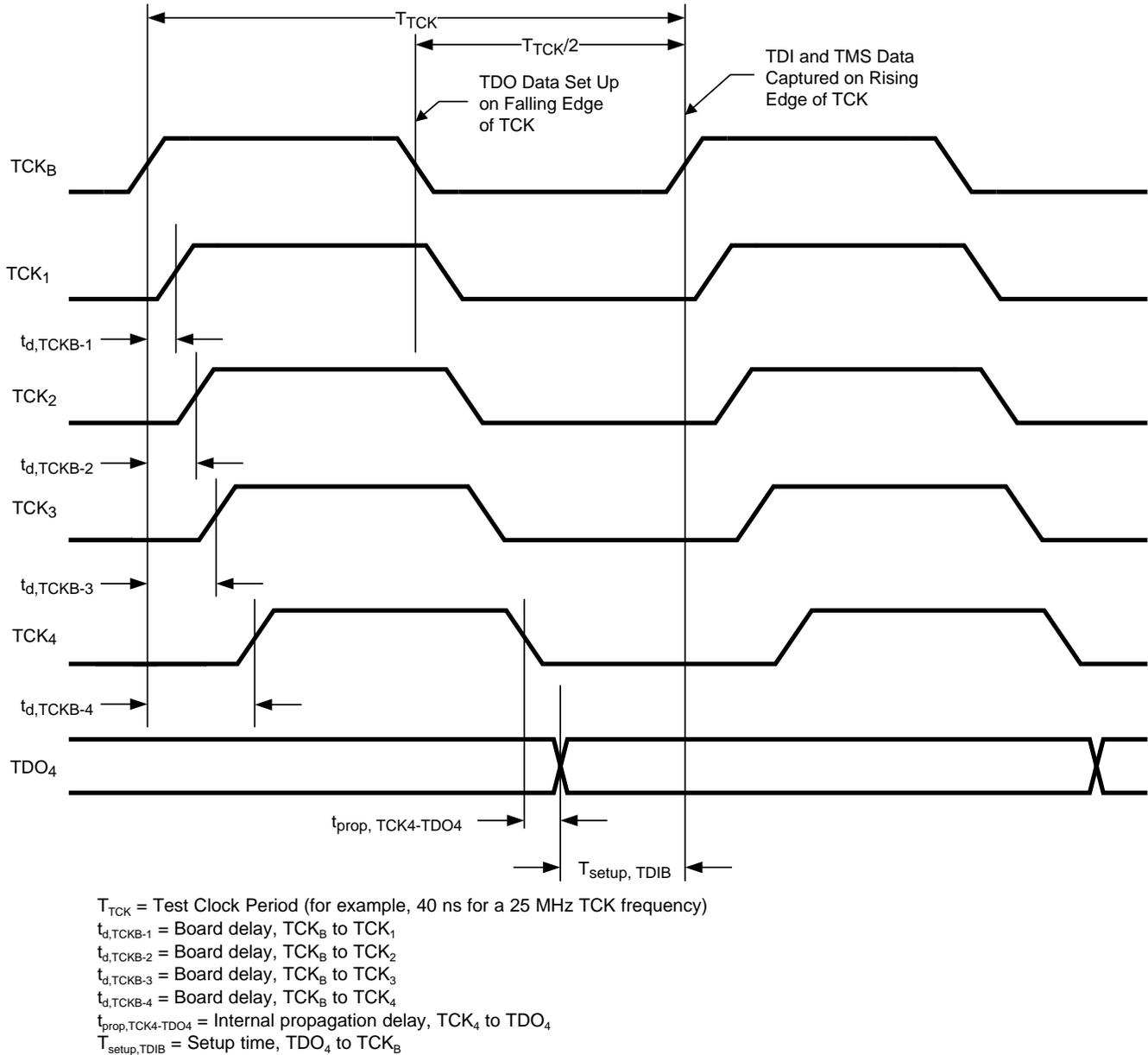


Figure 3. Simple Scan Chain Timing Diagram

The important specifications to be satisfied by the timing of the scan chain are the setup and hold times for the TDI_B input to the boundary scan master. Of course, the setup and hold times for all the other devices in the scan chain must also be satisfied, but if the setup and hold times for the boundary scan master are satisfied the other devices' setup and hold times will probably be satisfied as well.

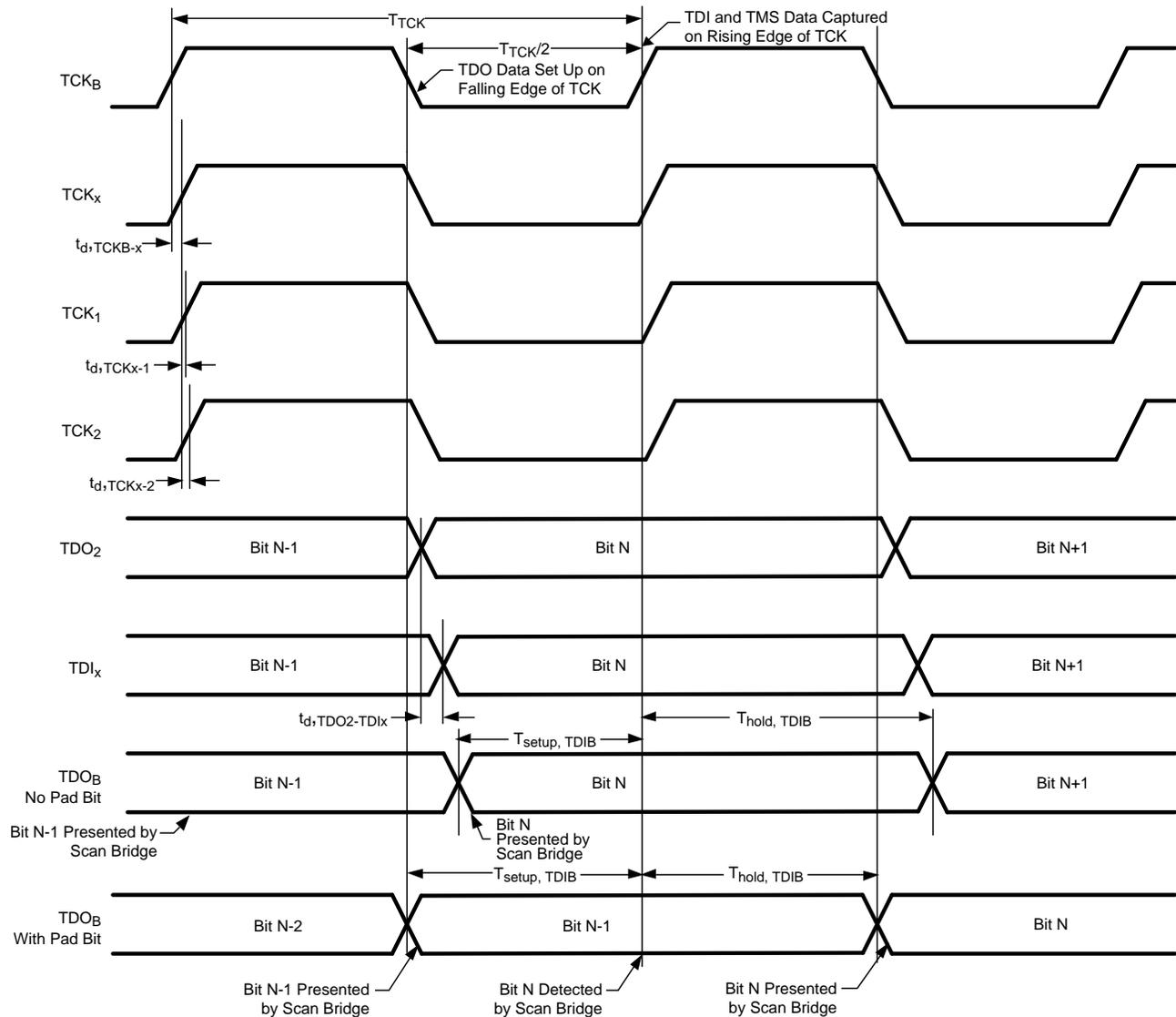
As an example, consider the case where the TCK frequency is 25 MHz. This means that the TCK period T_{TCK} = 40 ns. Also stipulate that there are four devices in the scan chain and that each of the devices is separated from the previous one by six inches of FR-4 board trace with a delay of 1 ns for each trace.

The internal propagation delay from the falling edge of the TCK line to the time when the output of the TDO line is valid differs from device to device. This value might be in the range of 1-2 ns.

For this example, we would compute that the setup time for T_{DI_B} is given by $T_{setup,TDIB} = T_{TCK}/2 - 4 \times t_d - t_{prop, TCK4-TDO4}$. This gives us $T_{setup,TDIB} \approx 14$ ns.

The specified setup time for the SCANSTA101 STA master is 3.5 ns. For the system in this example, the setup time requirements would be satisfied with a significant margin.

When the scan chain is partitioned using a Scan Bridge as shown in Figure 2, an additional delay, which may be significant, is introduced in the TCK line. A timing diagram for a scan chain partitioned using a Scan Bridge is shown in Figure 4.



T_{TCK} = Test Clock Period (for example, 40 ns for a 25 MHz TCK frequency)

$t_{d,TCKB-x}$ = Internal propagation delay, TCK_B to TCK_x

$t_{d,TCKx-1}$ = Board delay, TCK_x to TCK_1

$t_{d,TCKx-2}$ = Board delay, TCK_x to TCK_2

$t_{d,TDO2-TDIx}$ = Board delay, TDO_2 to TDI_x

$T_{setup,Scan Bridge}$ = Setup time available for Scan Bridge

$T_{hold,TDIB}$ = Hold time, TCK_B to TDI_B

$T_{setup,TDIB}$ = Setup time, TDI_B to TCK_B

Figure 4. Partitioned Scan Chain Timing Diagram

The additional delay is the internal propagation delay from the backplane TCK line to the local scan port TCK line. This is shown as $t_{d,TCKB-x}$ in [Figure 4](#).

The Scan Bridge is designed to re-synchronize the local scan port to the backplane TCK line by adding a pad bit to the scan chain. When the pad bit is enabled, the TDO output of the Scan Bridge is re-synchronized to the backplane TCK line as shown in [Figure 4](#). Rather than propagating the bit received on the TDI_x line to the backplane TDO line asynchronously, the Scan Bridge registers the received bit and transmits it to the backplane TDO line synchronously with the falling edge of the backplane TCK line. This results in the transitions of the TDO output of the Scan Bridge occurring at approximately the same time as the falling edge of the backplane TCK line. This is the transition timing specified in the IEEE 1149.1 standard.

3 References

For more details regarding the operation and timing of the SCANSTA111 and SCANSTA112, see the following documentation available at <http://www.ti.com/lscds/ti/analog/interface.page>:

- *SCANSTA111 Enhanced SCAN Bridge Multidrop Addressable IEEE 1149.1 (JTAG) Port Data Sheet* ([SNLS060](#))
- *SCANSTA112 7-Port Multidrop IEEE 1149.1 (JTAG) Multiplexer Data Sheet* ([SNLS161](#))
- *AN-1259 SCANSTA112 Designer's Reference* ([SNLA055](#))

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