AN-2070 AVS Adaptor Board for USB AVS System Mainboards

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The AVS Adaptor Board (AAB) is not intended for standalone use, but rather to enable interconnect of non-PEK/SPEK footprint daughterboards to Texas Instruments PowerWise/SPMI System Mainboards. The AAB provides a means to plug in TI's evaluation boards with the modified DOSA style connector, the proprietary MAK style connector, or the standard 1x9 SIP interface. The AAB provides various power supply options for bench evaluation, and several jumper options to support the desired setup.

2 Evaluation Board Overview

The AAB is, for the most part, a passive board. The vast majority of its functionality is to appropriately route power and signals from the system mainboard and/or bench equipment to the DUT. The only active circuitry on the board is a low-power LDO which can be used to provide the PWI/SPMI I/O signaling voltage. Because of the flexibility designed into the board, you must be very careful with the jumper set-up of the board stack to ensure no damage is done to any of the circuitry. While it would be impossible to cover all combinations of board stacks, great effort will be taken to provide a method/procedure to ensure that the boards can be configured without damaging anything.

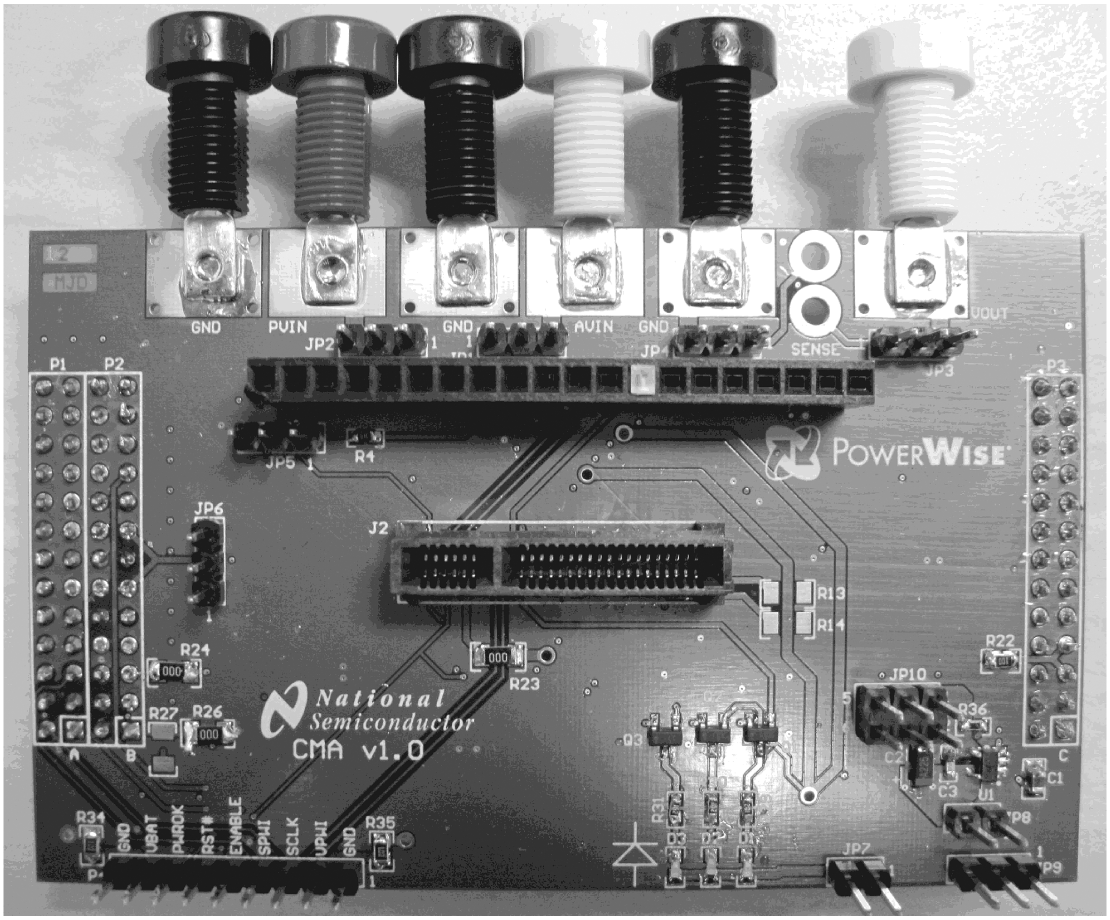

Figure 1. AVS Adaptor Board

3 LM10000 Evaluation Board Quick Start

A typical set up using AAB requires a Texas Instruments AVS System Mainboard, the AAB, and a compliant evaluation board to make up the board stack. The board is driven from a PC with a GUI that is tailored to the evaluation board and DUT. The system mainboard connects to the PC via USB. The board stack can be entirely standalone and powered from USB for quick evaluation/demo purposes, or can be powered from a bench supply for more thorough testing of the regulator(s).

3.1 Basic Setup

1. Set the appropriate jumpers for power supply on the chosen system board. Details of the supply can be found in the documentation for that TI system board.
2. Plug the AAB into the system board..
3. Set the jumpers on the AAB per the following tables.
4. Plug the DUT board into the AAB.
5. Follow the associated documentation for the device you are working with as to power up sequence and special GUI considerations. As a general rule though, you want any external/bench supplies to be on prior to plugging in the USB cable.
6. Plug in the USB cable of the TI system board and follow the documentation pertaining to that device and GUI.

There are many jumper options on the AAB to allow it to perform in as many roles as possible. Great care must be taken in setting up the jumpers prior to applying power to avoid damaging the boards in the board stack. The jumpers and their purpose is explained here:

Jumper	Purpose	Note
JP1	Selects the power source for AVIN. AVIN is typically used to power the power supply's control electronics.	1-2: AVIN is supplied via the system mainboard's "VBAT" input; DEFAULT.
		2-3: AVIN is supplied via the YELLOW banana jack on the AAB.
JP2	Selects the power source for PVIN. PVIN is typically used to power the power electronics of the power supply.	1-2: PVIN is supplied via the system mainboard's "VBAT" input; DEFAULT.
		2-3: PVIN is supplied via the RED banana jack on the AAB.
JP3 (+Sense) and JP4 (-Sense)	Selects either local feedback for the sense lines or remote sense.	1-2: The regulated sense point will be based on the remote sense points labeled "Sense" in the silkscreen.
		2-3: The regulated sense point for the supply will occur at the WHITE banana jack; DEFAULT.
JP5	ENABLE pull-up/pull-down strap.	1-2: ENABLE is pulled-up to AVIN via 10K.
		2-3: ENABLE is pulled-down to GND via 10K.
JP6	Selects the PWI/SPMI sideband (signals other than the 2-wire data and clock) I/O level reference.	1-2: Referenced to the "VBAT" supply from the system board; depends on what that supply is set to.
		2-3: Referenced to the same voltage as the PWI/SPMI signals, "VPWI"; DEFAULT.
JP7	LED supply On/Off. The LEDs are powered from the system board "VBAT".	On: With the jumper installed, the LED indicators will be functional; DEFAULT.
		Off: LEDs are disabled.
JP8	Short out on-board "VPWI" regulator.	On: U1, the "VPWI" LDO will be shorted. This will make "VPWI" equal to the system board "VBAT".
		Off: "VPWI" can be generated on-board or elsewhere; DEFAULT.
JP9	'VPWI" regulator On/Off.	1-2: "VPWI" LDO is enabled; DEFAULT.
		2-3: "VPWI" LDO is disabled.
JP10	'VPWI" regulator output voltage selection.	1-2: 3.3V; DEFAULT.
		3-4: 2.5V.
		5-6: 1.8V.

3.2 Interconnects

There are several ways to connect to/from the AAB board. The board will nearly always be paired with a system mainboard that will connect via P1, P2, and P3. These are male pin headers on the bottom side of the board that allow the board to plug down into the standard mainboard footprint. The AAB itself then breaks out the required power and signal traces to the appropriate locations on the interconnects.

J1 is the modified DOSA-style interconnect. It leverages the DOSA Standard for Non-Isolated 9.6 – 14.4VIN, 15/16/20A DC/DC converters. It is completely backwards compatible with existing DOSA style parts, but expands upon the connector footprint to add in PWI/SPMI functionality. The pinout is in the below table:

DOSA Pin Number	AAB Pin Number	Function
1	1	VOUT
2	2	VOUT
3	3	SENSE
4	4	VOUT
5	5	GND
	6	GND
	7	GND
	<<KEY>>	Mechanical Key
	8	SCLK
	9	SPWI
	10	VPWI
	11	AVIN
	12	PGOOD
A	13	I Share - Not Routed
6	14	GND
7	15	VIN
8	16	VIN
B	17	SEQ - Not Routed
9	18	TRIM - Not Routed
10	19	ON/OFF

J2 is the “MAK” connector that is utilized to connect to a few TI DUT boards. It is a vertical edge-card socket strip. Its use is relegated to a couple of very specific applications and will not be detailed here. For further details, see the device-specific schematics and DUT documentation.

The last major connector is P4. This 1x9 SIP connector has been on the vast majority of TI AVS products for several years. It allows a convenient means to access most of the major signals involved in the PWI/SPMI interface, and can also be used to cable across to an external AVS setup to provide the proper signaling environment. The P4 pinout is found in the following table:

Pin Number	Function	Description
1	GND	System ground
2	VPWI	VPWI voltage
3	SCLK	Serial clock
4	SPWI	Serial data
5	ENABLE	Regulator enable
6	RST#	Regulator reset (active low)
7	PWROK	Regulator output of power okay indicator
8	VBAT	Mainboard “VBAT” voltage
9	GND	System ground

3.3 Indicator LEDS

When JP7 is ON and the indicator LEDs are enabled, they have the following functionality:

Ref Des	Color	Description
D1	Red	AVIN is powered up
D2	Yellow	VPWI is powered up
D3	Green	The PWROK signal is driven high

- R26 and R27 can be used either as a voltage divider for the output voltage or as a RC for the ADC converter on the system mainboard. By default, R26 is shorted and R27 is open, but you can mount these as desired. You must ensure that the VOUT fed back to the mainboard does NOT exceed 3.3V for the USB Interface Board or 1.8V for the PEK/SPEK. VOUTs above this should be divided down to appropriate levels.
- If “VPWI” is provided externally by you in some fashion, care should be taken to disable U1 (set JP9 to 2-3) and open JP8. Additionally, you should make sure that the provided “VPWI” does NOT exceed the mainboard “VBAT” by more than 1 diode drop or current may flow from “VPWI” to “VBAT”. “VBAT” is dependent upon the system board used and the settings applied to it.

4 Bill of Materials (BOM)

Table 1. Bill of Materials (BOM)

Qty	Designator	Value	Description	Mfg. P/N
1	AVIN	Yellow Banana Jack	Yellow Nylon Banana Jack	Emerson 108-0907-001
1	C1	1µF/35V/X7R	VPWI C_{IN}	T-Y GMK212B7105KG-T
1	C2	2.2µF/10V/20%/Tant	VPWI C_{OUT}	Nichicon F931A225MAA
1	C3	7pF/50V/C0G	VPWI Feedback Bypass	TDK C1608C0G1H070D
1	D1	LS L29K-H1J2-1-Z	Red LED for AVIN Indicator	OSRAM LS L29K-H1J2-1-Z
1	D2	LY L29K-J1K2-26-Z	Yellow LED for VPWI Indicator	OSRAM LY L29K-J1K2-26-Z
1	D3	LG L29K-G2J1-24-Z	Green LED for PGOOD Indicator	OSRAM LG L29K-G2J1-24-Z
3	GND, GND2, GND3	Black Banana Jack	Black Nylon Banana Jack	Emerson 108-0903-001
1	J1	DOSA Receptacle	1x20 100-mil Receptacle	Tyco 6-534237-8
1	J1-Key	DOSA Receptacle Key	Key to make pin 8 inaccessible	Tyco 86286-1
1	J2	Samtec HSEC8	MAK Connector Receptacle	Samtec HSEC8-125-01-S-DV-A
7	JP1, JP2, JP3, JP4, JP5, JP6, JP9	1x3, 100-mil Header	1x3 100-mil Jumper	Molex 90120-0763
2	JP7, JP8	1x2, 100-mil Header	1x2 100-mil Jumper	Molex 90120-0762
1	JP10	2x3, 100-mil Header	VPWI Voltage Select Jumper	Molex 90131-0763
3	P1, P2, P3	A28694-ND	Baseboard Connectors	Tyco 1-87227-3
1	P4	1x9, 100-mil Header	1x9 PWI Access Header	Molex 90120-0769
1	PVIN	Red Banana Jack	Red Nylon Banana Jack	Emerson 108-0902-001
3	Q1, Q2, Q3	NDS331N	Logic NFET	Fairchild NDS331N
4	R1, R22, R34, R35	10R/0.25W/5%	Fuse Rs	Rohm ESR10EZPJ100

Table 1. Bill of Materials (BOM) (continued)

Qty	Designator	Value	Description	Mfg. P/N
2	R2, R3	1.5K/0.1W/1%	Presence Detect Rs	Rohm MCR03EZPFX1501
2	R4, R9	10K/0.1W/1%	ENABLE P-U/P-D	Stackpole RMCF 1/16 10K 1% R
18	R5, R6, R7, R8, R10, R11, R12, R15, R16, R17, R18, R19, R20, R21, R23, R24, R25, R26	0R/0.25W	Pad shorts	Vishay CRCW12060000Z0EA
3	R13, R14, R27	No Load	Open pads	N/A
1	R28	53.6K/0.1W/1%	2.5V VPWI Divider R	Panasonic ERJ-3EKF5362V
3	R29, R30, R31	1.6K/0.1W/1%	LED Current Limit R	Yageo RC0603FR-071K6L
1	R32	86.6K/0.1W/1%	3.3V VPWI Divider R	Panasonic ERJ-3EKF8662V
1	R33	24.0K/0.1W/1%	1.8V VPWI Divider R	Panasonic ERJ-3EKF2402V
1	R36	51.1K/0.1W/1%	LS VPWI Divider R	Panasonic ERJ-3EKF5112V
2	TP1, TP2	No Load	Remote Sense pads	N/A
1	U1	LP2980	VPWI Adjust LDO	Texas Instruments LP2980
1	VOUT	White Banana Jack	White Nylon Banana Jack	Emerson 108-0901-001
9	Jumper Shunts -- Installed Per Golden Sample	1x2 Shunt	Jumper	Sullins SPC02SYAN

5 Layout Artwork

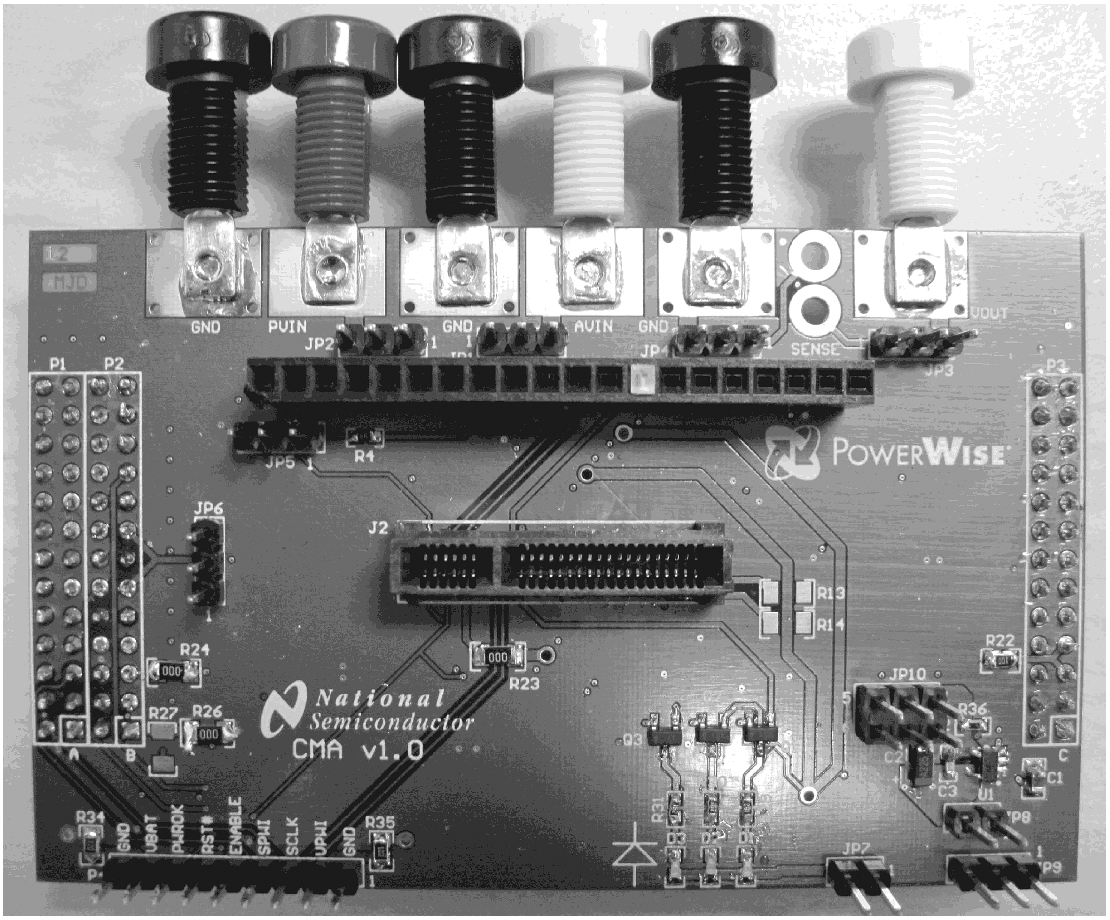

Figure 2. Evaluation Board (Top View)

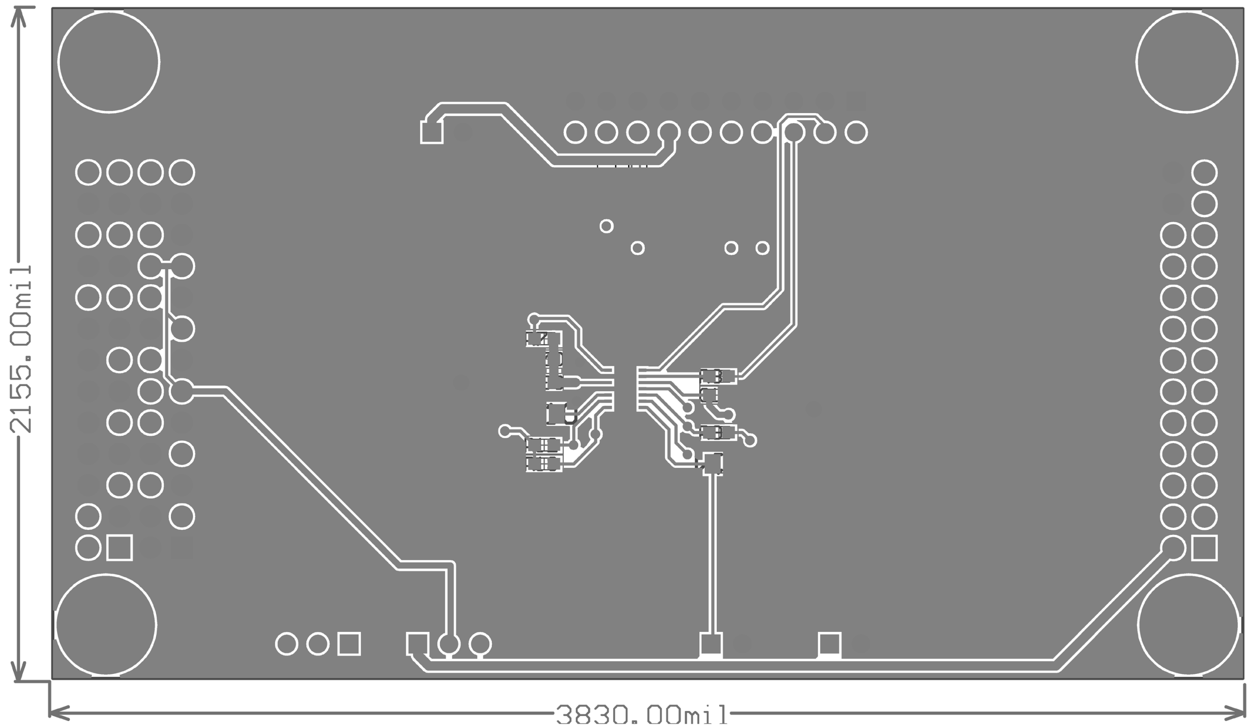

Figure 3. Top Layer

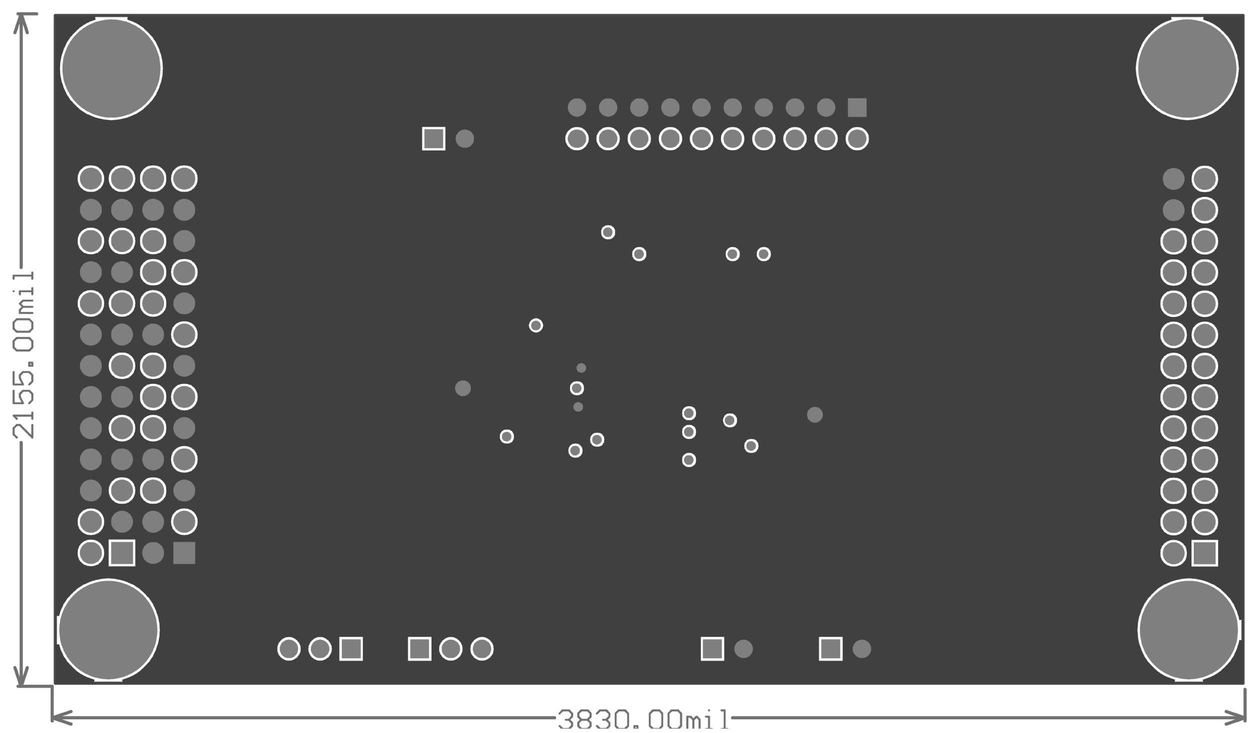

Figure 4. Mid-Layer 1

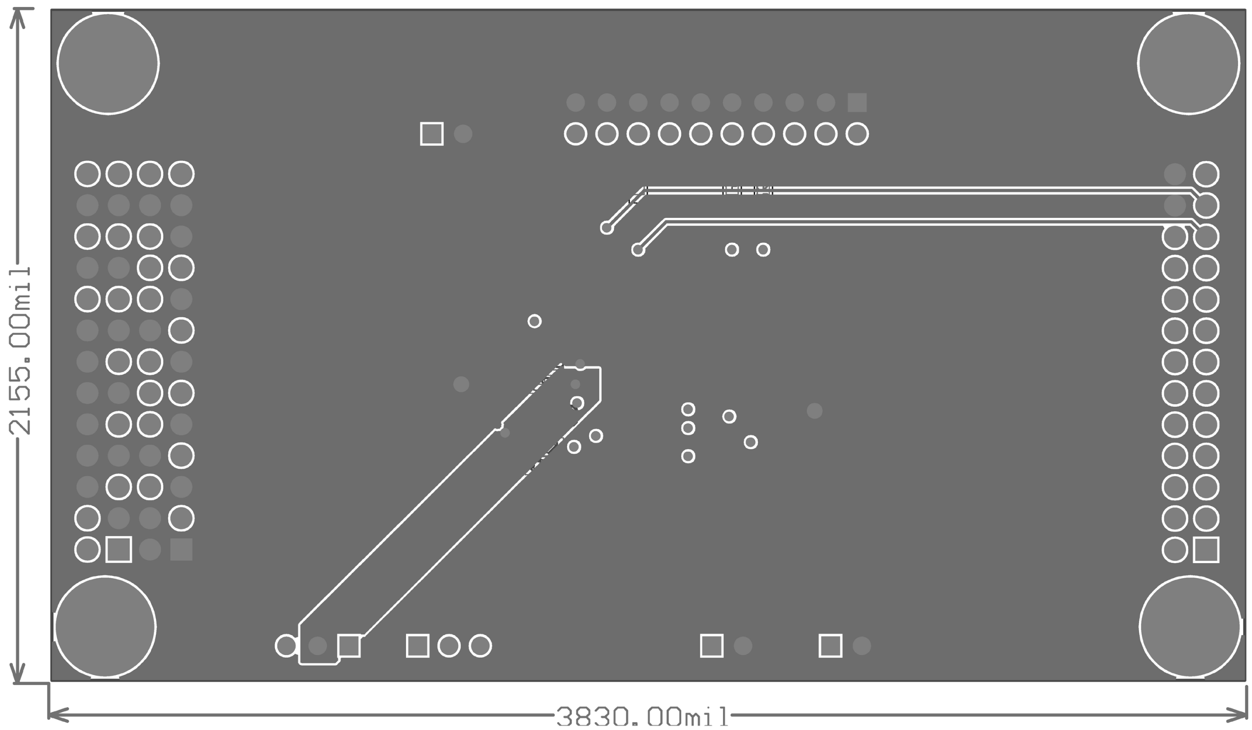

Figure 5. Mid-Layer 2

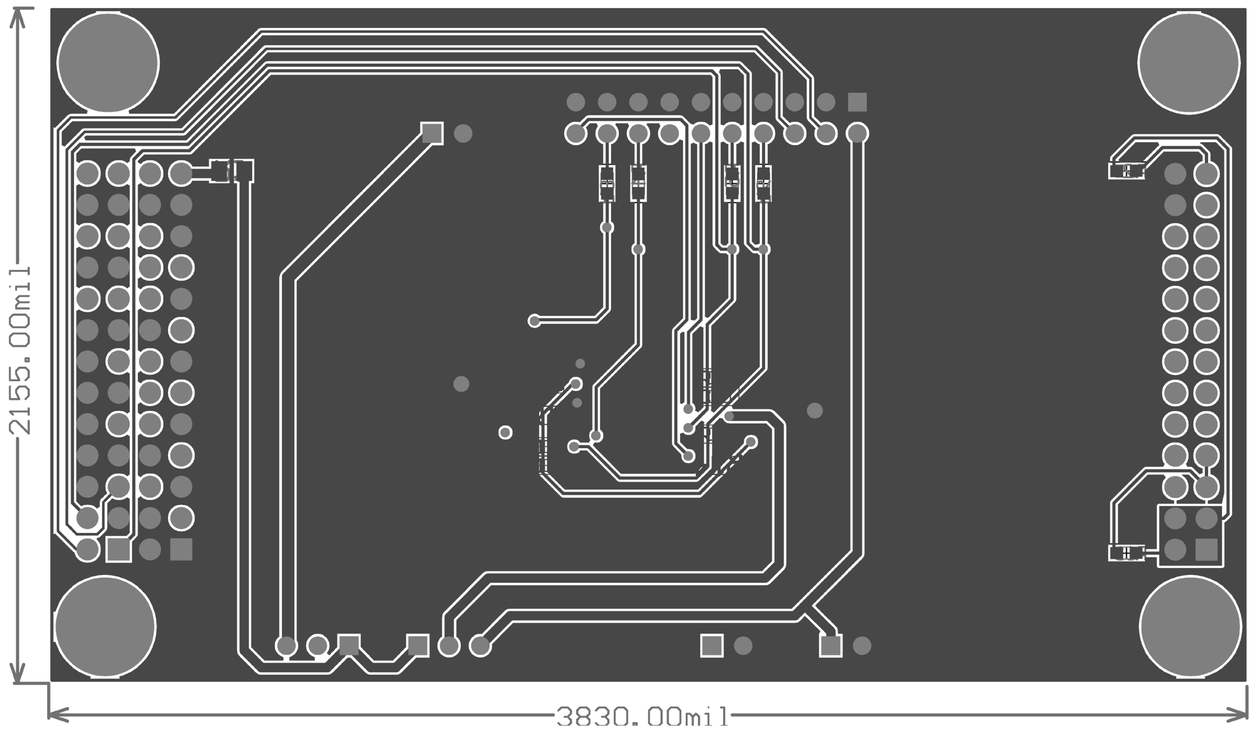

Figure 6. Bottom Layer

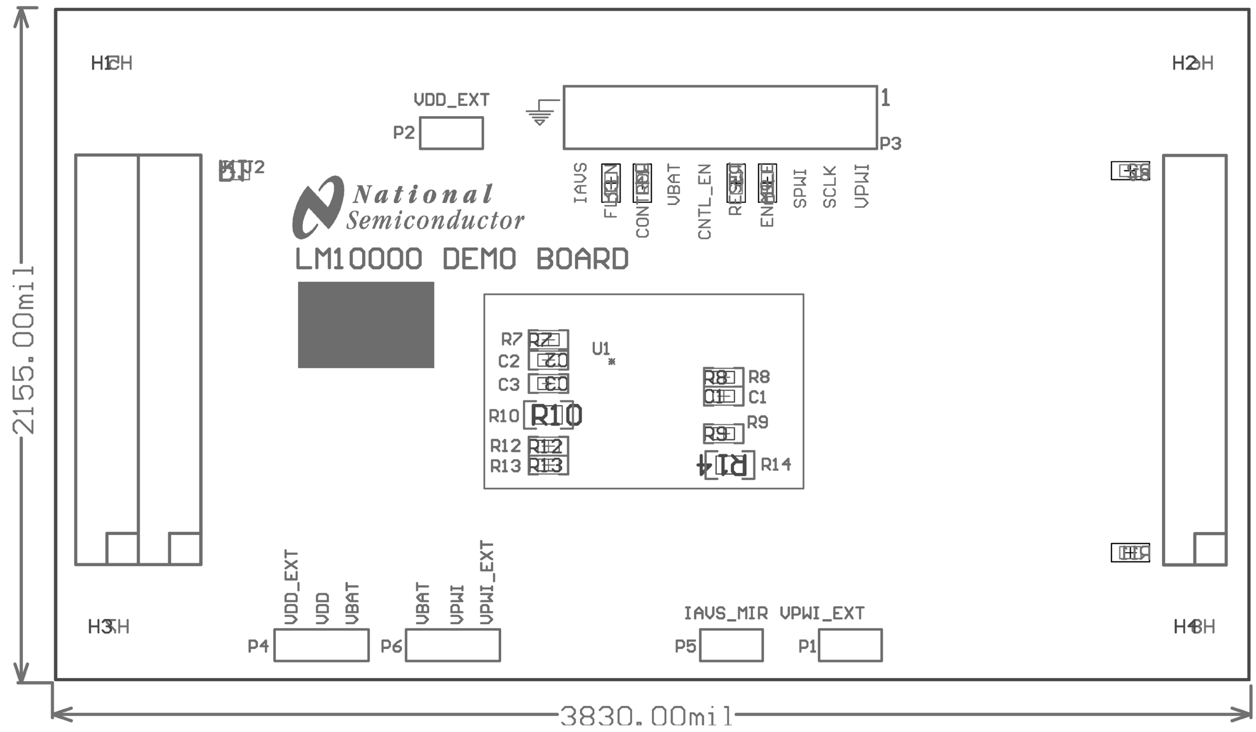

Figure 7. Top Silk Screen

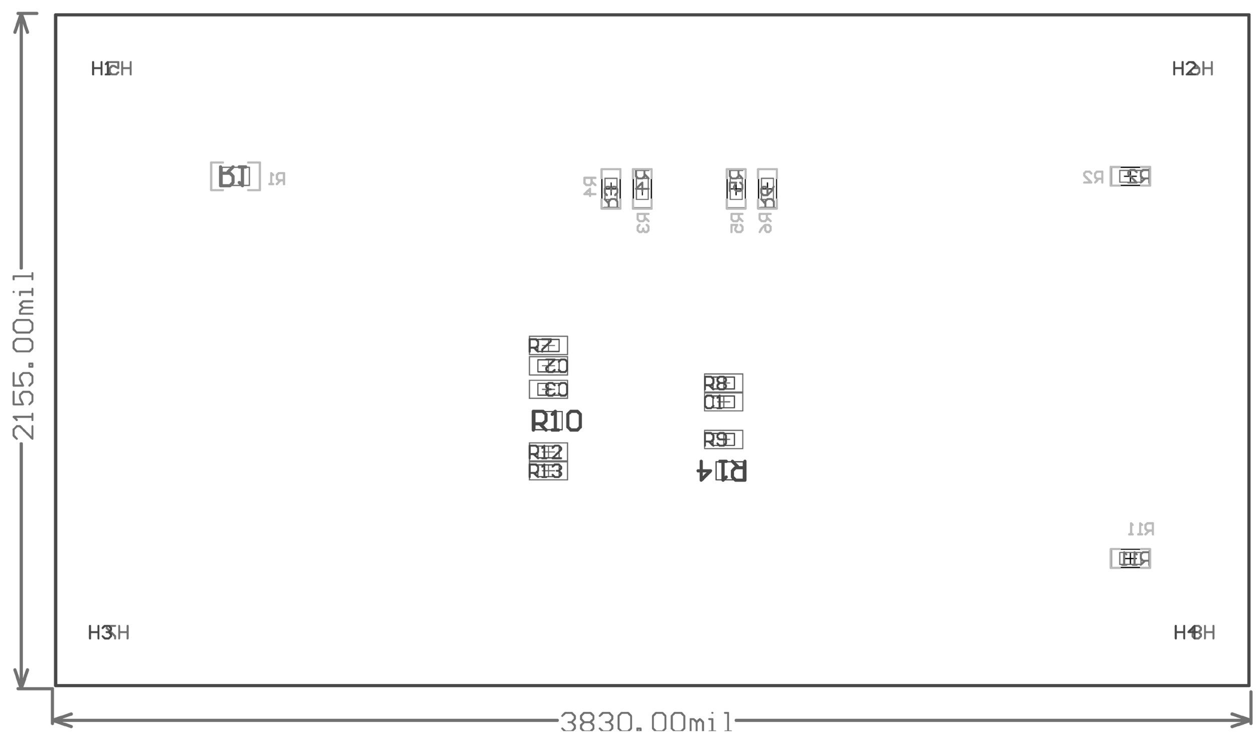

Figure 8. Bottom Silk Screen

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