Thermal Issues and Solutions in Power Management

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Featured Products

Industry's First High Power Density 1A SOT-23 Buck Switching Regulators

The LM2734 and LM2736 are monolithic, high-frequency (550 kHz and 1.6 MHz), PWM step-down DC-DC converters in six-pin, thin SOT-23 packaging.

With a minimum of external components and support through WEBENCH® online design tools, the LM2734/36 are easy to use. The control circuitry allows for on-times as low as 13 ns, thus supporting exceptionally high frequency conversion over the entire 3V to 20V input operating range down to the minimum output voltage of 0.8V. Switching frequency is internally set to 550 kHz (LM2734Y), 1.6 MHz (LM2734X), or 3.0 MHz (LM2734Z), allowing the use of extremely small surface-mount inductors and chip capacitors. External shutdown is included, featuring an ultra-low stand-by current of 30 nA. The LM2734/36 utilize current-mode control and internal compensation to provide high-performance regulation over a wide range of operating conditions.

Features

- 3.0V to 20V input voltage range
- 0.8V to 18V output voltage range
- 1A output current
- 550 kHz (LM2734Y), 1.6 MHz (LM2734X), and 3.0 MHz (LM2734Z) switching frequencies
- Internal soft-start
- WEBENCH® design tools available
- Available in thin SOT23-6 packaging

The LM2734/36 are ideal for use in local point-of-load regulation, core power in HDDs, set-top boxes, battery-powered devices, USB-powered devices, DSL modems, and notebook computers.

www.national.com/pf/LM/LM2734.html
www.national.com/pf/LM/LM2736.html

100V Power MOSFET Drivers

The LM5100/01/05/07 high-voltage gate drivers are designed to drive both the high-side and the low-side N-Channel MOSFETs in a synchronous-buck or half-bridge configuration. The floating high-side driver is capable of operating with supply voltages up to 100V. The outputs are independently controlled with CMOS-input thresholds (LM5100) or TTL-input thresholds (LM5101/05/07). An integrated high-voltage diode is provided to charge the high-side gate drive bootstrap capacitor. A robust level-shifter operates at high speed while consuming low power and providing clean level transitions from the control logic to the high-side gate driver. Under-voltage lockout is provided on both the low-side and the high-side power rails.

Features

- Drives both a high-side and low-side N-channel MOSFET
- Independent high-and low-driver logic inputs
- Bootstrap supply-voltage range up to 118V DC
- Fast propagation times (25 ns typical)
- Drives 1000 pF load with 15 ns rise and fall times
- Available in SOIC-8, LLP-8, and LLP-10 packaging

These devices are ideal for use in cascade current-fed or voltage-fed converters, half- and full-bridge power converters, high-voltage buck DC-DC converters, solid-state motor drivers, and solid-state solenoid drivers.

www.national.com/pf/LM/LM5100.html
www.national.com/pf/LM/LM5101.html
www.national.com/pf/LM/LM5105.html
www.national.com/pf/LM/LM5107.html

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DESIGN | *idea*

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Thermal Issues and Solutions in Power Management

Power converter design is a multi-disciplinary process; an effective designer needs to understand analog and mixed-signal circuit design, wound components, electromagnetic compatibility, packaging, and thermal design. Packaging and thermal design are driven by increased power density and the many trade-offs in power topology selection. The challenging environment in equipment destined to power the expanding information infrastructure brings thermal design into sharp focus.

The world of modular DC-DC converters or “bricks” is evolving at a rapid pace since the first full-brick was commercialized in the mid-eighties. For instance, the sixteenth-brick format is 1.2 square inches of PCB area with a staggering 33W to 50W throughput.

The telecom bus operates over a wider range, 36V to 72V, than its datacom counterpart that has a tighter tolerance. A bus converter converts this bus with isolation at each card (the first use of the brick format). The on-card power is then applied directly to the load circuits. However, in recent years the proliferation of DSP and digital ASICs has spawned an intermediate bus architecture in which the bus converter delivers an isolated 12V to 14V, which is further converted by point-of-load regulators, physically located at the loads on the card.

Once the power supply designer has selected the topology to match the application, considered the number of power conversion stages[1] and whether the converter is hard- or soft-switched, then the switch and rectifier selection takes center stage. Most bricks employ power MOSFETs for the power switches and low-voltage synchronous rectifiers. MOSFET technology has evolved considerably, presenting the designer with trench devices with benchmark R_{DS-ON} and planar devices with low inter-electrode capacitance. Device selection, once the voltage and current rating has been established, depends on which characteristic, switching speed or R_{DS-ON} dominates the loss. In recent times the ratio of C_{DG} to C_{GS} has influenced designers as an indicator of the likelihood of shoot-through in high-power, high-frequency, half-bridge power stages.

Switching Frequency & EMI Trade-offs

A perennial trade-off is that of switching frequency with efficiency and electromagnetic interference. Switching losses in the power switches, rectifiers and control circuitry increase with switching frequency. In modular DC-DC converters, increasing frequency is desirable as it drives down the size of the filter and energy storage components. However in hard-switched applications, the increased high-frequency harmonic content in the power devices results in larger displacement currents in the stray capacitances between devices and heat sinks or power planes, and through the interwinding capacitance of transformers. Such displacement currents manifest themselves as common-mode interference.

In DC-DC converter control and drive applications, IC design and packaging has embraced the challenge presented by the brick environment. At the circuit-design level, increased integration, in-board, high-voltage regulators, higher clock frequencies and low shoot-through drivers with programmable slew rate are available for new designs[2]. A key issue in power IC design is that of thermal regulation. Power ICs have integrated drivers, regulator pass transistors and power switches arranged at the periphery of the die next to the bond pads. As these devices operate, heat conducts through the body of the die creating a thermal “map” with isotherms (contour lines of constant temperature). Certain sub-circuits, particularly differential circuits where matching is critical, are adversely affected if the individual transistors are positioned on different isotherms. IC layouts must be adjusted such that transistors in such applications see the same temperature, at the same time, when the device is operating, which is not a trivial task. Photomicrographs of power ICs often reveal devices that are cross-coupled for first-order cancellation of thermal effects.

Figure 1. Top and bottom view of an LLP

The LLP® leadless leadframe package, shown in ***Figure 1***, is a leadframe-based chip scale package (CSP) that enhances chip speed, reduces thermal impedance, and reduces the printed circuit board area required for mounting. The small size and very low profile make this package ideal for the high component density, multi-layer PCBs used in modular DC-DC converters.

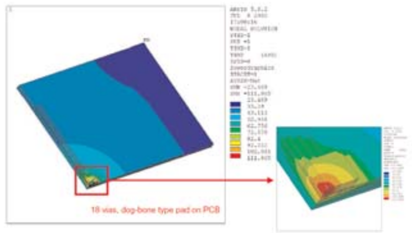

Figure 2. Finite element plot of an LLP

The LLP has the following advantages:

- Low thermal resistance
- Reduced electrical parasitics
- Improved board space efficiency
- Reduced package height
- Reduced package mass

IC package design is a painstaking process involving extensive thermal and mechanical modeling coupled with fabrication and measurement stages in which finite element models (as shown in *Figure 2)* are compared with spot measurements on the die or by thermal imaging. Generally spot measurements on the die are accomplished by measuring the forward drop of a diode in a test die incorporated within the new package. This tried and tested technique is used in many of the remote diode temperature-sensing devices[3] that protect the latest generation of microprocessors, DSPs and digital ASICs. One or more diodes in the test die may also be used to inject heat to verify the thermal characteristics of the die.

Package Design & Thermal Properties

Thermal properties of electronic packages[4] are characterized by θ_{JA} and θ_{JC}. θ_{JA} can be defined as an overall package thermal resistance, which is the sum of package internal and external thermal resistance. It can be expressed as:

$$\theta_{JA} = \theta_{JC} + \theta_{CA} = (T_J - T_A)/P$$

Where:

θ_{JC}: $(T_J - T_C)/P$, junction-to-case conductive thermal resistance (°C/W)

θ_{CA}: $(T_C - T_A)/P$, case-to-ambient convective thermal resistance (°C/W)

P: I (current) x V (voltage), device heat dissipation (W)

T_J: Average device junction temperature (°C)

T_A: Average ambient temperature (°C)

T_C: Case temperature at a prescribed package surface (°C)

θ_{JC} is dominated by the conductive thermal resistance within layers of packaging materials, and is highly dependent on the package configuration. If the heat flow is assumed to be perpendicular to each layer of the packaging material, θ_{JC} may be expressed as:

$$\sum t_i/(k_i A_i)$$

Where t_i, k_i, and A_i are the thickness, thermal conductivity, and heat transfer surface area of each packaging material layer, e.g., die-attach material, lead frame, die coating, and encapsulant or mold compound.

θ_{CA} is the external convective thermal resistance. It is greatly affected by adjacent ambient conditions, package boundary conditions, and conjugate heat transfer. In the LLP, low junction to ambient thermal resistance is primarily affected by reducing the resistance from the thermal plane on the PCB to the junction. The cross-section in *Figure 3* shows that the die is soldered to the die-attach pad, which is directly soldered to the power plane on the PCB. The area of the PCB power plane dominates θ_{CA}, in brick applications where conduction is the primary method of heat transfer and convection cooling is restricted due to the diminishing pitch between cards.

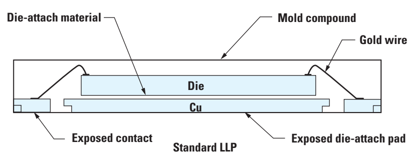

Figure 3. Cross-section of an LLP

Packaging Comparisons

The θ_{CA} may be improved by utilizing thermal vias in the power plane under the device. This improvement is second order compared with that achieved by increasing the area of the plane to which the LLP is soldered. A comparison between the LLP and a conventional small-outline package with the same pin count and die reveals the benefits.

Let's take an MSOP-8, where the PCB area is 15 mm^2 compared to an LLP-8 which is 9 mm^2. The dramatic difference is in the thermal resistance where the LLP-8 exhibits a thermal resistance (θ_{JC}) of 40°C/W versus 200°C/W for the MSOP-8.

In conclusion, a modular DC-DC converter is a most demanding environment for power ICs. The inexorable push to higher power density and the necessity for higher-efficiency drives power IC and package designers to set new standards in thermal resistance and volumetric efficiency. Giving power supply designers a brief glimpse into the package design, measurement and verification process is an important part of launching a new standard, particularly in power applications where new discrete power packages are a frequent part of the landscape. ■

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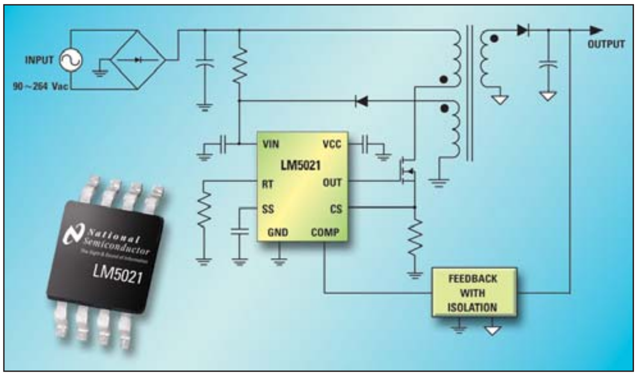

AC-DC Current-mode PWM Controller

The LM5021 off-line pulse width modulation (PWM) controller contains all of the features needed to implement highly efficient off-line single-ended flyback and forward power converters using current-mode control. The LM5021 features include an ultra-low (25 µA) start-up current, which minimizes power losses in the high-voltage start-up network. A skip-cycle mode reduces power consumption with light loads for energy-conserving applications (such as ENERGY STAR®, CECP). Additional features include under-voltage lockout, cycle-by-cycle current limit, hiccup-mode overload protection, slope compensation, soft-start and oscillator synchronization capability. This high-performance, 8-pin IC has total propagation delays less than 100 nS and a 1 MHz-capable oscillator that is programmed with a single resistor.

Features

- Ultra-low start-up current (25 µA maximum)
- Current mode control
- Skip-cycle mode for low standby power
- Single-resistor programmable oscillator
- Synchronizable oscillator
- Available in MSOP-8 and MDIP-8 packaging

The LM5021 is ideal for use in off-line, telecommunication, and consumer applications.

www.national.com/pf/LM/LM5021.html

800 mA Sub-bandgap Low-noise Adjustable Voltage Regulator

The LP3878-ADJ is an 800 mA adjustable output voltage regulator designed to provide high-performance and low-noise in applications requiring very low-output voltages. Output noise is typically 18 µV with a 10 nF capacitor to the bypass pin.

Using an optimized VIP (Vertically Integrated PNP) process, the LP3878-ADJ delivers superior performance including ground pin current that is typically 5.5 mA at 800 mA load, and precision 1% output voltage accuracy at room temperature. In addition, when the shutdown pin is pulled low, quiescent current is less than 10 µA.

Features

- Input voltage range 2.5V to 16V
- Adjustable output voltage range 1.0V to 5.5V
- 475 mV dropout (typ.) at 800 mA (V_{OUT} = 3.8V)
- Designed for use with low ESR ceramic capacitors
- 18 µV (typical) output noise
- <10 µA quiescent current in shutdown
- 1% V_{OUT} accuracy at room temperature
- -40°C to +125°C operating temperature range
- Over-temperature /over-current protection
- Available in PSOP-8 and LLP-8 packaging

The LP3878-ADJ is ideal for use in medical instrumentation, ASIC power supplies: in desktops, notebooks, and graphics cards; in set-top boxes, printers and copiers; in DSP and FPGA power supplies; and in SMPS post-regulators.

www.national.com/pf/LP/LP3878-ADJ.html

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