

TMS320C6000 Board Design: Considerations for Debug

David Bell

Digital Signal Processing Solutions

ABSTRACT

This document discusses printed circuit board design issues relative to the Texas Instruments TMS320C6000[™] platform of digital signal processors (DSPs).

As the sophistication of DSP board design increases, it is important to incorporate debug features into a design. Visibility into the system is important to be able to identify what is going wrong and how. Different levels of visibility may be achieved by providing emulator support to see into the DSP, JTAG support to examine IC interconnect, and signal probe points to view signal waveforms. Simplicity is the key to quickly debugging a board. A sophisticated system may be simplified through isolation of complicated subsystem areas and by providing a default state with a manual system reset. Flexibility allows more debug options. This can be built into a system with the use of configuration switches to provide different operating modes and by providing sockets to allow for upgrading silicon. Taking these steps will allow for a more efficient debug process.

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TEXAS INSTRUMENTS

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1 Introduction

One critical element to board design that is often overlooked is the ease of board verification. As systems become more sophisticated, properly debugging a new board requires planning during its design. By taking a few precautions and designing in a few added features, the debug process can be greatly simplified and will not require excessive time and resources.

Several concepts should govern the design of a new board are:

- Visibility;
- Simplicity; and
- Flexibility

Keeping these concepts in mind during system development saves time during the testing of the board.

2 Visibility Lets You Identify What Is Going Wrong and How

It is critical to have visibility into the system to understand what is going on between (and within) the components on the board. Visibility into a device may be done with emulation/debugger software. The interconnection of the IC components on a board may be verified through JTAG boundary scan. A logic analyzer or oscilloscope may view the intercommunication of the components if probe points are provided on all critical signals.

2.1 Emulator Support Allows Visibility Into the DSP

The most obvious requirement to provide visibility into a system is to use the Texas Instruments emulation software through the JTAG port. This provides a real-time debugging environment on which to develop the system software. The Code Composer[™] debugger environment allows visibility into all internal registers and memory locations of the C6000[™] device (or any other TI DSP)[†]. In addition, there is extensive code debugging functionality available through this software. JTAG emulation for the C6000 device platform is described in the *TMS320C6000 Peripherals Reference Guide* (SPRU190).

2.2 JTAG Support Enables the Use of Boundary Scan Verification

Many other devices that may be used in the system are also JTAG compliant and may also have software available to gain internal visibility. Boundary scan tests may be performed on JTAG-compliant devices to ensure that they are functional and properly configured on a board. The following companies offer boundary scan software and hardware:

- ASSET Intertech, Inc.
- Corelis, Inc.
- JTAG Technologies B.V.
- Göpel Electronic GmbH

Companies that provide JTAG-compliant devices should provide Boundary Scan Description Language (BSDL) models for the generation of test vectors. For information on obtaining TI's BSDL models, go to the TI web site at http://www.ti.com.

Code Composer and C6000 are trademarks of Texas Instruments.

[†] For a complete list of Texas Instruments DSP devices, go to the TI web site at http://www.ti.com

The C6000 platform of devices has several emulation pins included with the JTAG signals (EMU*x*). For use with the emulation environment, it is required that these signals be pulled up to V_{CC} with external resistors. These EMU signals should be pulled down for boundary scan; therefore, it is advised that, on systems supporting both emulation and boundary scan, these signals should be pulled to power or ground through a switch or jumpers. Figure 1 depicts the desired JTAG connection to a C6000 device.



Figure 1. TMS320C6000 JTAG Connection

2.3 Signal Probe Points Allow Signal Waveforms to Be Captured

To ensure that the board components are properly communicating with one another, test points and signal headers should be placed on important signals. The only way to understand why devices are not communicating properly is to verify that all signals transition according to the specifications provided in each device's datasheet. The use of headers allows signals to be captured and viewed by a logic analyzer, which can then measure the relationships between signal transitions.

The ability to effectively use a logic analyzer and oscilloscope to monitor system behavior is crucial. Although requiring board space, headers allow the board to be easily monitored by a logic analyzer without having to probe individual signals by hand. Test points should be placed on signals that may need periodic verification, such as power and ground, so that voltage levels and signal integrity can be observed. An excellent logic analyzer header is the Matched Impedance Connector (MICTOR) available from Amp, Inc. (part #767054-1). Logic analyzer cables that connect to MICTOR receptacles are available for Tektronix and Hewlett Packard logic analyzers.

3 Simplicity Is the Key to Quickly Debugging a Board

A majority of C6000 systems contain a high level of complexity. To simplify the debug process, a complex system should be designed such that portions may be verified independently of the rest of the system. If portions of the system can be localized into independent blocks, then they can be quickly tested before the system is verified as a whole. A manual reset can provide a means to force the system into a known default state.

3.1 Isolation of Complicated System Areas Simplifies Debug

A system should be broken up into blocks that can be isolated for test. Ideally, each portion of the system should be independently testable. For example, incoming serial streams should be testable without verifying that the external memory communication is functioning, and the external memory interface should be testable without testing a complicated shared memory scheme.

In systems that have a host controlling the DSP(s), it is useful to be able to disconnect the host and manually load code using the debugger. In this way, the DSP code may be debugged separately from the host interface. This "disconnecting" could be as simple as changing the boot mode with configuration switches.

3.2 Manual Reset Provides Default State

A system reset should be provided with a pushbutton to allow a hard reset if needed. During early testing, it may be possible to get various system components in an undesirable state. Having a manual reset is a simple way to initialize the system. A simple reset circuit using TI's TLC7733IPWLE[†] supply voltage supervisor is shown in Figure 2. The TLC7733 provides a reset signal to the DSP when the pushbutton switch is depressed, as well as when the voltage level drops below a threshold voltage of 2.93 V. The minimum pulse width of the RESET# low is determined by the capacitor C1.



Figure 2. Reset Circuit Using TLC7733IPWLE

4 Flexibility Allows More Debug Options

A DSP board should be designed to be flexible to allow testing in multiple DSP modes, and to facilitate new silicon as it becomes available. By configuring the board through switches rather than dedicated pullup/pulldown resistors, it is possible to change system settings during the debug process to get around obstacles. Using sockets for the DSPs (or other complicated components) in a system allows preliminary silicon to be used for system development, with the capability of migrating to custom parts as they become available.

⁺ For information on the TLC7733 family of supply voltage supervisors, go to to the TI web site at http://www.ti.com

4.1 Configuration Switches Enable Debugging in Different Modes

TMS320C6000 DSPs are configurable to run in different modes. Although a system only requires a specific setup for its application, it is beneficial to provide a means to operate in different modes during debug. This may be accomplished by providing switches (or jumpers) to select different settings. All C6000 DSPs have three primary configuration inputs that determine functionality:

- **BOOTMODE signals:** determine the memory map and boot process of the DSP. By having selectable boot modes, the device may be initialized without a specified boot process, even though one will be specified for the final system. This feature can overcome any problems in the off-chip components (ROM or Host) required for boot. During the initial stages of debug, code can be loaded directly into the DSP using the JTAG interface rather than through a boot process, allowing for the boot process to be debugged separately from the rest of the system.
- **LENDIAN signals:** determine in which endian mode the DSP will operate. Endianness selection allows interoperability with either little- or big-endian systems.
- **CLKMODE signals:** select the PLL frequency multiplier. The clock mode select option is useful to debug portions of the system by running at a very slow clock rate. This capability will circumvent any problems relating to timing delays on the signals.
- Specific devices from the C6000 platform may also have additional configuration signals available. Figure 3 shows the desired pullup/pulldown connection of a configuration pin.



Figure 3. TMS320C6000 Configuration Layout

4.2 Sockets Allow Silicon Upgrading

Another useful practice is to socket the DSP. Sockets should be used with identical footprints so that the same board can be used in production. Since the DSP is probably the most complicated component in the board, providing a socket is a way to isolate it from the rest of the system. A socket allows the system to use updated silicon as it becomes available. A socket also allows the board to be tested without concern for proper mounting of the device.

A DSP socket can also increase the life span of a board. Future devices of the C6000 platform may be offered in pin-compatible packages, which would allow a current board to be used to work with new devices as they become available.

Due to the high frequency of operation used by TMS320C6000 devices, sockets must be of extremely high quality. The pin inductance introduced by a socket must be 2 nH or less. Table 1 lists pin-compatible custom sockets for all TMS320C6000 devices. Among others, companies that offer custom made sockets for TMS320C6000 devices are Advanced Interconnections Corporation, Gold Technologies Incorporated, and Aries Electronics Incorporated.

Socket Part Number	Package	BGA Suffix	Company	Texas Instruments Inc. DSP Device
TSG256-690GGYC	GFN 256-pin BGA	GFN (S-PBGA-N256)	Advanced Interconnect Inc.	TMS320C6211/C6211B, TMS320C6711/C6712
S309-M-BGA080	GHK 288-pin BGA	GHK (S-PBGA-N288)	Gold Technologies Inc.	TMS320C6204/C6205
S384-M-BGA080	GLW 340-pin BGA GLS 384-pin BGA	GLW (S-PBGA-N340) GHK (S-PBGA-N288)	Gold Technologies Inc.	TMS320C6204/C6205 (GLW), TMS320C6202/C6202B/ C6203 (GLS)
TSG352-690GGYC	GJC 352-pin BGA	GJC (S-PBGA-N352)	Advanced Interconnections Inc.	TMS320C6201/C6207 (GJC)
S352-M-BGA127	GJL 352-pin BGA	GJL (S-PBGA-N352)	Gold Technologies Inc.	TMS320C6202/C6203
S352-MCS-BGA080	GLZ 532-pin BGA	GLZ (S-PBGA-N532)	Gold Technologies Inc.	TMS320C64x
S288-R-BGA100- 1662	GTS 288–pin BGA	GTS (S-PBGA-N288)	Gold Technologies Inc.	TMS320C6410/C6413

Table 1. TMS320C6000 Compatible Sockets

5 Conclusion

Debugging a sophisticated system can be a difficult task, but can be simplified considerably by taking several initial steps during the design of the board. Use test points and logic analyzer headers to view external signals. Use JTAG emulation and boundary scan to view internal signals.

Simplify the debug task by breaking up complicated portions of a system into simple blocks and allowing individual areas to be tested in isolation from the remainder of the system. Provide a manual system reset to allow the board to return to a known state at any time. Use switches and sockets to allow operation in simple modes as well as upgrades from preliminary to prototype silicon as it becomes available. Designing a board with debug in mind can greatly reduce risk and speed up the time to market.

6 References

1. TMS320C6000 Peripherals Reference Guide (SPRU190).

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Mailing Address:

Texas Instruments

Post Office Box 655303 Dallas, Texas 75265

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