

66AK2Ex KeyStone™ Multicore DSP+ARM® System-on-Chips



Overview

The 66AK2Ex platform, based on TI's industry leading KeyStone™ II architecture, combines up to four ARM® Cortex™-A15 MPCore™ processors with TI's TMS320C66x high-performance fixed- and floating-point DSP. The 66AK2Ex platform provides up to 5.6 GHz of ARM and 1.4 GHz of DSP processing coupled with security and packet processing and Ethernet switching, all at lower power than multichip solutions making it optimal for embedded systems. For applications like industrial imaging, industrial control, industrial routing and switching, enterprise gateway, avionics and defense, and general-purpose embedded controllers, the 66AK2Ex platform combines ARM's best-in-class single-thread performance for control processing with the compute performance of the C66x DSP. Using TI's heterogeneous programming runtime software and tools, customers can easily develop differentiated products with 66AK2Ex SoCs.

Power and Performance

The combined floating-point processing power of the ARM Cortex-A15 processor and C66x DSP core is more than 67 GFLOPS of double-precision performance and more than 198 GFLOPS of single-precision performance. Combining the real-time performance of the C66x DSP with ARM Cortex-A15 general-purpose embedded processors yields new opportunities for bringing powerful analytics to emerging applications. These SoCs deliver new levels of power savings, achieving as low as 6 Watts on the 66AK2E02 SoC.

Fast and Wide Packet Interfaces

Processing performance alone doesn't differentiate infrastructure from consumer applications. High-performance networking

Key Features

Key features of 66AK2Ex devices include:

CorePac Processors

- Up to four Cortex-A15 processors, 19600 Dhrystone MIPS
- One C66x DSP core, 44.8 GMACS / 22.4 GFLOPS

Network AccelerationPac

- Packet coprocessor (IPv4/IPv6) for Layer 2–4
- Security coprocessor IPSec/SRTP
- Five-port 1Gb Ethernet switch
- Three-port 10Gb Ethernet switch

Memory

- Cache-coherent Multicore Shared Memory Controller (MSMC)
- 4MB Level 2 RAM/cache for ARM cluster with ECC and cache coherency
- 512KB Level 2 RAM/cache for DSP core with ECC

- 2MB shared memory with ECC and cache coherency
- One DDR3/3L 1600 interface with ECC

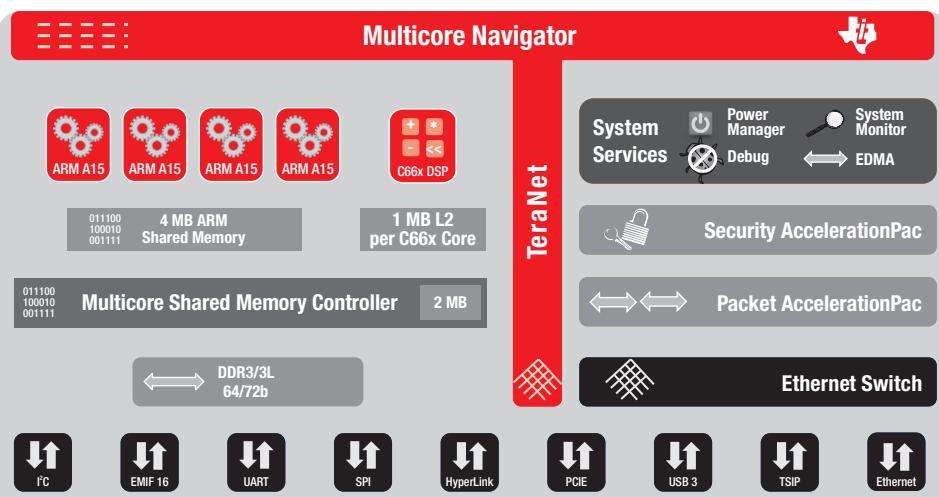
KeyStone II Architecture

- Multicore Navigator – brings single-core programming simplicity to multicore SoCs
- 8,000 atomic hardware queues
- TeraNet – on-chip interconnect providing more than two terabits per second throughput
- Low power – 6–9 Watts at 55°C case temperature, 8.5 Watts typical for 66AK2E05 SoC

High-Speed I/O

- PCI Express Gen2—up to 20 Gbps
- USB 3.0
- 1Gb Ethernet/10Gb Ethernet
- HyperLink – up to 50 Gbaud for chip-to-chip interconnect

For more technical detail see the [data sheet](#).



▲ TI's KeyStone 66AK2E05 SoC

interfaces are critical to deliver data to processors fast enough. The on-chip addition of a five-port 1Gb Ethernet switch, three-port 10Gb Ethernet switch, packet coprocessor and security coprocessor provides carrier-grade Ethernet throughput without the increase in ARM or DSP processor loading that normally comes from layer 2–4 processing, encryption and decryption. Other high-performance SERDES interfaces like PCIe deliver data to processors at infrastructure speeds, enabling the 66AK2Ex platform to handle tremendous data throughput.

TeraNet is a multilevel interconnection of high-speed non-blocking channels that delivers over two terabits per second of concurrent throughput – enabling full multicore entitlement where every processing element can operate near full capacity all of the time.

HyperLink uses a low overhead protocol that extends the TeraNet off-chip to other KeyStone SoCs and third-party devices making them appear as one larger device while simplifying software development, reducing latency and improving system performance.

High-Speed Memory for Demanding Applications

Infrastructure applications demand non-blocking, high-performance memory with error

correction. For KeyStone II, TI upgraded the multicore shared memory controller (MSMC) so that memories can operate at the speed of the processor cores, which reduces latency and contention while providing high-bandwidth interconnections between processor cores and shared internal and external memory. The 72-bit DDR3/3L controller runs at 1600 MT/s with optional error correction (ECC) support and hardware-based cache coherency, enabling more than 12.8-Gbps data transfers between external and internal memory.

Tools and Software to Reduce Development Time

Texas Instruments' development tools and runtime software support make migration and development for heterogeneous platforms simpler than ever.

The Multicore Software Development Kit (MCSDK) provides support for mainline Linux™ and TI's SYS/BIOS™ operating system for ARM and C66x DSP cores. Evaluation modules (EVMs) are available with the MCSDK and preloaded example projects. TI also provides optimized single and multicore DSP libraries for FFT, image and video analytics, matrix math and other commonly used algorithms. Third-party commercial RTOSes will also be available for 66AK2Ex processors.

TI was the first to support OpenMP® for multicore DSPs and will continue to advance OpenMP support for KeyStone II platforms. TI's OpenMP software uses a packet-based network-on-chip interconnect called Multicore Navigator to get the best multicore performance. The combination of OpenMP and Multicore Navigator frees developers from complex queue management and allows developers to use industry-standard APIs for programming TI's devices. Support for OpenCL™ is coming soon.

Code Composer Studio™ Integrated Development Environment (IDE) provides a development environment that reduces porting time and can be used as a plug-in to the open-source Eclipse IDE. TI also plans to support open source development and profiling tools for KeyStone II-based SoCs.

For more information about the 66AK2Ex platform and TI's portfolio of KeyStone multicore devices please visit www.ti.com/multicore.

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