TI-RSLK

Texas Instruments Robotics System Learning Kit





Module 11

Introduction: Liquid Crystal Display



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Educational Objectives:

REVIEW Software/hardware synchronization with busy-wait UNDERSTAND synchronous serial communication DEVELOP a set of display output functions LEARN how to display characters on an LCD screen DESIGN, BUILD & TEST A SYSTEM

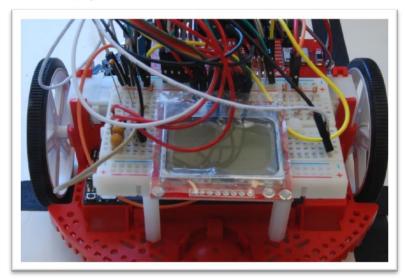
Interface an LCD to the microcontroller

Prerequisites (Modules 1, 4, and 6)

- Running code on the LaunchPad using CCS (Module 1)
- Basic C programming (Module 4)
- GPIO (Module 6)

Recommended reading materials for students:

- Volume 1 Sections 4.5, 7.6, 7.7, 8.3, and 8.4
 Embedded Systems: Introduction to the MSP432 Microcontroller ISBN: 978-1512185676, Jonathan Valvano, copyright (c) 2017
- Volume 2 Sections 1.5, 3.4, and 7.5
 Embedded Systems: Real-Time Interfacing to the MSP432
 Microcontroller, ISBN: 978-1514676585, Jonathan Valvano, copyright (c) 2017



Microcontrollers employ multiple approaches to communicate synchronously with peripheral devices and other microcontrollers. The synchronous peripheral interface (SPI) system can operate as a master or as a slave. The channel can have one master and one slave, or it can have one master and multiple slaves. In this module, the MSP432 will be the master and the LCD will be the slave. The master initiates all data communication.

A universal asynchronous receiver transmitter (UART, see Module 18) implements an asynchronous protocol, meaning the data are transmitted without timing information and the receiver derives time from the data. SPI implements a synchronous protocol, meaning transmitter and receiver operate off the same clock. Two devices communicating with asynchronous serial interfaces operate at the same frequency (baud rate) but have two separate clocks. With a UART protocol, the clock signal is not included in the interface cable between devices. Two devices communicating with SPI operate from the same clock (synchronized). With an SPI protocol, the clock signal is included in the interface cable between devices. Typically, the master device creates the clock, and the slave device(s) uses the clock to latch the data (in or out.)

The SPI protocol includes four I/O lines. The slave select STE is an optional negative logic control signal from master to slave signal signifying that the channel is active. The second line, CLK, is a 50% duty cycle clock generated by the master. The slave in master out (SIMO) is a data line driven by the master and received by the slave. The slave out master in (SOMI) is a data line driven by the slave and received by the master. In order to work properly, the transmitting device uses one edge of the clock to change its output, and the receiving device uses the other edge to accept the data.

In the lab associated with this module, we will interface a Nokia 5110 LCD using busy-wait synchronization. Before we output data or commands to the display, we will check a status flag and wait for the previous operation to complete. Busy-wait synchronization is very simple and is appropriate for I/O devices that are fast and predicable. Debugging is a critical task when developing complex systems. The motivation for this lab is to provide a real-time monitoring, so you can visualize debugging parameters as the robot is exploring its world.

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