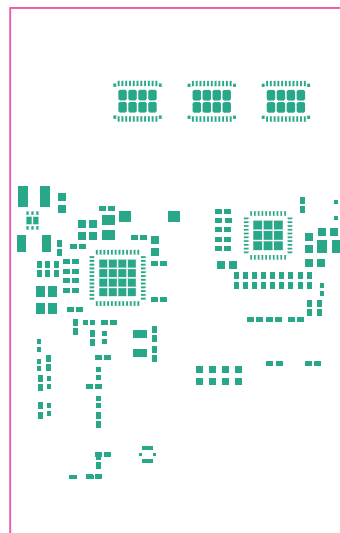
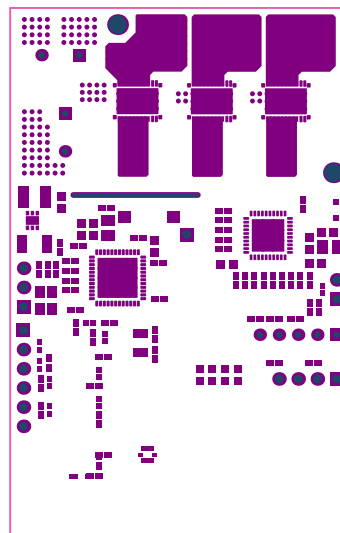


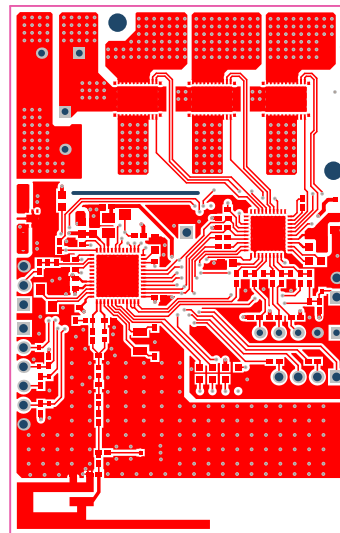
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-01516	REV: E2	SUN REV: Not In VersionControl
LAYER NAME = Top Overlay	TID #: TIDA-01516		
Top Overlay	GENERATED : 2/9/2018	8:05:45 PM	TEXAS INSTRUMENTS



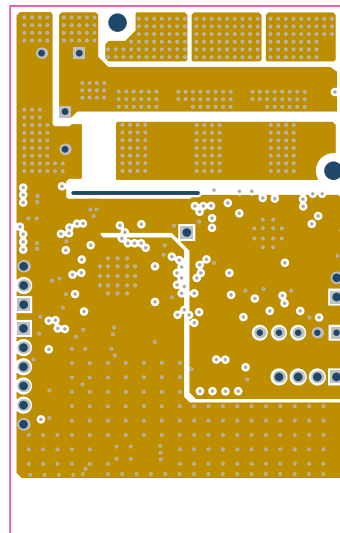
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-01516	REV: E2	SUN REV: Not In VersionControl
LAYER NAME = Top Paste	TID #: TIDA-01516		
Top Paste	GENERATED : 2/9/2018	8:05:46 PM	TEXAS INSTRUMENTS



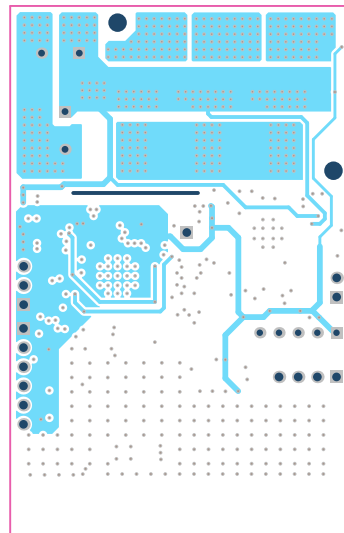
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-01516	REV: E2	SUN REV: Not In VersionControl
LAYER NAME = Top Solder	TID #: TIDA-01516		
Top Solder Mask	GENERATED : 2/9/2018 8:05:47 PM	TEXAS INSTRUMENTS	



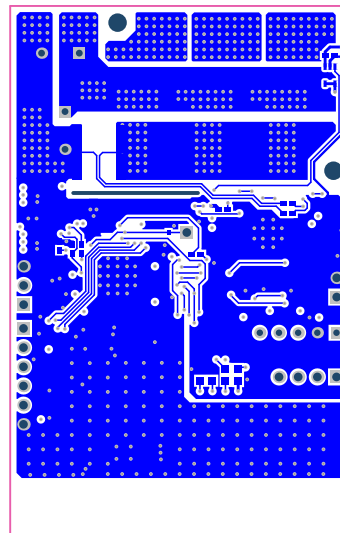
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-01516	REV: E2	SUN REV: Not In VersionControl
LAYER NAME = Top Layer	TID #: TIDA-01516		
Top Layer	GENERATED : 2/9/2018	8:05:48 PM	TEXAS INSTRUMENTS



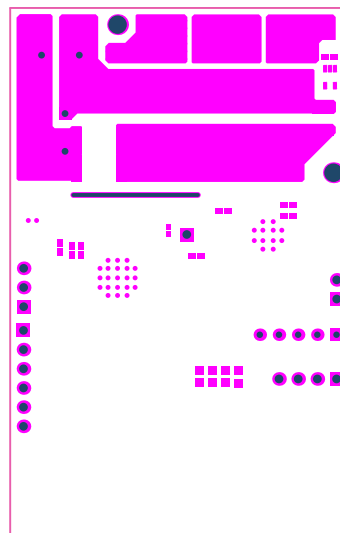
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-01516	REV: E2	SUN REV: Not In VersionControl
LAYER NAME = GND Layer	TID #: TIDA-01516		
GND	GENERATED : 2/9/2018 8:05:49 PM	TEXAS INSTRUMENTS	



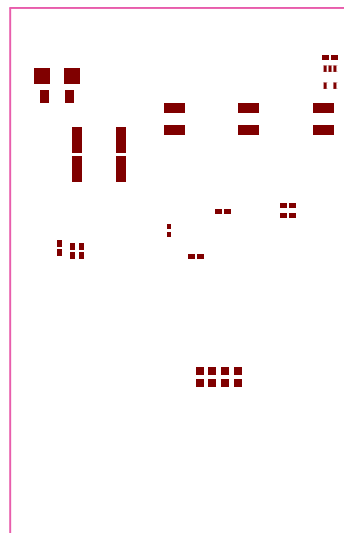
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-01516	REV: E2	SUN REV: Not In VersionControl
LAYER NAME = PWR Layer	TID #: TIDA-01516		
PWR	GENERATED : 2/9/2018 8:05:50 PM	TEXAS INSTRUMENTS	



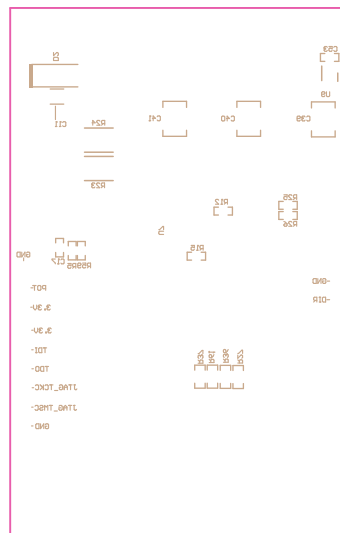
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-01516	REV: E2	SUN REV: Not In VersionControl
LAYER NAME = Bottom Layer	TID #: TIDA-01516		
Bottom Layer	GENERATED : 2/9/2018 8:05:51 PM	TEXAS INSTRUMENTS	



ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-01516	REV: E2	SUN REV: Not In VersionControl
LAYER NAME = Bottom Solder	TID #: TIDA-01516		
Bottom Solder Mask	GENERATED : 2/9/2018 8:05:51 PM	TEXAS INSTRUMENTS	



ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-01516	REV: E2	SUN REV: Not In VersionControl
LAYER NAME = Bottom Paste	TID #: TIDA-01516		
Bottom Paste	GENERATED : 2/9/2018 8:05:52 PM	TEXAS INSTRUMENTS	



ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-01516	REV: E2	SUN REV: Not In VersionControl
LAYER NAME = Bottom Overlay	TID #: TIDA-01516		
Bottom Overlay	GENERATED : 2/9/2018	8:05:53 PM	TEXAS INSTRUMENTS

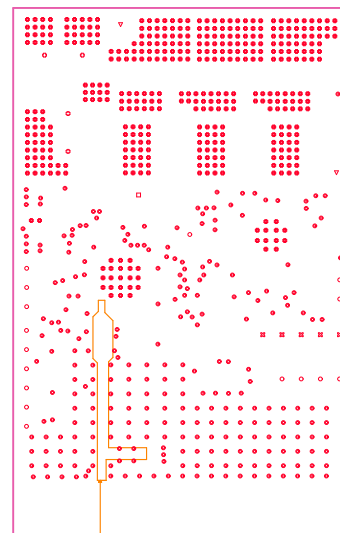
IMPEDANCE TABLE:-

Layer	SE IMP (OHM) +/-10%	SE TRACE WIDTH IN MILS	REFERENCE Layer
Top Layer	50	7.874mil	GND Layer
GND Layer	-	-	-
PWR Layer	-	-	-
BOTTOM Layer	-	-	-

STACKUP_TABLE:-

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top Layer	Copper	1.38mil		
4	Dielectric1	FR-4 High Tg	6.88mil	4.8	
5	GND Layer	Copper	1.38mil		
6	Dielectric 2	FR-4 High Tg	43.70mil	4.2	
7	PWR Layer	Copper	1.38mil		
8	Dielectric 3	FR-4 High Tg	6.88mil	4.2	
9	Bottom Layer	Copper	1.38mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				

DESIGN INFORMATION	
BOARD SIZE (REFER ALSO ARRAY/PANEL PROFILING INFORMATION) 45mm X 70mm	
Number of Layers : 4	
MIN. TRACK WIDTH: 7.874MIL	
MIN. CLEARANCE: 7 MIL	
MIN. VIA DRILL SIZE: 7.87 MIL	
MINIMUM ANNULAR RING 5 MIL EXTERNAL	
PER IPC-D-275 CLASS 2 LEVEL C	
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL	
MATERIAL:	
<input type="checkbox"/> FR-408 <input checked="" type="checkbox"/> FR-4 High Tg <input type="checkbox"/> OTHER	
THICKNESS: <input checked="" type="checkbox"/> 63 MIL (1.6mm) +/-10% <input type="checkbox"/> OTHER	
TOLERANCE: <input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2	
<input type="checkbox"/> OTHER +/-	
BOW & TWIST: <input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2	
<input type="checkbox"/> OTHER +/-	
COPPER THICKNESS (FINISHED):	
OUTER: <input checked="" type="checkbox"/> 1.4MIL (1oz) <input type="checkbox"/> 2MIL (1.4oz) <input type="checkbox"/> 2.8MIL (2oz)	
INNER SIGNAL: <input checked="" type="checkbox"/> 1.4MIL (1oz) <input type="checkbox"/> 2.8MIL (2oz) <input type="checkbox"/> N/A	
DRILLING:	
REFERENCE: <input checked="" type="checkbox"/> AS SHOWN <input checked="" type="checkbox"/> NC_DRILL FILES	
PTH MIN COPPER THICKNESS: <input checked="" type="checkbox"/> 1MIL <input type="checkbox"/> OTHER	
BOARD FINISH:	
SILKSCREEN: <input checked="" type="checkbox"/> TOP <input checked="" type="checkbox"/> BOTTOM	
SILKSCREEN COLOR: <input checked="" type="checkbox"/> WHITE <input type="checkbox"/> OTHER	
SOLDER RESIST COLOR:	
<input checked="" type="checkbox"/> GREEN <input type="checkbox"/> BLUE <input type="checkbox"/> OTHER	
SURFACE FINISH: <input checked="" type="checkbox"/> IMMERSION GOLD (ENIG) <input type="checkbox"/> ENEPIG	
IMM. TIN/SILVER OR EQUIV <input type="checkbox"/> OTHER	
ARRAY/PANEL: <input type="checkbox"/> CUT AND TRIM PER MECH LAYER 1	
<input type="checkbox"/> N.C. ROUTE <input checked="" type="checkbox"/> V. SCORE	
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:	
<input checked="" type="checkbox"/> ANSI IPC-A-600F CLASS -> <input type="checkbox"/> 1 <input checked="" type="checkbox"/> 2 <input type="checkbox"/> 3	
<input checked="" type="checkbox"/> UL 94V-0 <input checked="" type="checkbox"/> RoHS <input type="checkbox"/> OTHER PER ORDER	
ADDITIONAL REQUIREMENTS: VIA TENTING: YES <input checked="" type="checkbox"/> NO <input type="checkbox"/>	
MICROSECTION: <input type="checkbox"/> YES IMPEDANCE CONTROL: YES <input checked="" type="checkbox"/> NO <input type="checkbox"/>	
BARE BOARD ELEC. TEST: <input type="checkbox"/> NONE <input checked="" type="checkbox"/> REQUIRED <input type="checkbox"/> PER ORDER	
MANUFACTURER'S UL: <input type="checkbox"/> RAIL <input type="checkbox"/> METAL <input checked="" type="checkbox"/> SILK	

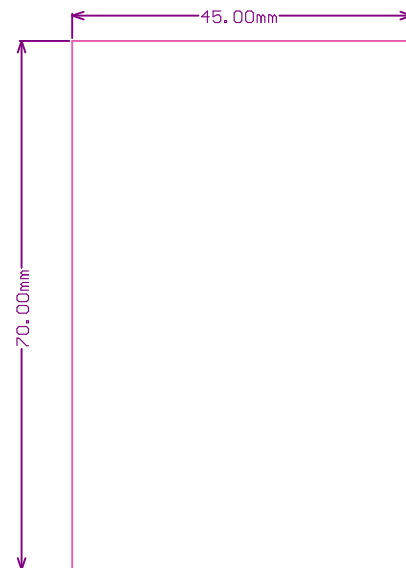


NOTE:
1. Only 10 mil vias are tented, others are not tented.
2. Only the trace inside highlighted location is impedance controlled (50 OHM)

Symbol	Count	Hole Size	Hole Length	Routed Path Length	Plated	Hole Type
□	1	20.00mil (0.508mm)	670.00mil (17.018mm)	650.00mil (16.510mm)	NPTH	Slot
□	1	19.6146mil (2.450mm)	-	-	NPTH	Round
□	4	35.43mil (0.900mm)	-	-	PTH	Round
⊗	5	33.47mil (0.850mm)	-	-	PTH	Round
○	16	45.28mil (1.150mm)	-	-	PTH	Round
○	270	10.00mil (0.254mm)	-	-	PTH	Round
○	426	7.87mil (0.200mm)	-	-	PTH	Round
718 Total						

Slot definitions : Routed Path Length = Calculated from tool start centre position to tool end centre position.
Hole Length = Routed Path Length + Tool Size = Slot length as defined in the PCB layout

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-01516	REV: E2	SUN REV: Not In VersionControl	Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.	ENGINEER: Manu Balakrishnan	LAYOUT BY: Avinash N
LAYER NAME = Drill Drawing	TID #: TIDA-01516	GENERATED : 2/9/2018 8:05:55 PM			SCALE: 1.00	ALTIM DESIGNER VERSION: 17.1.5.472
Drill Drawing	TEXAS INSTRUMENTS					



ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-01516	REV: E2	SUN REV: Not In VersionControl
LAYER NAME =	TID #: TIDA-01516		
Board Dimensions	GENERATED : 2/9/2018 8:05:59 PM	TEXAS INSTRUMENTS	

IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Texas Instruments Incorporated ("TI") technical, application or other design advice, services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using any particular TI Resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications (and of all TI products used in or for your applications) with all applicable regulations, laws and other applicable requirements. You represent that, with respect to your applications, you have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. You agree that prior to using or distributing any applications that include TI products, you will thoroughly test such applications and the functionality of such TI products as used in such applications. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

You are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING TI RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY YOU AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

You agree to fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of your non-compliance with the terms and provisions of this Notice.

This Notice applies to TI Resources. Additional terms apply to the use and purchase of certain types of materials, TI products and services. These include; without limitation, TI's standard terms for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>), [evaluation modules](#), and [samples](http://www.ti.com/sc/docs/sampterm.htm) (<http://www.ti.com/sc/docs/sampterm.htm>).

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2018, Texas Instruments Incorporated