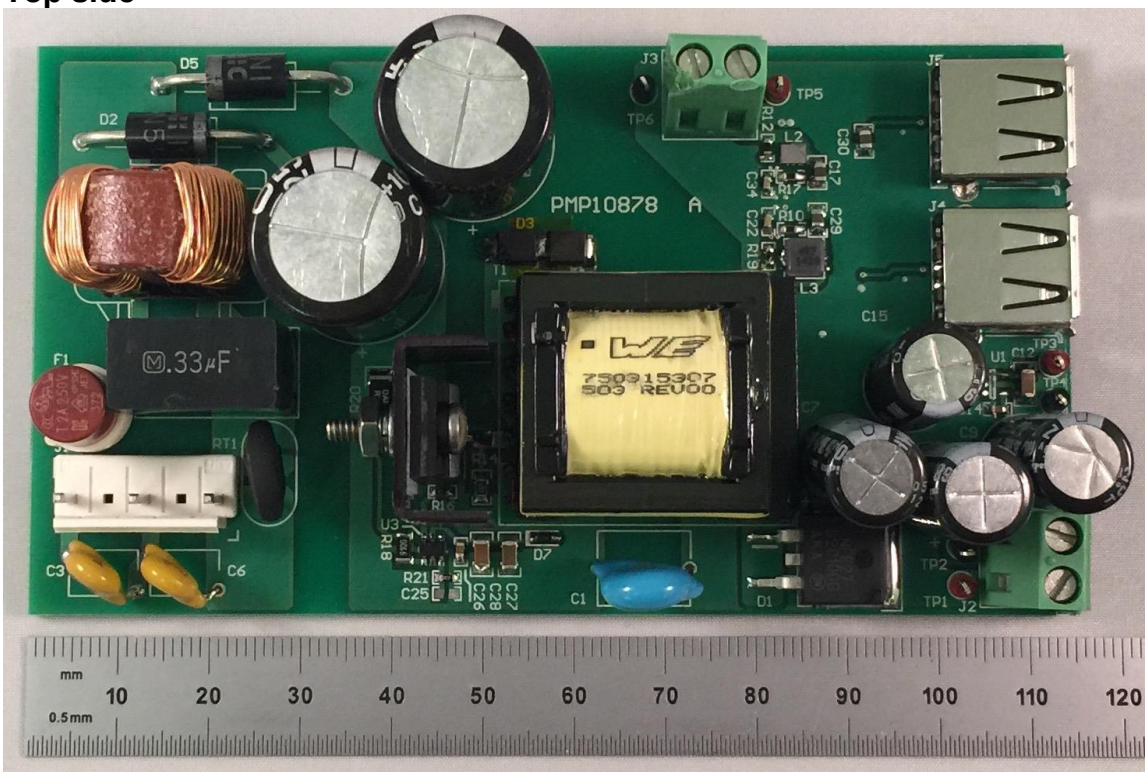
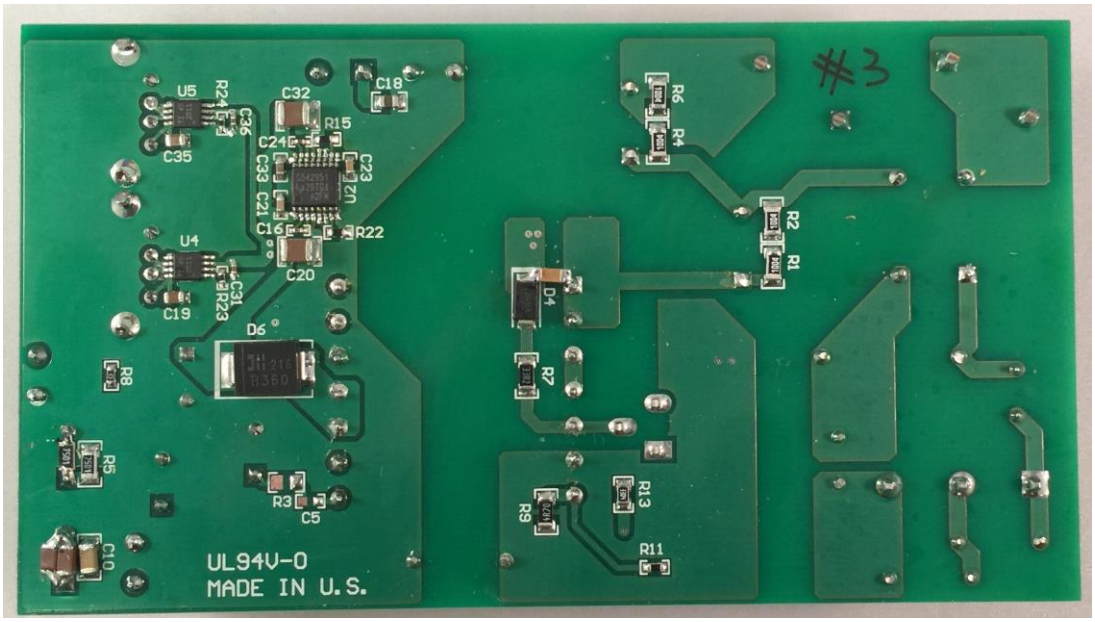
1 Photo

The photographs below show the PMP10878 Rev A assembly. This circuit was built on a PMP10878 Rev A PCB.

Top side



Bottom side

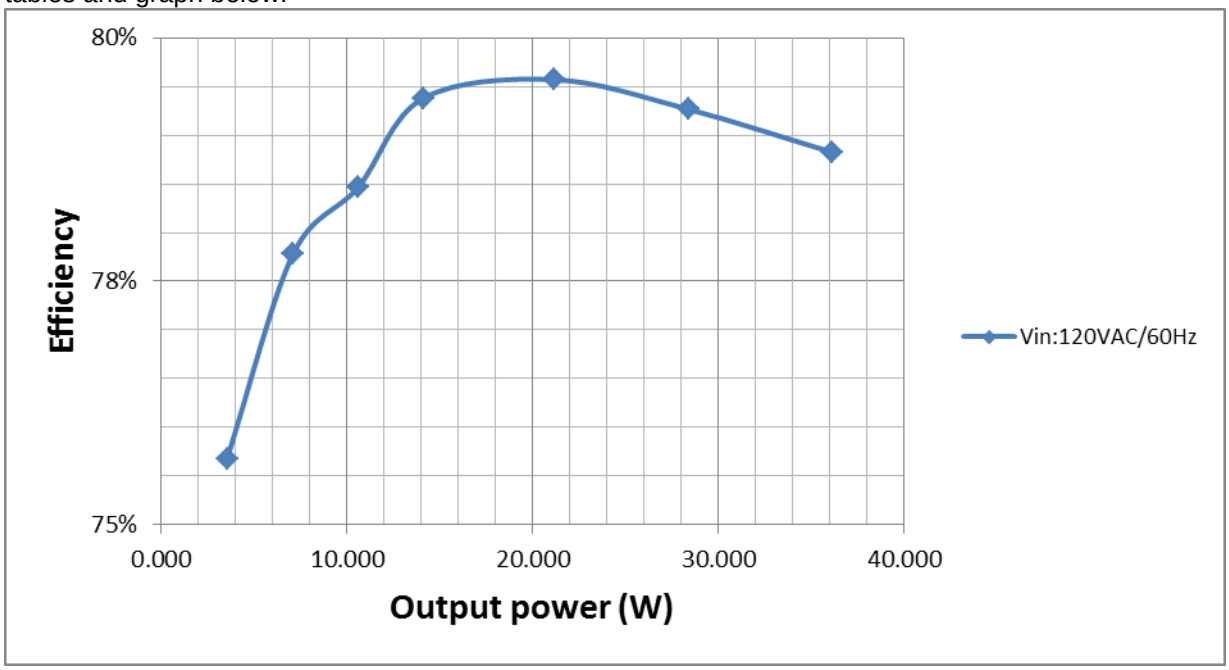


2 Converter Efficiency

The efficiency data of PMP10878Rev A was tested stage by stage.

2.1 Total efficiency:

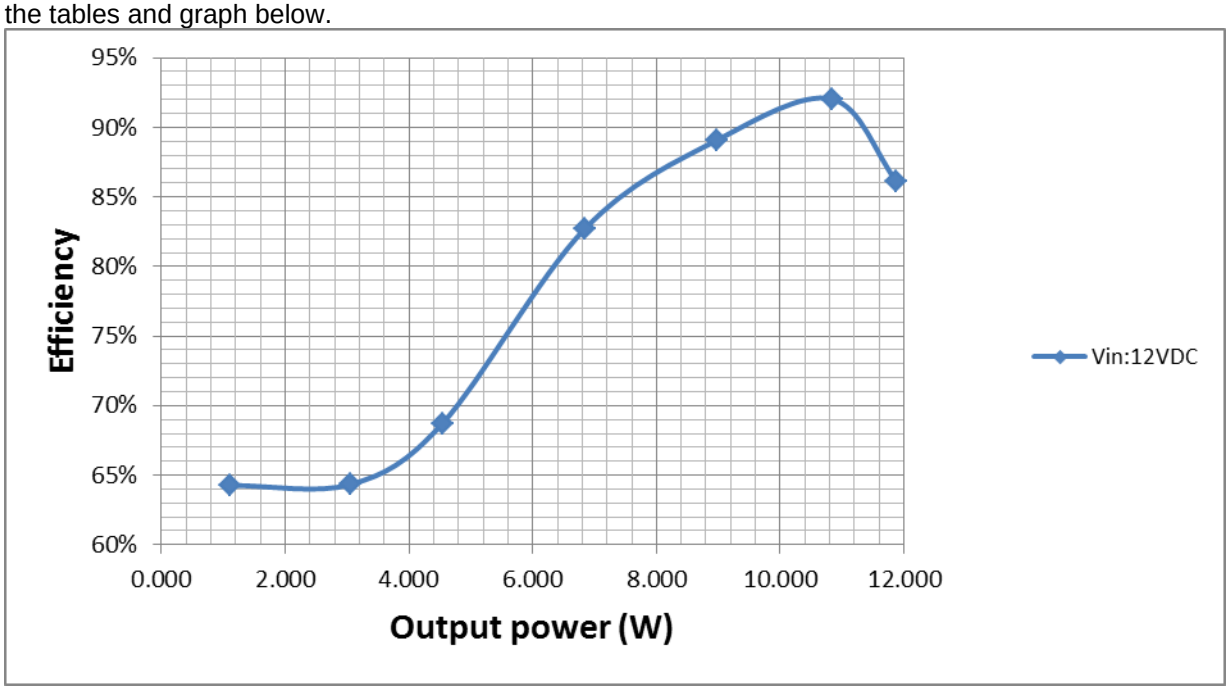
During this test, AC source is applied to connector J1 with U1 shorted. The efficiency data is shown in the tables and graph below.



Vin(AC)	Iin(A)	Pin(W)	24V(V)	24V(A)	Vo1(V)	Io1(A)	Vo2(V)	Io2(A)	Vo3(V)	Io3(A)	Pout(W)	Eff. (%)
120.03	0.64	45.87	24.32	1.04	5.09	0.99	5.13	0.49	3.29	1.01	36.16	78.82%
119.97	0.51	35.84	24.26	0.80	5.10	0.83	5.13	0.41	3.30	0.81	28.41	79.27%
120.10	0.38	26.57	24.18	0.59	5.12	0.63	5.15	0.30	3.31	0.61	21.14	79.57%
120.14	0.26	17.75	24.09	0.40	5.14	0.42	5.15	0.21	3.31	0.42	14.09	79.38%
120.23	0.21	13.48	24.24	0.30	5.15	0.30	5.16	0.15	3.31	0.30	10.58	78.46%
120.07	0.14	9.12	24.24	0.20	5.20	0.20	5.20	0.10	3.31	0.20	7.09	77.78%
120.20	0.08	4.66	24.16	0.10	5.18	0.10	5.18	0.05	3.31	0.10	3.53	75.68%
120.33	0.02	0.28	24.55	0.00	5.22	0.00	5.22	0.00	3.33	0.00	0.00	0.00%

2.2 5V & 3.3V converter efficiency with $12V_{DC}$ input:

During this test, $12V_{DC}$ source is applied to connector TP3 with U1 shorted. The efficiency data is shown in the tables and graph below.

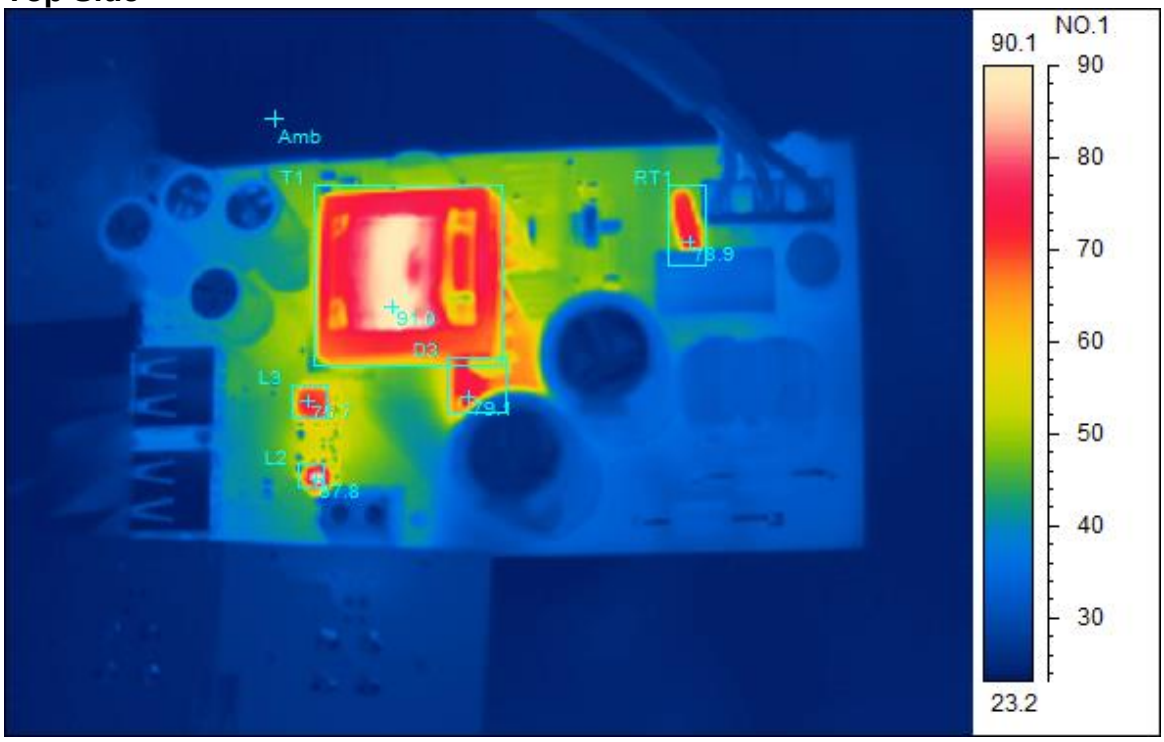


Vin(V)	Iin(A)	Pin(W)	Vo1(V)	Io1(A)	Vo2(V)	Io2(A)	Vo3(V)	Io3(A)	Pout(W)	Eff. (%)
12.00	1.150	13.800	5.070	1.20	5.130	0.49	3.295	1.00	11.881	86.09%
12.01	1.039	11.768	5.090	0.99	5.130	0.49	3.295	1.00	10.831	92.04%
12.04	0.845	10.069	5.100	0.82	5.130	0.41	3.296	0.81	8.967	89.06%
12.07	0.635	8.272	5.120	0.63	5.140	0.32	3.312	0.60	6.842	82.71%
12.10	0.418	6.604	5.140	0.42	5.160	0.20	3.311	0.41	4.537	68.70%
12.12	0.282	4.764	5.150	0.30	5.160	0.10	3.309	0.30	3.065	64.35%
12.14	0.102	1.732	5.180	0.10	5.180	0.05	3.309	0.10	1.113	64.27%
12.16	0.000	0.760	5.180	0.00	5.180	0.00	3.312	0.00	0.000	0.00%

3 Thermal Images

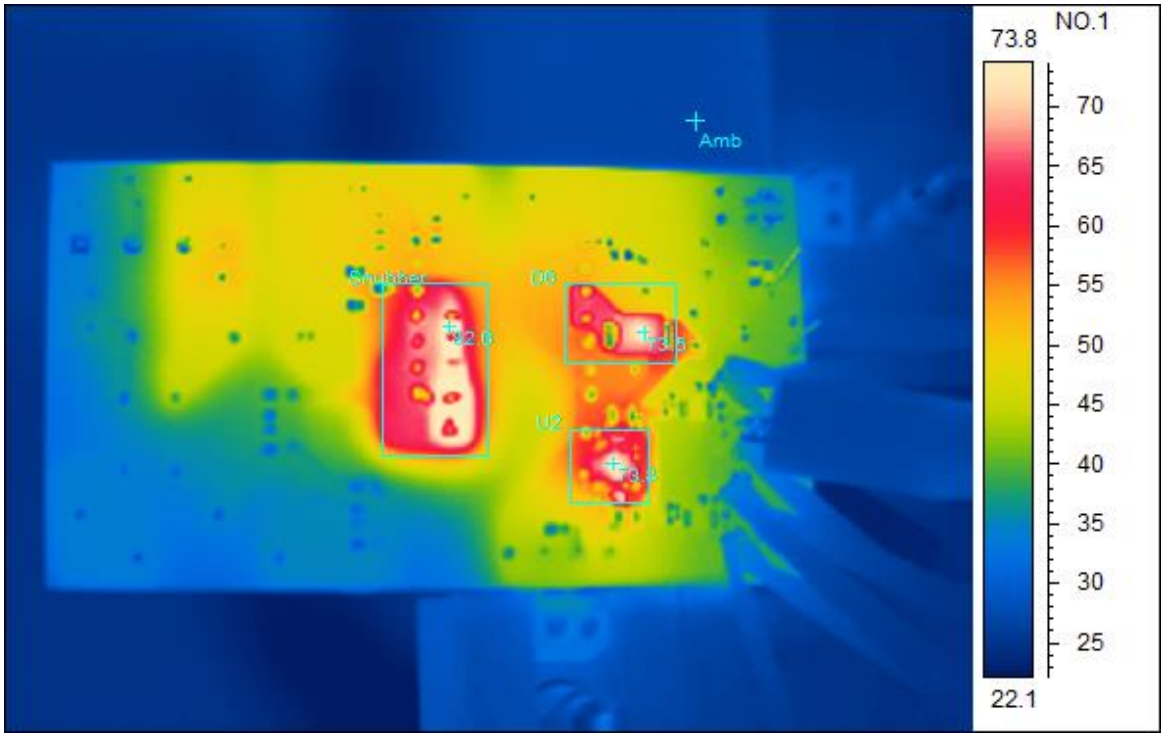
The thermal images below show a top view and bottom view of the board at 120V_{AC}/60Hz input. The ambient temperature was 20ºC with no forced air flow. The outputs were loaded with 24V/1A, 5V/1A, 5V/0.5A, 3.3V/1A.

Top Side



Spot analysis	Value
Amb Temperature	24.0°C
Area analysis	**Value**
T1Max	91.0°C
L3Max	75.7°C
L2Max	87.8°C
RT1Max	78.9°C
D3Max	79.1°C

Bottom Side



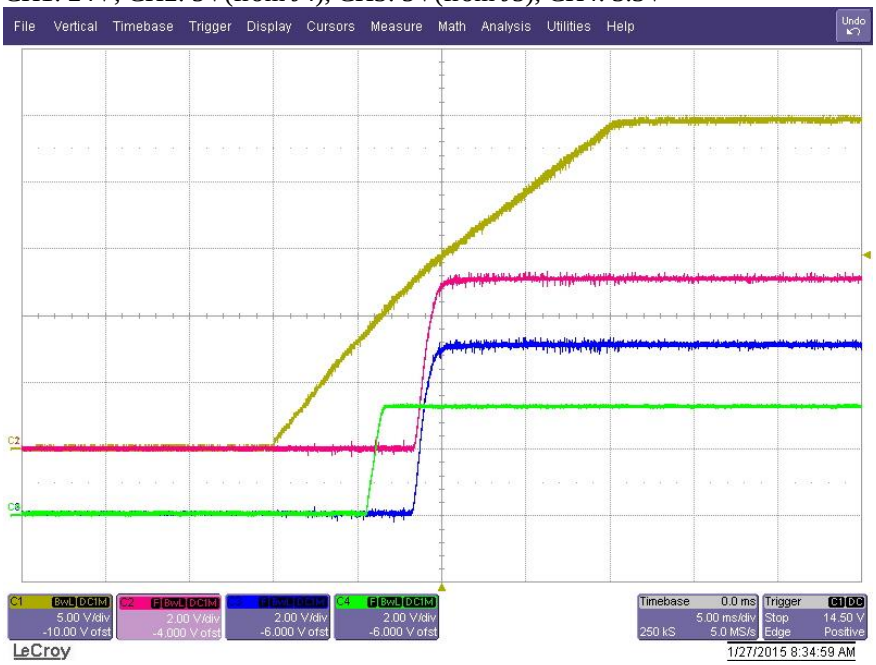
Spot analysis	Value
Amb Temperature	27.5°C
Area analysis	**Value**
SnubberMax	82.6°C
D6Max	73.5°C
U2Max	73.8°C

4 Startup

The output voltages at startup are shown in the images below.

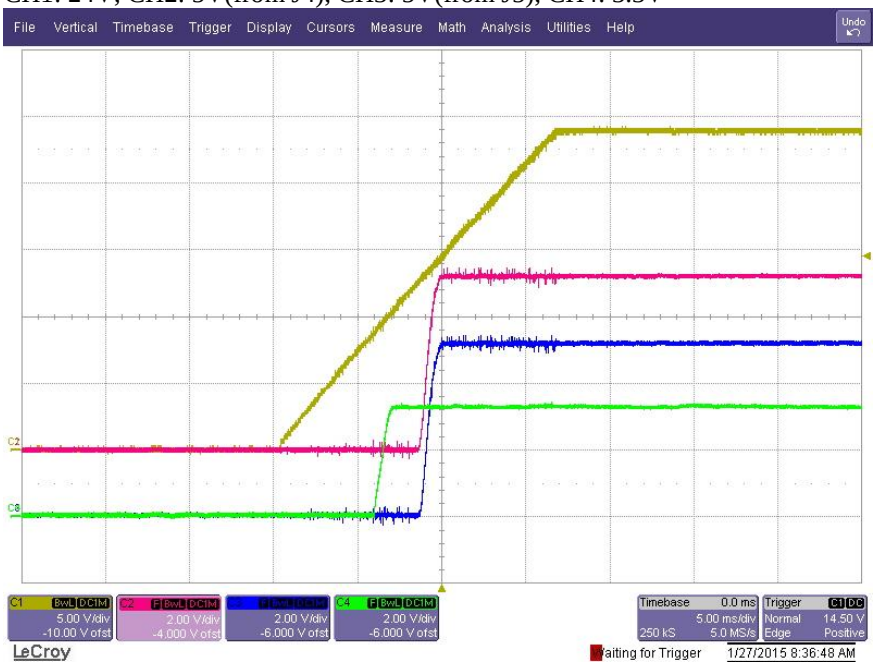
4.1 Full load startup @ 120V_{AC}/60Hz: 24V/1A, 5V/1A (from J4), 5V/0.5A (from J5), and 3.3V/1A outputs.

CH1: 24V, CH2: 5V(from J4), CH3: 5V(from J5), CH4: 3.3V



4.2 No load startup @ 120V_{AC}/60Hz.

CH1: 24V, CH2: 5V(from J4), CH3: 5V(from J5), CH4: 3.3V



5 Cross regulation

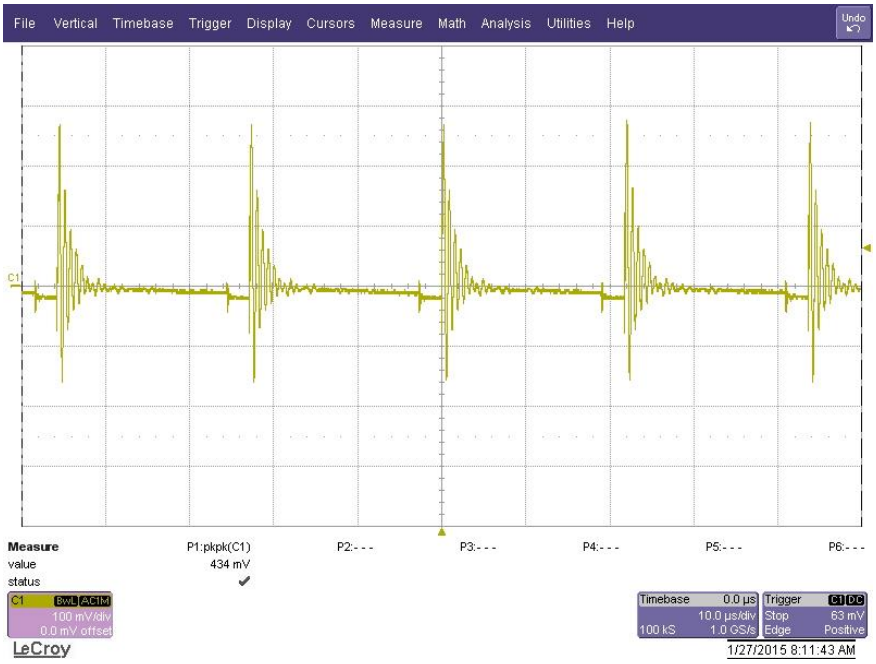
Cross regulation between 24V and the input voltage at U2 is tested at $120V_{AC}$/60Hz input with U1 shorted.

Current(A)				Voltage(V)	
24V	5V(from J4)	5V(from J5)	3.3V	24V	12V(D2D/U2 input)
1	0	0	0	23.61	13.18
0.103	0.992	0.489	0.989	**26.33**	11.67

6 Output Ripple Voltages

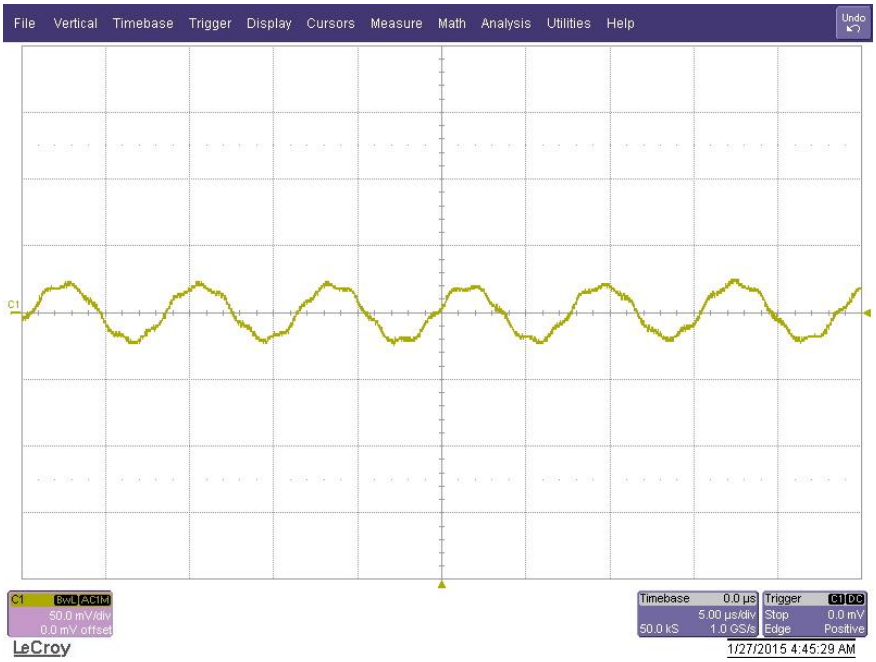
The output ripple voltages are shown in the plots below with full load and 120V_{AC}/60Hz input.

6.1 24V, and 12V (U2 input): 24V/1A, 5V/1A (from J4), 5V/0.5A (from J5), and 3.3V/1A outputs.

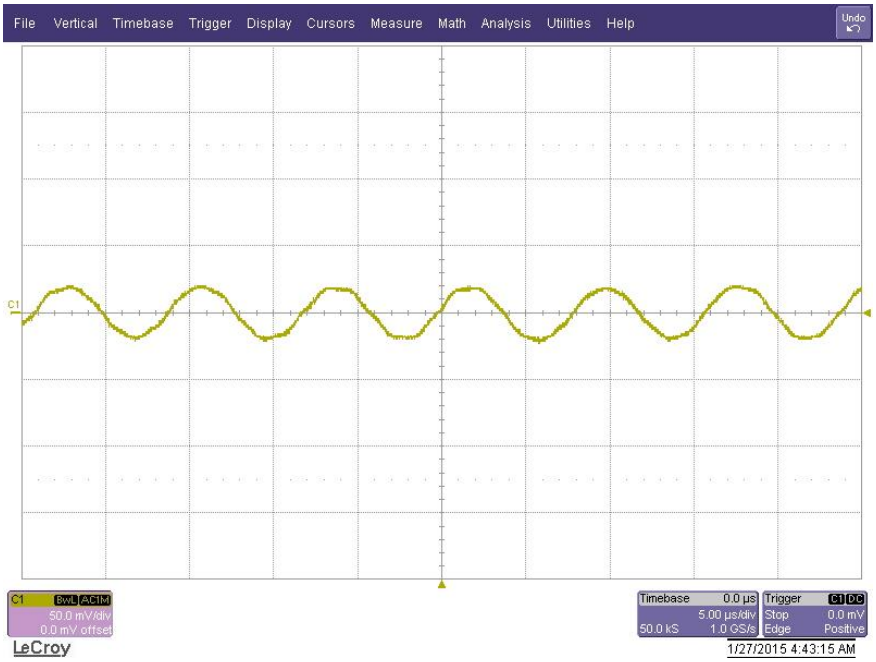


6.2 24V, and 12V (U2 input): no load.

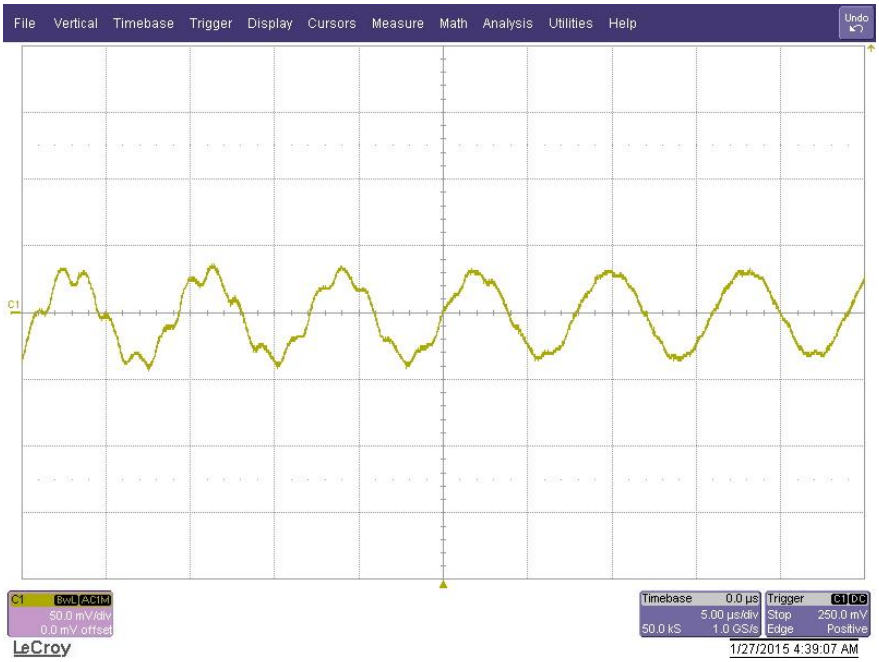
6.3 5V(from J4): 5V/1A (from J4), 5V/0.5A (from J5), and 3.3V/1A outputs.



6.4 5V(from J5): 5V/1A (from J4), 5V/0.5A (from J5), and 3.3V/1A outputs.



6.5 3.3V: 5V/1A (from J4), 5V/0.5A (from J5), and 3.3V/1A outputs.



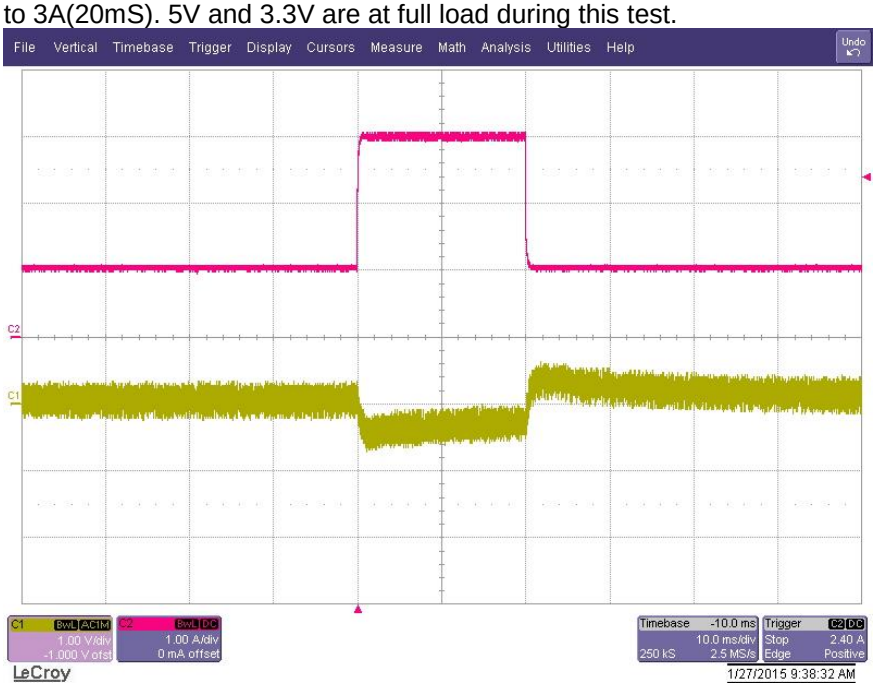
6.6 5V(from J4): no load.

6.7 5V(from J5): no load.

6.8 3.3V: no load.

7 Dynamic Load Response

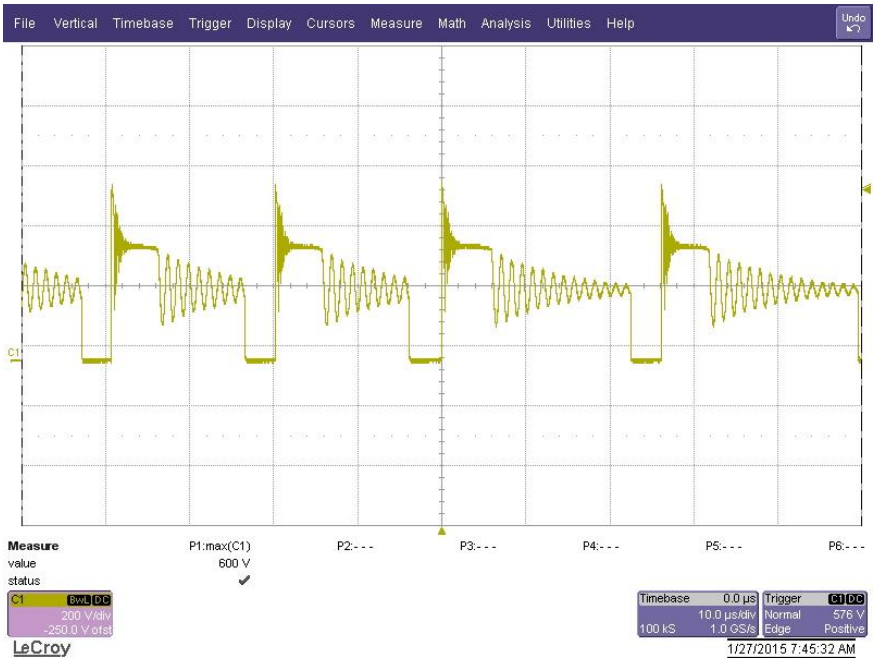
The image below shows the dynamic load response on 24V at $120V_{AC}$/60Hz. Load step is from 1A(2second) to 3A(20mS). 5V and 3.3V are at full load during this test.



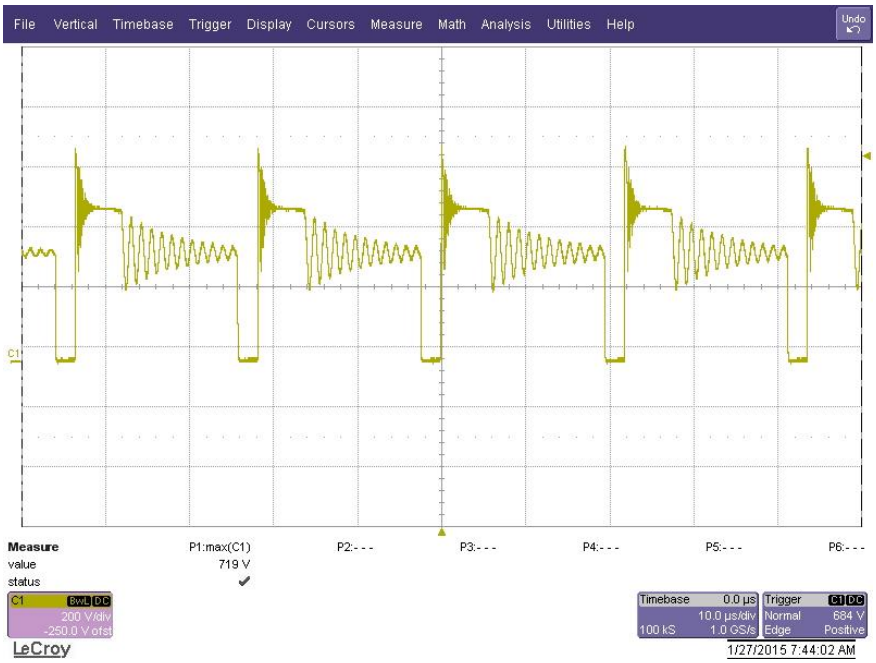
8 Switching Waveforms

The images below show key switching waveforms of PMP10878RevA. The waveforms are measured at full load.

8.1 Voltage at Q1 Drain @ 90V_{AC}/60Hz input and 24V/1A, 5V/1A (from J4), 5V/0.5A (from J5), 3.3V/1A outputs

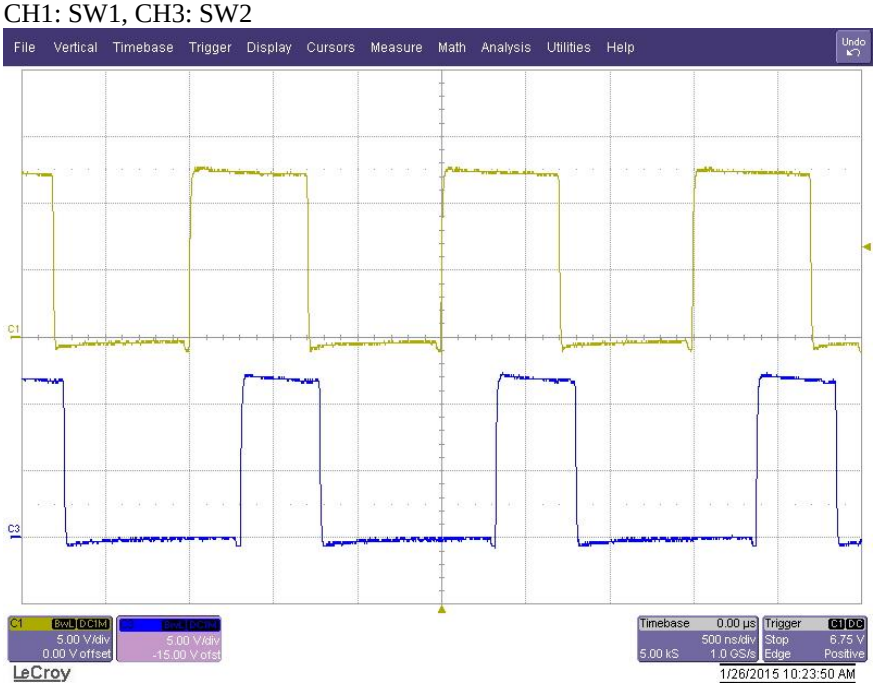


8.2 Voltage at Q1 Drain @ 132V_{AC}/60Hz and 24V/1A, 5V/1A (from J4), 5V/0.5A (from J5), 3.3V/1A outputs



8.3 Voltage at U2 SW1 and SW2 pins @ 12V_{DC} input on U2 and 5V/1A (from J4), 5V/0.5A (from J5), 3.3V/1A outputs

CH1: SW1, CH3: SW2



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