TI Designs

10-W Bias Supply for Brushless DC Applications With >75% Efficiency at Low Load Reference Design

TI Designs

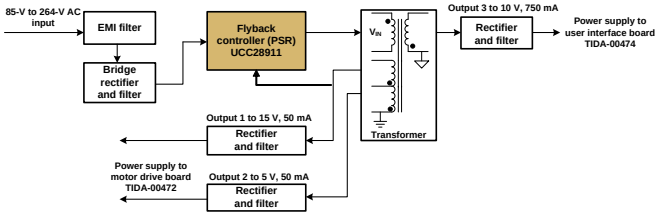
The reference design TIDA-00473 is a universal input, 10-W, high-efficiency, low-cost power supply with three isolated outputs. This is a constant-voltage (CV) and constant-current (CC) flyback converter without an optical coupler and external MOSFET. The hardware is designed and tested to pass conducted emissions, surge, and EFT testing as per the EN55014 requirements for household appliances. This can be used in applications like cooker hoods and other appliances wherever motor drive along with user interface is involved.
The key highlights of this reference design are:

- Optimized transformer design, valley switching used to reduce switching losses and enable the optimum efficiency over entire operating range
- Integrated 700-V MOSFET and primary side regulation control eliminating external FET and optical-coupler for optimal cost and reliability
- Valley switching and frequency dithering to ease EMI compliance and reduce the total cost of BOM

Design Resources

TIDA-00473	Design Folder
UCC28911	Product Folder

TI E2E™ Community — ASK Our E2E Experts



Design Features

- Universal Input Voltage Range (85-V to 270-V AC) to Address Customer Needs Across all Regions
- Up to 700-V Start-Up and Smart Power Management Enables <30-mW Standby Power
- Primary Side Regulation (PSR) Control Eliminates Optical Coupler
- Multiple Operating Modes and Valley Switching for Optimum Efficiency Over Entire Operating Range
- Valley Switching and Frequency Dithering to Ease EMI Compliance
- No Need of External Voltage Compensation Components
- Meets Requirements of Conducted Emissions Standard—EN55022 Class B
- Meets Requirements of EFT Norm IEC6000-4-4 and Surge Norm IEC61000-4-5
- Small Use PCB Form Factor (72 × 65 mm)

Featured Applications

- Bias Power for Cooker Hood
- Home Appliances
- Bias Power for Air Conditioning
- Power Tools Bias Power Supply

1 Key System Specifications

Table 1. Electrical Performance Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	NOM	MAX	UNIT
INPUT CHARACTERISTICS						
Input voltage	V_{IN}		85	115/230	270	VAC
Frequency	f_{LINE}		47	50/60	64	Hz
No load power	P_{NL}	Vin = 90 V Iout = 0 A		40		mW
Brownout voltage	V_{IN_UVLO}	IOUT = INOM		75		V
Brownout recovery voltage	V_{INOV}			85		V
Input current	I_{IN}	V_{IN} =V_{MIN} I_{OUT} = $I_{OUT(MAX)}$		0.25		A
OUTPUT CHARACTERISTICS						
Primary output voltage	V_{OUT1}	V_{IN} =V_{MIN} to V_{MAX} I_{OUT} = 0 to I_{NOM}	4.5	5	5.5	V
	V_{OUT2}		14.5	15		
Secondary output voltage	V_{OUT3}		9.5	10	10.5	
Maximum output current	$I_{OUT1(MAX)}$	V_{IN} =V_{MIN} to V_{MAX}		50		mA
	$I_{OUT2(MAX)}$			50		
	$I_{OUT3(MAX)}$			750		
Minimum output current	$I_{OUT1(MIN)}$	V_{IN} = V_{MIN} to V_{MAX}	5			mA
	$I_{OUT2(MIN)}$		0			
	$I_{OUT3(MIN)}$		10			
Line regulation				± 1		%
Load regulation				± 5		%
Output voltage ripple	ΔV_{OUT1}	V_{IN} = V_{MIN} to V_{MAX}		70		mV
	ΔV_{OUT2}	I_{OUT1}, I_{OUT2}, I_{OUT3} = 0 to I_{NOM}		80		
	ΔV_{OUT3}			150		
Total maximum output power	P_{OUT}	V_{IN} = V_{MIN} to V_{MAX}		8.5		W
Insulation class		Test from primary to secondary		Reinforced insulation		
SYSTEM CHARACTERISTICS						
Efficiency	η	V_{IN} =V_{NOM} I_{OUT} = 25%, 50%, 75%, 100% of I_{OUT}	75	80	83	%
Protection		Output overpower				
		Output overvoltage				
		Input UVLO				
		Thermal shutdown				
Operation ambient	T	Open frame	-40	25	65	°C
Conducted emissions		Test with TIDA-00472 Or test individual	As per EN55022 – class B			
EFT		Tested with TIDA-00472	As per IEC-61000-4-4			
Surge		Tested with TIDA-00472	As per IEC-61000-4-5			

Table 1. Electrical Performance Specifications (continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	NOM	MAX	UNIT
MECHANICAL						
Dimensions	W	Width		72		mm
	L	Length		65		
	H	Component height		20		

2 System Description

Home appliance equipment use different subsystems for the proper functionality, such as motor drives, lighting systems, user interfaces, and so on. Air conditioners, washing machines, refrigerator, dish washers, and kitchen hoods are examples of such home appliances. A properly rated and protected bias power supply is required for gate drivers, microcontrollers, LED lighting and interface, user interface, and so on used in these subsystems.

The TIDA-00473 reference design is primarily aiming to power kitchen hood (also called range vent hood, range hood, cooker hood, or chimney) subsystems. The cooker hood consists of a suction fan driven by a mains powered electric motor, lamps, and human interface or control options. The advanced cooker hood uses the efficient brushless DC (BLDC) motor drives. The BLDC motor drive uses gate drivers and microcontrollers, which need different regulated bias supplies such as 15 V, 3.3 V, 5 V, and so on for their functionality. LED lighting is another subsystem in kitchen hood, which needs a regulated low-voltage DC power supply with enough power rating to drive the LEDs. The user interface such as touch keys or proximity sensing also consists of microcontrollers and sensors that need a regulated low-voltage DC power supply.

The TIDA-00473 is a reference bias power supply design for kitchen hoods. However, it is applicable in any other systems where a bias power supply needs to be generated from the high voltage mains. The TIDA-00473 is designed meet the universal input voltage range of 85-V to 270-V AC. The design provides three isolated outputs: 15 V for the gate driver used in the motor drive, 5 V for the microcontroller in the motor drive, and 10 V for the LED drive and user interface. The TIDA-00473 is a CV and CC flyback converter without an optical coupler and external MOSFET.

Valley switching technique reduces switching losses, and the controller consumption is dynamically adjusted with load, which can enable the optimum efficiency over the entire operating range. The integrated 700-V MOSFET and primary side regulation control eliminates the external FET and optical coupler for optimal cost and reliability. Valley switching and frequency dithering eases EMI compliance and reduces the total cost of the BOM.

The hardware is designed and tested to pass conducted emissions, surge, and EFT testing as per the EN55014 requirements for household appliances.

3 Block Diagram

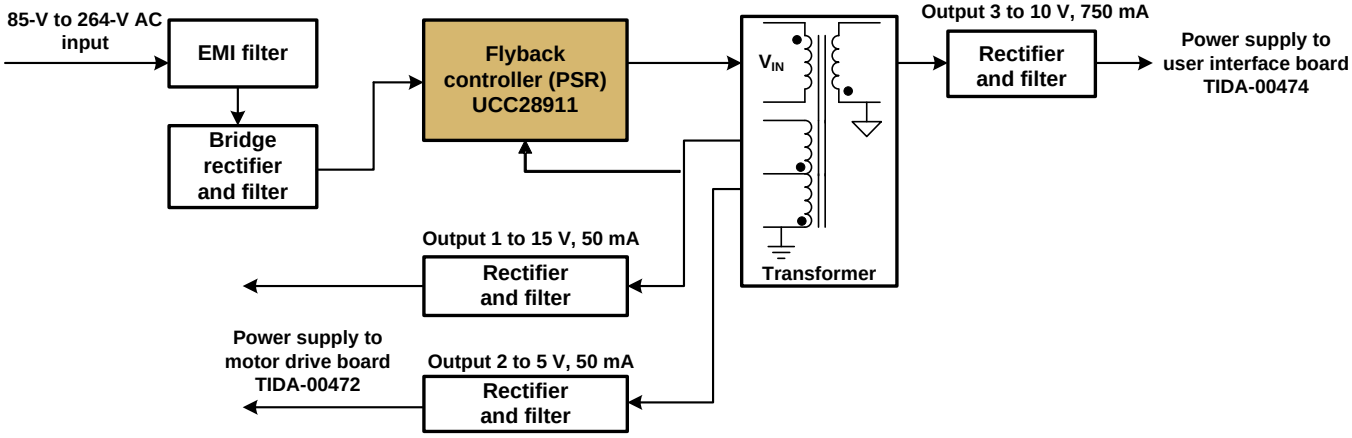


Figure 1. Block Diagram of Power Supply With Isolated Multiple Outputs

3.1 Highlighted Products and Key Advantages

The following subsections detail the highlighted products used in this reference design, including the key features for their selection. See their respective product datasheets for complete details.

3.1.1 UCC28911—Flyback Controller (Primary Side Regulation)

The UCC28911 is high-voltage flyback switcher that provides output voltage and current regulation without the use of an optical coupler. This device incorporate a 700-V power FET and a controller that process operating information from the flyback auxiliary winding and power FET to provide a precise output voltage and current control. The integrated high-voltage current source for startup is switched off during operation, and the controller current consumption is dynamically adjusted with the load. This controller can enable a very low standby power consumption.

Control algorithms in the UCC28911, combining switching frequency and peak primary current modulation, allow operating efficiencies to meet or exceed applicable standards. Discontinuous conduction mode (DCM) with valley switching reduces switching losses. Built-in protection features help to keep secondary and primary component stress levels in check across the operating range. The frequency jitter helps to reduce EMI filter cost.

Low system parts count and built-in advanced protection features result in a cost-effective solution that meets stringent world-wide energy efficiency requirements.

The UCC28911 also has a complete set of system protection features that greatly improve reliability and further simplifies the design:

- Input undervoltage lockout
- Output overvoltage protection
- Output overpower protection
- Primary overcurrent
- VDD clamp overcurrent
- Thermal shutdown

4 System Design Theory

This reference design is a universal input, 10-W power supply with three isolated outputs designed for bias power of appliances. The power supply is configured as a CV and CC flyback converter using the UCC28911 controller. The UCC28911 is a high voltage switcher that integrates a high voltage power FET and a primary-side-regulated controller, supporting magnetically-sensed output voltage regulation through the transformer bias winding. This type of sensing eliminates the need for a secondary-side reference, error amplifier, and optical isolator for output voltage regulation. The device delivers accurate output voltage under static load, load variations, and line voltage variation and provides accurate control of output current.

The magnetic sampling scheme allows operation only in DCM so the device is not allowed to turn on the power FET if it does not sense a zero crossing detector (ZCD) event. A ZCD event is when auxiliary winding voltage crosses zero from high to low after transformer demagnetization is completed. The modulator adjusts both frequency and peak current in different load regions to maximize efficiency throughout the operating range. The smart management of the control logic power consumption and the high-voltage (HV) current source, used for startup that is off during operation and have very low leakage current, allow designing converters with very low standby input power. The standby input power less than 30 mW at
90-V AC input can be easily achieved with this device.

4.1 Design Requirement

The design parameters used in this reference design is given in Table 2.

Table 2. Design Parameters

PARAMETER	SYMBOL	NOTES AND TEST CONDITIONS	MIN	NOM	MAX	UNIT
INPUT CHARACTERISTICS						
Input voltage	V_{IN}		85	115/230	270	VAC
Frequency	f_{LINE}		47	50/60	64	Hz
No load power	P_{NL}	V_{IN} = 90 V I_{OUT} = 0 A		40		mW
Brownout voltage	V_{IN_UVLO}	$I_{OUT} = I_{NOM}$		75		V
Brownout recovery voltage	V_{INOV}			85		V
Input current	I_{IN}	$V_{IN} = V_{MIN}$ $I_{OUT} = I_{OUT(MAX)}$		0.25		A
OUTPUT CHARACTERISTICS						
Primary output voltage	V_{OUT1}	$V_{IN} = V_{MIN}$ to V_{MAX} I_{OUT} = 0 to I_{NOM}	4.5	5	5.5	V
	V_{OUT2}		14.5	15		
Secondary output voltage	V_{OUT3}		9.5	10	10.5	
Maximum output current	$I_{OUT1(MAX)}$	$V_{IN} = V_{MIN}$ to V_{MAX}		50		mA
	$I_{OUT2(MAX)}$			50		
	$I_{OUT3(MAX)}$			750		
Minimum output current	$I_{OUT1(MIN)}$	$V_{IN} = V_{MIN}$ to V_{MAX}	5			mA
	$I_{OUT2(MIN)}$		0			
	$I_{OUT3(MIN)}$		10			
Output voltage ripple	ΔV_{OUT1}	$V_{IN} = V_{MIN}$ to V_{MAX} I_{OUT1}, I_{OUT2}, I_{OUT3} = 0 to I_{NOM}		70		mV
	ΔV_{OUT2}			80		
	ΔV_{OUT3}			150		
Total maximum output power	P_{OUT}	$V_{IN} = V_{MIN}$ to V_{MAX}		8.5		W
SYSTEM CHARACTERISTICS						
Efficiency	η	$V_{IN} = V_{NOM}$ I_{OUT} = 25%, 50%, 75%, 100% of I_{OUT}	75	80	83	%

4.2 Detailed Design Procedure

This procedure outlines the steps to design the CV, CC flyback converter based on the UCC28911. See Figure 2 for component names and network locations. The design procedure equations use terms that are defined in Section 4.2.1.

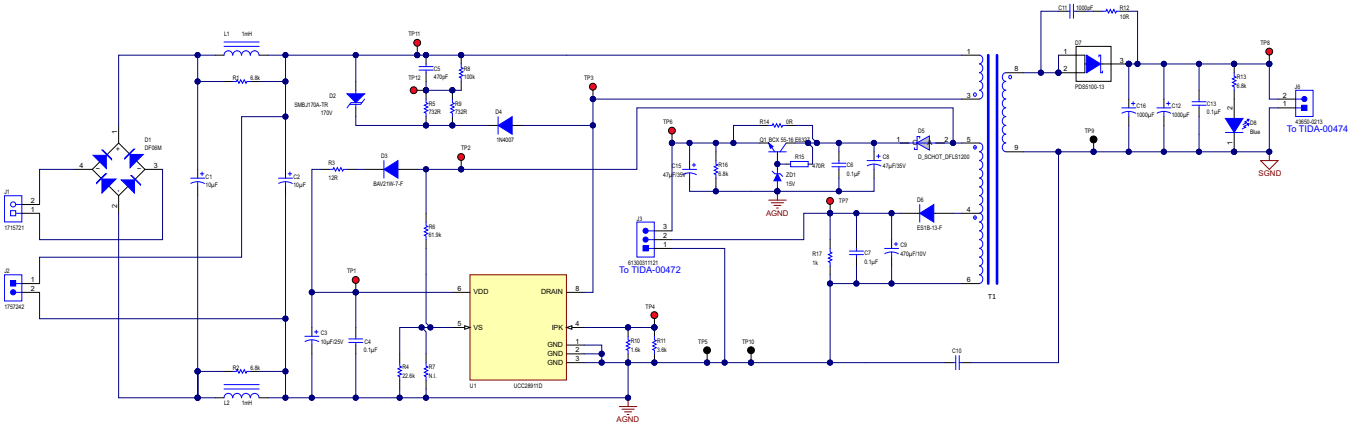


Figure 2. Multiple Output Flyback Converter Based on UCC28911

- Diode bridge D1, input capacitors C1 and C2, transformer T1, UCC28911 switcher U1, Schottky rectifiers D5, D6, and D7, and capacitors C8, C9, and C16 form the power stage of the converter. Note that the U1 is also part of the power stage since the high-voltage MOSFET is integrated in U1.
- The input EMI filter is made up of C1 and C2 and differential mode inductors L1 and L2.
- R1 and R2 serve the dual function of dampening input filter oscillations and prevent a large voltage being developed across L1 and L2 in the event of an ESD pulse.
- Resistors R5 and R9, capacitor C5, and diode D4 make up the primary side voltage clamp. The clamp prevents the drain voltage on U1 from exceeding its maximum rating. A secondary function of the clamp is to alleviate the EMI currents associated with the turn-off voltage of U1.
- Operating bias to the controller is provided by the auxiliary winding on T1, diode D3, resistor R3, and bulk capacitor C3.
- Resistor R6 programs the startup voltage threshold.
- Resistors R4 and R7 program the output voltage set point.
- Resistors R10 and R11 program the maximum output current.
- Resistors R13, R16, and R17 adjust the no load output voltage.

4.2.1 Transformer Design

Design specifications:

- Maximum input DC voltage: V_{MAX} = 380 V
- Minimum start up input DC voltage: V_{MIN} = 120 × 0.6 = 75 V (see Section 4.2.2)
- Ripple current to peak current ratio: K_{RP} = 0.4
- Output voltage 1): V_{O1} = 10 V
- Output current 1: I_{O1} = 0.75 A
- Diode voltage drop at output 1: V_{D1} = 0.6 V
- Output voltage 2: V_{O2} = 5 V
- Output current 2: I_{O2} = 0.05 A
- Diode voltage drop at output 2: V_{D2} = 0.5 V
- Output voltage 3: V_{O3} = 15 V
- Output current 3: I_{O3} = 0.05 A
- Diode voltage drop at output 3: V_{D3} = 0.4 V
- Maximum switching frequency: $f_{TARGET(MAX)}$ = 80 kHz
- Allowed AC flux density (Tesla): B_{AC} = 0.075; B_{MAX} = 0.3
- Maximum duty cycle: $D_{MAX} = 1 - 0.425 - 0.000002 \times \frac{f_{TARGET(MAX)}}{2} = 0.495$
- Target Converter efficiency: η = 0.75
- Window utilization factor: K_U = 0.4
- Current density (A/m^2): $J_C = 500 \times 10^4$

Calculate the total output power, P_{OUT}:

$$P_{OUT} = \left(V_{O1} + V_{D1}\right) \times I_{O1} + \left(V_{O2} + V_{D2}\right) \times I_{O2} + \left(V_{O3} + V_{D3}\right) \times I_{O3} = 8.995\ W \quad (1)$$

Calculate transformer primary-to-secondary turns ratio, N_{PS}:

$$N_{PS} = \frac{D_{MAX} \times V_{MIN}}{0.425 \times \left(V_{O1} + V_{D1}\right)} = 7.911 \quad (2)$$

Calculate the primary peak current, I_{PK}, and the primary RMS current, I_{PRMS}, using the main secondary peak current, I_{SPK}:

$$I_{SPK} = \frac{\frac{P_{OUT}}{V_{O1}} \times 2}{0.425} = 4.233\ A \quad (3)$$

$$I_{PK} = \frac{I_{SPK}}{N_{PS}} = 0.535\ A \quad (4)$$

$$I_{PRMS} = I_{PK} \times \sqrt{D_{MAX} \times \left(\frac{K_{RP}^2}{3} - K_{RP} + 1\right)} = 0.304\ A \quad (5)$$

Calculate the primary inductance (H), L_P:

$$L_P = \frac{P_{OUT} \times 2}{\left(I_{PK} \times 1.05\right)^2 \times f_{TARGET(MAX)} \times \eta} = 0.95\ mH \quad (6)$$

Calculate the area product (mm^4), A_P:

$$AP = \frac{2 \times I_{PRMS} \times I_{PK} \times K_{RP} \times L_P}{J_C \times K_U \times (2 \times B_{AC})} \times 10^{12} = 412.42 \text{ mm}^4 \quad (7)$$

Select a proper core from core database according to AP, Select the Core size is EE16, and the real AP value is A_{PREAL} = 801 mm^4.

Calculate the primary winding turns, N_P:

$$N_P = \frac{L_P \times I_{PK} \times 1.05}{B_{MAX} \times A_E} = 88 \quad (8)$$

Calculate the three output winding turns, N_{S1}, N_{S2}, and N_{S3}:

$$N_{S1} = \frac{N_P \times (V_{O1} + V_{D1}) \times 0.425}{D_{MAX} \times V_{MIN}} = 11 \quad (9)$$

$$N_{S2} = \frac{N_P \times (V_{O2} + V_{D2}) \times 0.425}{D_{MAX} \times V_{MIN}} = 6 \quad (10)$$

$$N_{S3} = \frac{N_P \times (V_{O3} + V_{D3}) \times 0.425}{D_{MAX} \times V_{MIN}} = 17 \quad (11)$$

Calculate the real maximum flux density, B_{MAX_REAL}:

$$B_{MAX\_REAL} = \frac{L_P \times I_{PK}}{N_P \times A_E} = 0.284 \quad (12)$$

Because $B_{MAX\_REAL} < B_{MAX}$, this transformer will not saturate even at the worst case.

4.2.2 Selecting Input Bulk Capacitance

The minimum input capacitance voltage, the input power of the converter based on target full-load efficiency, minimum input RMS voltage, and minimum AC input frequency determine the input capacitance requirement.

The maximum converter input power can be estimated from the output voltage in the CV mode (V_{OCV}), the converter's output current when operating in CC mode (I_{OCC}), and the full-load target efficiency (η).

$$P_{IN} = \frac{V_{OUT1} \times I_{OUT1} + V_{OUT2} \times I_{OUT2} + V_{OUT3} \times I_{OUT3}}{\eta}$$

$$P_{IN} = \frac{5 \times 0.05 + 15 \times 0.05 + 10 \times 0.75}{0.8} = 10.625 \text{ W} \quad (13)$$

Equation 14 provides an accurate solution for input capacitance based on a target minimum bulk capacitor voltage ($V_{BULK(MIN)}$). To target a given input capacitance value, iterate the minimum capacitor voltage to achieve the target capacitance.

$$C_{BULK} = \frac{\frac{2 \times P_{IN}}{f_{LINE(MIN)}} \times \left(\frac{1}{RCT} - \frac{1}{2 \times \pi} \times \arccos\left(\frac{V_{BULK(MIN)}}{\sqrt{2} \times V_{IN(MIN)}} \right) \right)}{\sqrt{2} \times V_{IN(MIN)}^2 - V_{BULK(MIN)}^2} \quad (14)$$

As shown in Figure 2, the reference design has a full wave bridge rectifier at the input. The voltage $V_{BULK(MIN)}$ is generally selected around 65% to 60% of $\sqrt{2} \times V_{IN(MIN)}$. With these considerations:

$$C_{BULK} = \frac{\frac{2 \times 10.625}{47} \times \left(\frac{1}{2} - \frac{1}{2 \times \pi} \times \arccos\left(\frac{75}{120} \right) \right)}{2 \times 85^2 - 75^2} = 18.3 \text{ µF}$$

Taking into account that electrolytic capacitance with 10% of tolerance, the values selected for C1 and C2 are: C1 = C2 = 10 µF.

The maximum DC bus voltage is 380 V. Therefore, a 400-V/450-V capacitor is a good choice.

4.2.3 Selecting Output Capacitance

The output capacitor value is typically determined by the transient response requirement from no load (for example, to maintain a minimum output voltage of 9 V with a load-step transient from 0 to 750 mA (I_{TRAN})). Equation 15 assumes that at no load the converter is operating at the minimum switching frequency ($f_{SW(MIN)}$).

$$C16 = \frac{I_{TRAN}}{V_{out\Delta} \times f_{SW(MIN)}} = \frac{750\ mA}{(10-9) \times 420} = 1786\ \mu F \quad (15)$$

A margin of 20% is added to the output capacitance, so the values selected for C16 is 2200 µF.

4.2.4 VDD Capacitance for UCC28911

The capacitance on VDD of the UCC28911 needs to supply the device operating current until the output of the converter reaches the target minimum operating voltage in CC regulation. At this time, the auxiliary winding can sustain the supply voltage. The output current available to the load to charge the output capacitors is the CC regulation target. Equation 16 assumes the output current of the flyback is available to charge the output capacitance until the minimum output voltage is achieved. In Figure 2, C3 is provided as the V_{DD} capacitor.

$$C_{VDD} = \frac{C_{OUT} \times V_{OCC} \times I_{RUN(MAX)}}{I_{OCC} \times \Delta V_{UVLO}} \quad (16)$$

Where

- ΔV_{UVLO} is UVLO hysteresis, equal to $V_{DDON} - V_{DDOFF}$
- $I_{RUN(MAX)}$ is supply current required at V_{DD}

The ΔV_{UVLO} and $I_{RUN(MAX)}$ can be found in the datasheet of the UCC28911 (SLUS769). In this reference design, the values are selected as ΔV_{UVLO} = 3 V, $I_{RUN(MAX)}$ = 3.4 mA .

Substituting the values in Equation 16,

$$C3 = \frac{2200\ \mu F \times 5\ V \times 3.4\ mA}{0.75\ A \times 3\ V} = 16.6\ \mu F \quad (17)$$

10 µF is selected for C3, which is the nearest low value capacitor compared to 16.6 µF, to ensure a low start-up time.

4.2.5 Bridge Rectifier

The maximum input AC voltage is 270-V AC, so the DC voltage can reach voltage levels of up to 385-V DC. Considering a safety factor of 30%, select a component with voltage rating greater than 500-V DC. The input bridge rectifier must have an average current capability that exceeds the input average current ($I_{IN\_AVG(MAX)}$). To optimize the power loss due to the diode forward voltage drop, a bridge rectifier with higher current rating is recommended.

To get the $I_{IN\_AVG(MAX)}$, first calculate the maximum input RMS line current, $I_{IN\_RMS(MAX)}$.

$$I_{IN\_RMS(MAX)} = \frac{P_{IN}}{V_{IN(MIN)} \times PF} = \frac{10.625}{85 \times 0.6} = 0.208 \text{ A} \tag{18}$$

Based upon the calculated RMS values, the maximum input current, $I_{IN(MAX)}$, and the maximum average input current, $I_{IN\_AVG(MAX)}$, can be determined by assuming the waveform is sinusoidal, as shown in Equation 19 and Equation 20:

$$I_{IN(MAX)} = \sqrt{2} \times I_{IN\_RMS(MAX)} = \sqrt{2} \times 0.208 = 0.294 \text{ A} \tag{19}$$

$$I_{IN\_AVG(MAX)} = \frac{2}{\pi} \times I_{IN(MAX)} = \frac{2}{\pi} \times 0.294 = 0.187 \text{ A} \tag{20}$$

Considering the operating environment temperature and current margin, select DF06M for the D1. The forward voltage drop of DF06M is V_{F_BRIDGE} = 0.8 V.

Therefore, the power loss in the input bridge, P_{BRIDGE}, can be calculated as:

$$P_{BRIDGE} = 2 \times V_{F\_BRIDGE} \times I_{IN\_AVG(MAX)} = 2 \times 0.8 \times 0.187 = 0.299 \text{ W} \tag{21}$$

4.2.6 Output Voltage Set Point

The UCC28911 VS Signal Discriminator Block ensures an accurate sampling time for an accurate sample of the output voltage from the auxiliary winding. However, there are some details of the auxiliary winding signal to ensure reliable operation, specifically the reset time of the leakage inductance and the duration of any subsequent leakage inductance ring.

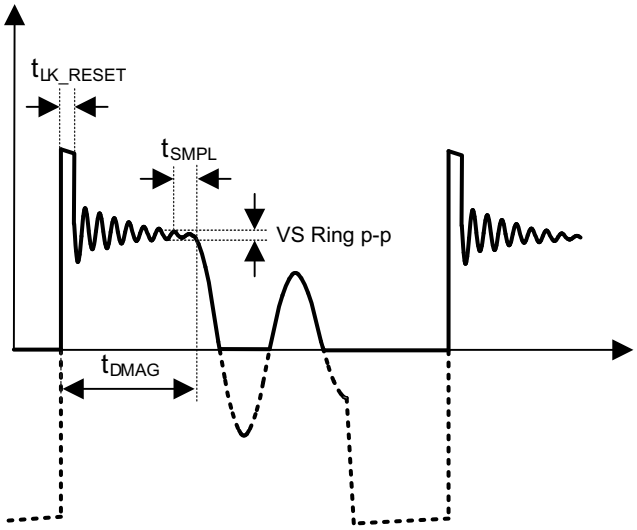


Figure 3. VS Voltage

The first detail to examine is the duration of the leakage inductance reset pedestal, t_{LK_RESET}. Because this can mimic the waveform of the secondary current decay, followed by a sharp down-slope, keep the leakage reset time less than 500 ns for I_{DRAIN} minimum, and less than 1.5µs for I_{DRAIN} maximum. The second detail is the amplitude of ringing on the auxiliary winding waveform (V_{AUX}) following t_{LK_RESET}. The peak-to-peak voltage at the VS pin should be less than approximately 100mVp-p at least 200 ns before the end of the demagnetization time, t_{DMAG}. If there is a concern with excessive ringing, it usually occurs during light or no-load conditions when t_{DMAG} is at the minimum. The tolerable ripple on VS is scaled up to the auxiliary winding voltage by R6 and R4 and is equal to 100 (R6 + R4) / R4 mV. So the VS divider resistors determine the output voltage regulation point of the flyback converter. Also, the high-side divider resistor (R6) determines the line voltage at which the controller enables continuous switching operation. R6 is initially determined based on transformer auxiliary to primary turn ratio and desired input voltage operating threshold.

$$R6 = \frac{V_{IN\_UVLO} \times \sqrt{2}}{N_{PA} \times I_{VSLRUN(MAX)}} \tag{22}$$

Where $I_{VSLRUN(MAX)}$ is the VS line sense run current (found in the datasheet of UCC28911)., The typical value of $I_{VSLRUN(MAX)}$ is 260 µA, so

$$R6 = \frac{75 \times \sqrt{2}}{5.17 \times 260\ \mu A} = 78.77k$$

In this reference design, the selected value of R6 is 76.8k. The low-side VS pin resistor R4 is selected based on desired output voltage regulation.

$$R4 = \frac{V_{VSR} \times R6 \times N_{PA}}{\left(V_{OUT} + V_F\right) \times N_{PS} - \left(V_{VSR} \times N_{PA}\right)} \tag{23}$$

Where V_{VSR} is the regulating level of VS pin (found in the datasheet of UCC28911). Usually, the typical value of V_{VSR} is 4.05 V.

$$R4 = \frac{4.05 \times 76.8 \times 5.17}{(10 + 0.5) \times 8 - (4.05 \times 5.17)} = 25.54k$$

In this reference design, the selected values of R4 and R7 are 27k and 510k, respectively.

4.2.7 Output Power Set Point

A resistance (R_{IPK}) connected between IPK pin and GND sets the maximum value of the power FET peak current, $I_{D\_PK(MAX)}$. A current, I_{SENSE}, proportional to the power FET current, comes out from the IPK pin during power FET on time. The voltage across R_{IPK} is fed to the PWM comparator and establishes to switch off the power FET according to Equation 24:

$$I_{D\_PK(MAX)} = \frac{V_{CSTE(MAX)}}{R_{IPK}} \tag{24}$$

Where $V_{CSTE(MAX)}$ is the equivalent current sense threshold, which can be found in the datasheet of UCC28911. From that datasheet, the maximum value of $V_{CST(MAX)}$ is 640 V at a V_{VS} of 3.75 V. If the IPK pin is shorted to GND (R_{IPK} = 0), the peak current is automatically set to $I_{D\_PEAK(MAX)}$, 700 mA for UCC28911.

A test is performed at device start-up to check whether the IPK pin is shorted to GND or the R_{IPK} is present. If R_{IPK} is less than maximum R_{IPK_SHORT}, the device interprets it as a short (R_{IPK} = 0) and the DRAIN peak current is set to $I_{D\_PEAK(MAX)}$. Otherwise, if R_{IPK} is greater than minimum $R_{IPK(MIN)}$, the device sets the DRAIN peak current according to Equation 24. A value of R_{IPK} that is in between the before said values are not allowed since the value of the peak current may be selected using either of the two sense resistances: the internal sense resistance and R_{IPK}.

In this reference, the R10 and R11 can be calculated by Equation 25:

$$R_{IPK} = \frac{640}{0.521 \times 110\%} = 1.12k \tag{25}$$

Considering the accuracy and environmental implication, place a margin of 10%, so the selected value of R10 and R11 are 1.6k and 3.6k.

4.2.8 Output Rectifier Diode Selection

The maximum reverse voltage that the secondary diode had to sustain can be calculated by Equation 26 where a margin of 50% is considered. Usually for this kind of application, a Schottky diode reduces the power losses due to the lower forward voltage drop. The maximum current rating of the diode is generally selected between two to five times the maximum output current (I_{OCC}).

$$V_{REV} = \left(V_{OUT} + \frac{V_{IN(MAX)} \times \sqrt{2}}{N_{PS}} \right) \times 1.5 = \left(10 + \frac{270 \times \sqrt{2}}{8} \right) \times 1.5 = 86 \text{ V} \tag{26}$$

In this reference design, the PDS5100-13 (100-V, 5-A Schottky) is selected as the secondary rectifier diode D7.

4.2.9 Pre-Load Calculation

When no load is applied on the converter output, the output voltage rises until the overvoltage protection (OVP) of the device is tripped, because the device cannot operate at zero switching frequency. The device's minimum switching frequency of 420 Hz will always deliver some energy to the output, causing the voltage to rise at no load. To avoid this, an R_{PRL} (pre-load resistance) must be used. The value of this pre-load can be selected using the following equation:

$$R_{PRL} = \frac{V_{OUT}^2}{\frac{1}{2} \times L_P \times f_{SW(MIN)} \times \left(\frac{I_{D\_PK(MAX)}}{K_{AM}}\right)^2 - VDD_{OFF(MIN)} \times I_{WAITQ(MIN)}} \quad (27)$$

where

- K_{AM} is AM control ratio, $K_{AM} = V_{CSE(MAX)} / V_{CSE(MIN)}$ (found in datasheet of UCC28911)
- $I_{WAITQ(MIN)}$ is quiescent wait supply current; in the UCC28911 datasheet, this is usually set as 190 µA
- $V_{DDOOF(MIN)}$ is V_{DD} turn-off threshold (found in datasheet of UCC28911)

So in this reference design, the pre-load resistance can be calculated by:

$$R13 = \frac{10^2}{\frac{1}{2} \times 0.97 \times 10^{-3} \times 420 \times \left(\frac{0.521}{3}\right)^2 - 7 \times 190 \times 10^{-6}} = 16.28k$$

In this reference design, the selected value of R13 is 6.8k.

4.2.10 Primary Drain Voltage Clamp Circuit

As in most flyback converters, the main purpose of drain voltage clamp circuit is to prevent the DRAIN voltage from rising up to the FET break-down voltage, at the FET turn-off, and destroying the FET itself (see Figure 4). An additional task, required by the primary-side regulation mechanism, is to provide a clean input to the VS pin by damping the oscillation that is typically present on the DRAIN voltage due to the transformer primary leakage inductance.

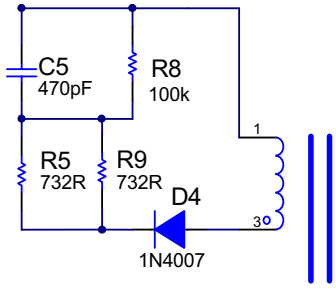


Figure 4. Drain Clamp Circuit Options

To perform damping, the diode D4 (see Figure 4) selected should not be a fast recovery diode (0.3 µs < t_{rr} < 1 µs) so the reverse current can flow in the RLC over damped circuit. This RLC circuit is formed by the transformer primary-leakage inductance (L_{LKP}), the resistances R5, R8, and R9, and the capacitance C5. To ensure proper damping, the resistance R5 has to satisfy the following condition:

$$R5 > 2 \times \sqrt{\frac{L_{LKP}}{C5}} \quad (28)$$

The capacitance C5 should not be too high, so it does not require too much energy to be charged. Typical values for C5 are between 100 pF and 1 nF.

The resistance R8 has been added to discharge the C5 capacitance, so at the next switching cycle diode D4 is activated to provide enough current and storage to have a reverse-recovery current large enough for proper oscillation damping.

5 Getting Started: Hardware

5.1 Test Conditions

Figure 5 shows the basic test setup recommended for evaluating the TIDA-00473 during no load and full load. During the no load test, set the power analyzer for long averaging to include several cycles of operation and an appropriate current scale factor should be used.

For input, the AC source (V_{IN}) must range from 50-V to 270-V AC. Set the Input current limit of input AC source to 1 A. For output, use an electronic variable load or a variable resistive load, which must be rated for ≥ 400 V and vary the load current from 0 mA to 1 A.

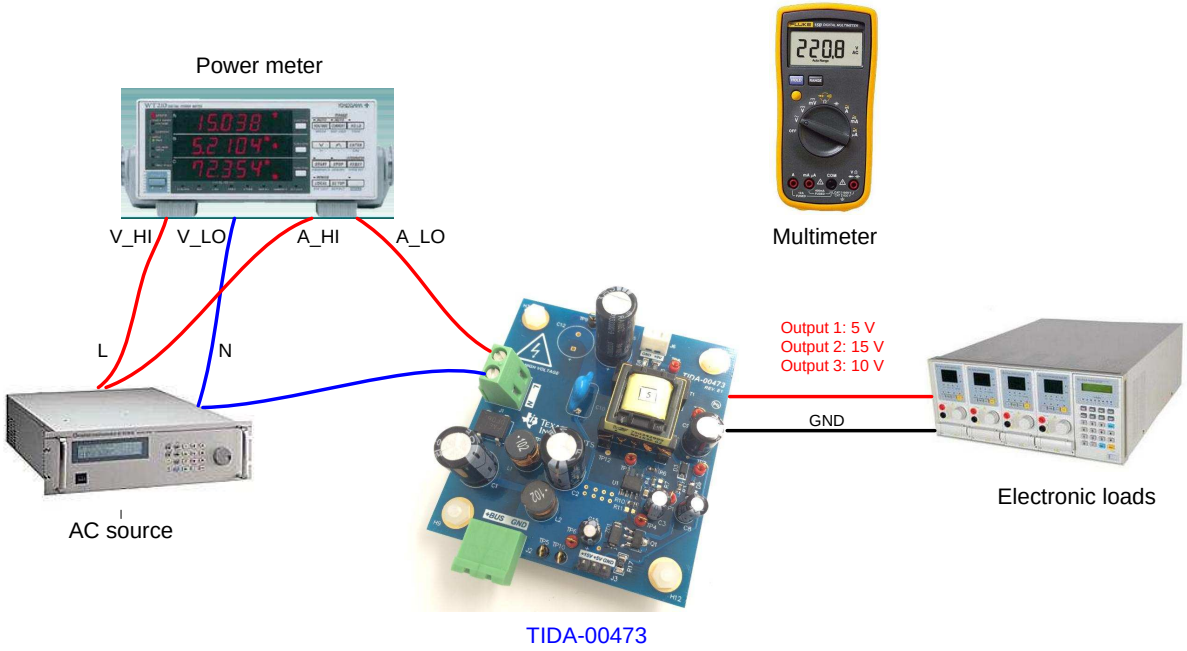


Figure 5. Test Environment Setup Recommended

5.2 Equipment Needed

- Isolated AC source: The input source must be an isolated variable AC source capable of supplying between 50-V and 270-V_{RMS} at no less than 25 W and connected as shown in Figure 5. For accurate efficiency calculations, insert a power meter between the AC source and the TIDA-00473. For highest accuracy, connect the voltage terminals of the power meter directly across the power source. (Connecting the voltage terminals directly to the TIDA-00473 will result in a small current error which is significant when measuring no load power.)
- Loads: Use a programmable electronic loads with three outputs set to constant resistance mode and capable of sinking 0 to 1-A DC at 20-V DC.
- Power meter: The power analyzer is capable of measuring low input current, typically less than 100 µA, and a long averaging mode if input power measurements of the low-power standby mode are to be taken. An example of such an analyzer is the Yokogawa WT210 Digital Power Meter. To measure the intermittent bursts of current and power drawn from the line during no-load operation, set the WT210 to integrate.
- Multimeter: Digital multimeters measure the regulated output voltages (DMM V_1, DMM V_2, and DMM V_3) and load current (DMM A_1, DMM A_2, and DMM A_3).
- Oscilloscope: A digital or analog oscilloscope with a 100-MHz scope probe is recommended.
- Recommended wire gauge: a minimum of AWG 24-wire is recommended. The wire connections between the AC source and the TIDA-00473 and the wire connections between the reference design board and the load should be less than two feet long.

5.3 Test Procedure

The following test procedure is recommended primarily for powering up and shutting down the TIDA-00473. Never leave a powered TIDA-00473 evaluated board unattended for a long time.

5.3.1 Applying Power to the TIDA-00473

1. Set up the TIDA-00473 evaluated board as shown in Figure 5.
   (a) If no load input power measurements are to be made, set the power analyzer to long averaging or integrating power measurement mode.
   (b) For operation with a load, as shown in Figure 5, set the electronic load to constant resistance mode. Adjust the resistance setting in the electronic load for changing the load.
2. Prior to turning on the AC source, set the voltage to between 85-V and 270-V AC.
3. Turn on the AC source.
4. Monitor the output voltage on DMM V_1, V_2, and V_3
5. Monitor the output current on DMM A_1, A_2, and A_3

5.3.2 Output Voltage Regulation and Efficiency

1. For load regulation:
   (a) Use the test setup shown in Figure 5.
   (b) Set the AC source to a constant voltage between 85-V and 265-V AC.
   (c) Apply power to the TIDA-00473 per Section 5.3.1.
   (d) Vary the load current from 0 A up to 0.75 A.
2. For line regulation:
   (a) Set the load to sink full load.
   (b) Vary the AC source from 85-V to 265-V AC.
3. Make sure the input power is off and the bulk capacitor and output capacitors are completely discharged before handling the TIDA-00473 evaluated board.

5.3.3 Equipment Shutdown

1. Ensure the load is at maximum; this will quickly discharge the output capacitors.
2. Turn off the AC source.
3. Make sure the bulk capacitors and output capacitors are completely discharged before handling the TIDA-00473 evaluated board.

6 Test Results

The test results are divided in multiple sections that cover the steady state performance measurements, functional performance waveforms and test data, transient performance waveforms, thermal measurements, conducted emission measurements, and surge and EFT measurements.

6.1 Performance Data

6.1.1 Cross Regulation With Load Variation

Table 3 shows the cross regulation data at 230-V AC input, where the data V_{15A} means 15-V voltage monitored after the LDO circuit (at TP6), and the V_{15B} means 15-V voltage monitored before LDO circuit (across C8).

Table 3. Cross Regulation With Load Variation at 230-V AC Input

V_5 (V)	I_5 (A)	V_{15A} (V)	V_{15B} (V)	I_{15} (A)	V_{10} (V)	I_{10} (A)
4.65	0	14.28	15.05	0	10.26	0
4.69	0	14.25	14.95	0	9.81	0.01
4.94	0	14.39	15.47	0	9.78	0.05
5.04	0	14.41	15.74	0	9.8	0.1
5.15	0	14.45	16.06	0	9.81	0.2
5.27	0	14.46	16.44	0	9.82	0.3
5.41	0	14.51	16.84	0	9.83	0.4
5.56	0	14.55	17.3	0	9.84	0.5
5.72	0	14.59	17.79	0	9.85	0.6
5.95	0	14.69	18.36	0	9.86	0.75
4.69	0.05	14.54	16.19	0	11.7	0
4.66	0.05	14.49	16.1	0	10.81	0.01
4.67	0.05	14.43	15.57	0	10.01	0.05
4.75	0.05	14.44	15.52	0	9.81	0.1
4.83	0.05	14.47	15.83	0	9.8	0.2
4.9	0.05	14.5	16.14	0	9.82	0.3
4.96	0.05	14.52	16.47	0	9.83	0.4
5.01	0.05	14.55	16.81	0	9.84	0.5
5.06	0.05	14.57	17.15	0	9.84	0.6
5.15	0.05	14.65	17.52	0	9.86	0.75
5.01	0	13.75	14.64	0.05	13.01	0
4.92	0	13.84	14.68	0.05	10.52	0.01
4.9	0	13.82	14.68	0.05	9.86	0.05
4.91	0	13.83	14.72	0.05	9.74	0.1
5.07	0	14.07	15.01	0.05	9.8	0.2
5.1	0	14.25	15.27	0.05	9.82	0.3
5.17	0	14.32	15.44	0.05	9.83	0.4
5.23	0	14.36	15.61	0.05	9.84	0.5
5.29	0	14.39	15.76	0.05	9.85	0.6
5.38	0	14.46	15.98	0.05	9.87	0.75
4.71	0.05	13.91	14.83	0.05	13.4	0
4.681	0.05	14.02	14.85	0.05	10.77	0.01
4.7	0.05	13.98	14.81	0.05	9.94	0.05
4.73	0.05	13.9	14.79	0.05	9.81	0.1
4.81	0.05	14.07	15	0.05	9.79	0.2
4.88	0.05	14.21	15.22	0.05	9.82	0.3

Table 3. Cross Regulation With Load Variation at 230-V AC Input (continued)

V_5 (V)	I_5 (A)	V_{15A} (V)	V_{15B} (V)	I_{15} (A)	V_{10} (V)	I_{10} (A)
4.93	0.05	14.29	15.4	0.05	9.83	0.4
4.98	0.05	14.33	15.56	0.05	9.84	0.5
5.02	0.05	14.37	15.69	0.05	9.85	0.6
5.09	0.05	14.45	15.88	0.05	9.87	0.75

6.1.2 Regulation With Line Variation (AC Input)

Table 4 shows the data for the line regulation of the output with AC input voltage variation.

Table 4. Regulation With Line Variation at Full Load

INPUT VOLTAGE (VAC)	V_5 (V)	I_5 (A)	V_{15A} (V)	V_{15B} (V)	I_{15} (A)	V_{10} (V)	I_{10} (A)
90	5.14	0.05	14.51	16.16	0.05	9.84	0.75
120	5.14	0.05	14.51	16.11	0.05	9.86	0.75
150	5.11	0.05	14.37	16.03	0.05	9.87	0.75
180	5.1	0.05	14.45	15.97	0.05	9.87	0.75
220	5.08	0.05	14.4	15.89	0.05	9.87	0.75
250	5.07	0.05	14.43	15.84	0.05	9.87	0.75
270	5.07	0.05	14.36	15.8	0.05	9.87	0.75

Table 5. Regulation With Line Variation at No Load

INPUT VOLTAGE (VAC)	V_5 (V)	I_5 (A)	V_{15A} (V)	V_{15B} (V)	I_{15} (A)	V_{10} (V)	I_{10} (A)
90	4.69	0	14.26	14.95	0	10.01	0
120	4.7	0	14.29	14.95	0	10.03	0
150	4.68	0	14.25	14.96	0	10.06	0
180	4.68	0	14.29	14.97	0	10.05	0
220	4.68	0	14.26	14.98	0	10.06	0
250	4.68	0	14.3	14.99	0	10.05	0
270	4.68	0	14.28	14.99	0	10.07	0

6.1.3 Standby Power

The standby power was tested at multiple AC input voltages with only a pre-load on output. The results are tabulated in Table 6.

Table 6. No Load Power Measurement

INPUT VOLTAGE (VAC)	INPUT CURRENT (mA)	STANDBY POWER (mW)
90	0.603	30.4
120	0.618	34
150	0.479	36.8
180	0.496	47
230	0.449	58
270	0.522	73

6.1.4 Efficiency Test

The efficiency was tested at 115-V AC and 230-V AC input voltages with full load on output. The results are tabulated in Table 7.

Table 7. Efficiency Test at 115-V AC Input

LOAD (%)	P_{IN} (W)	V_5 (V)	I_5 (A)	V_{15} (V)	I_{15} (A)	V_{10} (V)	I_{10} (A)	P_{OUT} (W)	EFFICIENCY (%)
100	10.31	5.146	0.0499	14.5	0.0505	9.94	0.749	8.43	81.77
75	7.85	5.155	0.0375	14.58	0.0375	9.92	0.573	6.42	81.83
50	5.25	5.113	0.0249	14.55	0.0255	9.9	0.38	4.26	81.13
25	2.65	5.03	0.0124	14.49	0.0125	9.89	0.186	2.08	78.55
10	1.12	4.961	0.0049	14.45	0.0055	9.88	0.0754	0.85	75.71
0	0.04	4.7	0	14.37	0	10.27	0	0	0

Table 8. Efficiency Test at 230-V AC Input

LOAD (%)	P_{IN} (w)	V_5 (V)	I_5 (A)	V_{15} (V)	I_{15} (A)	V_{10} (V)	I_{10} (A)	P_{OUT} (w)	EFFICIENCY (%)
100	10.19	5.117	0.0499	14.55	0.0505	9.94	0.75	8.45	82.91
75	7.76	5.123	0.0375	14.54	0.0375	9.93	0.574	6.44	83
50	5.21	5.1	0.0249	14.51	0.0255	9.91	0.38	4.26	81.82
25	2.67	5.08	0.0124	14.48	0.0125	9.88	0.185	2.07	77.57
10	1.11	5.01	0.0049	14.43	0.0055	9.87	0.0754	0.85	76.41
0	0.048	4.698	0	14.39	0	10.3	0	0	0

6.2 Performance Curves

6.2.1 Cross Regulation With Load Variation

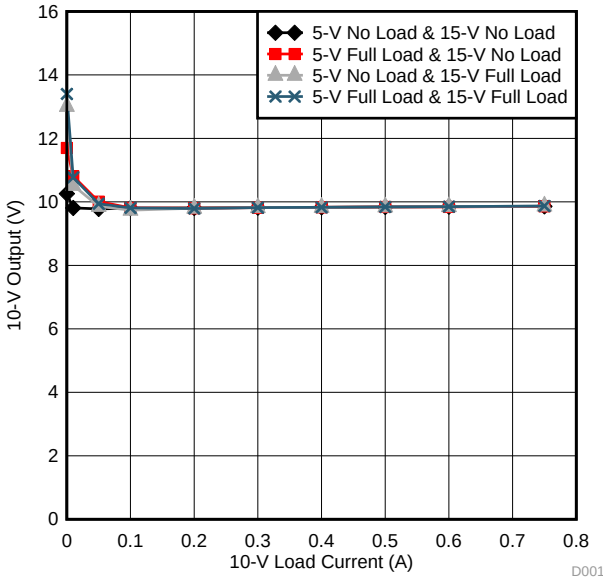


Figure 6. Cross Regulation at 10-V Output With 5-V and 15-V Load Parameter

6.2.2 Regulation With Line Variation (AC Input)

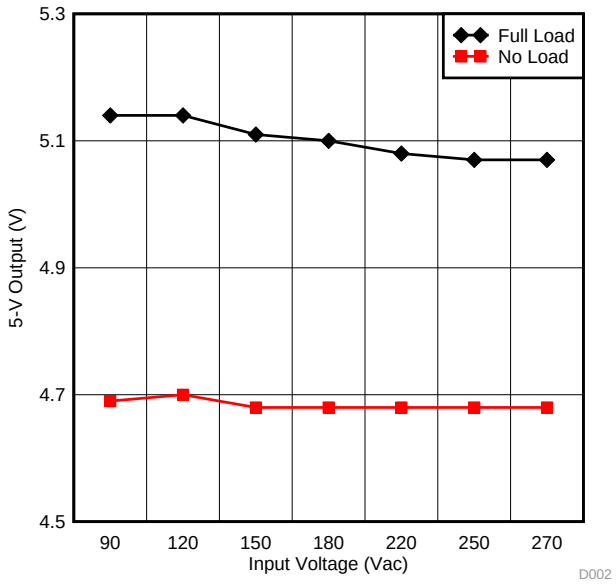


Figure 7. Line Regulation at 5-V Output With Full Load and No Load

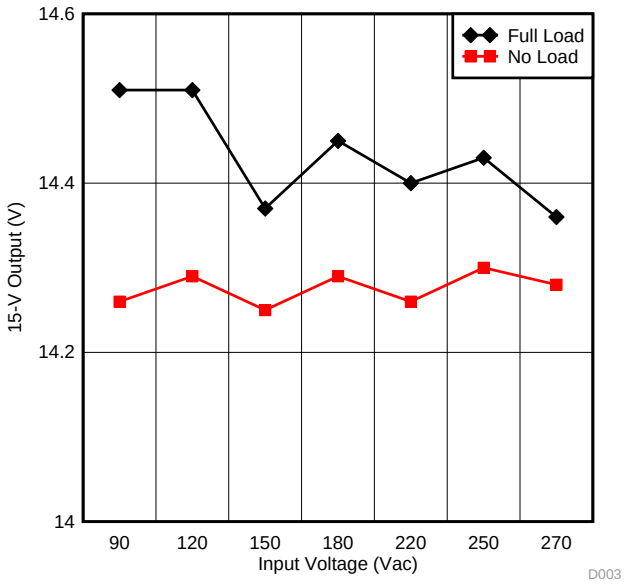


Figure 8. Line Regulation at 15-V Output With Full Load and No Load

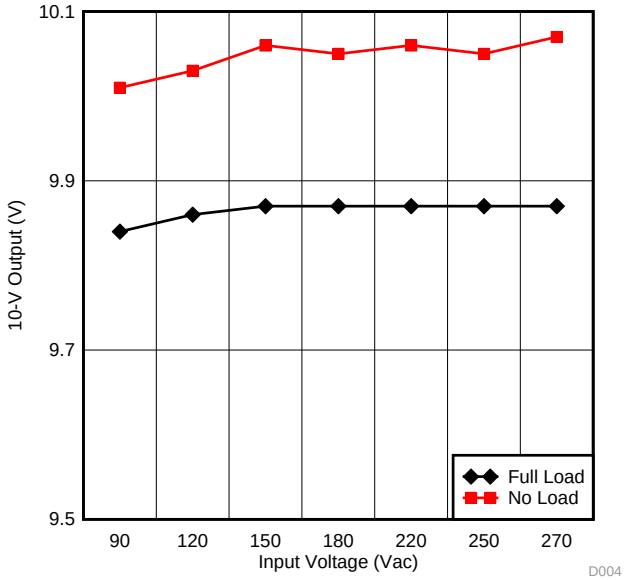


Figure 9. Line Regulation at 10-V Output With Full Load and No Load

6.2.3 Efficiency

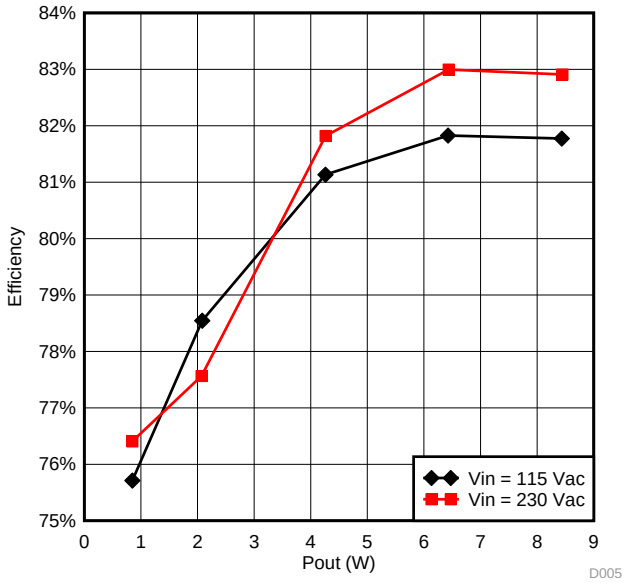


Figure 10. Efficiency Curves at 115-V AC and 230-V AC Inputs

6.3 Functional Waveforms

6.3.1 V_{DS} Switching Node Waveforms

Waveform at switching node (V_{DS}) was observed for 115-V AC and 270-V AC input under full load conditions.

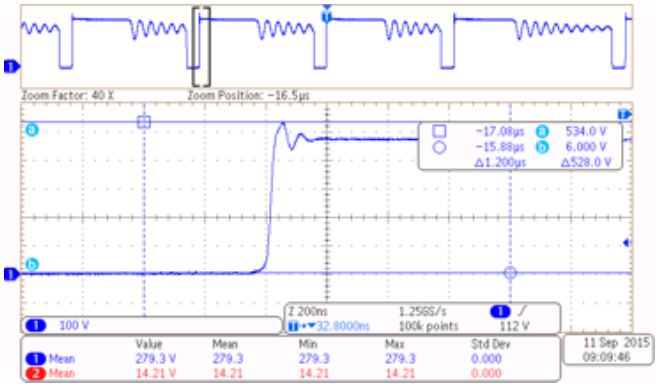


Figure 11. V_{DS} Waveform at V_{IN} = 270-V AC, Full Load

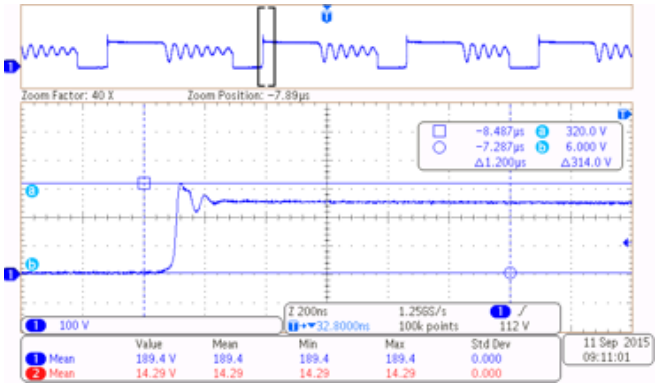


Figure 12. V_{DS} Waveform at V_{IN} = 115-V AC, Full Load

From the test result of the V_{DS} switching waveform, at V_{IN} = 270-V AC (the maximum input voltage), the peak V_{DS} voltage is only 528-V DC. This voltage is far below of the V_{DRAIN} maximum voltage stress of 700-V DC, so the voltage safety margin is satisfactory.

6.3.2 Start-up Time Waveform

Figure 13 shows the input current waveform at 230-V AC and with full load condition.

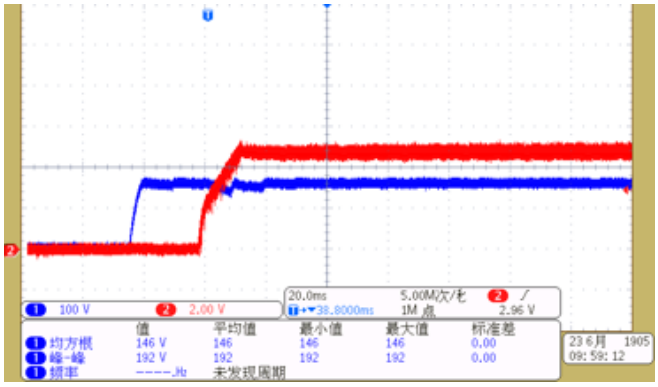


Figure 13. Start-up Time Under 115-V AC Input

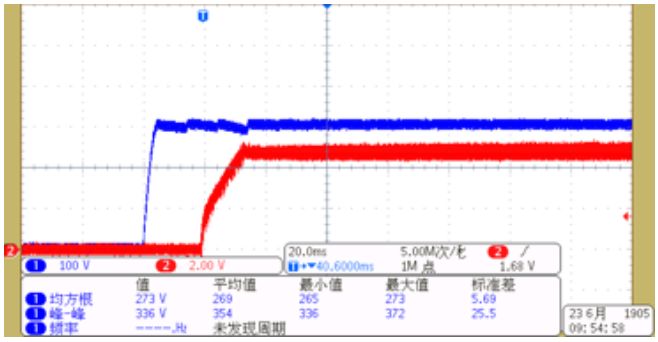


Figure 14. Start-up Time Under 230-V AC Input

NOTE: Channel 1 (Yellow trace): DC bus voltage, 100 V/div; Channel 2 (Blue trace): 5-V output voltage, 2V/div

6.3.3 Output Voltage Ripple

The output voltage ripple is observed at full load using an oscilloscope bandwidth of 20 MHz.

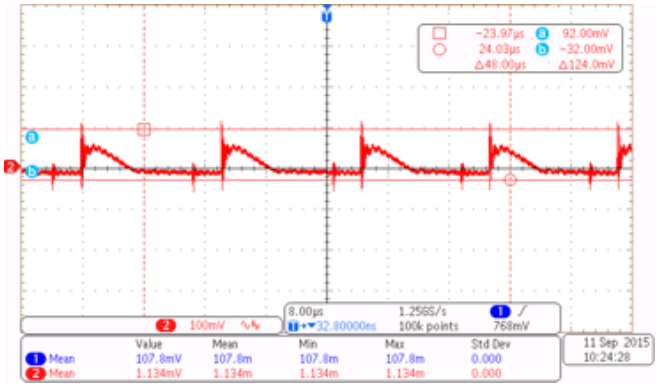


Figure 15. 10-V Output Voltage Ripple at Full Load

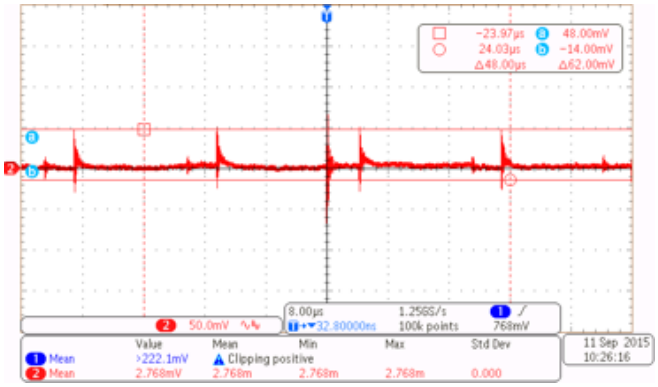


Figure 16. 15-V Output Voltage Ripple at Full Load

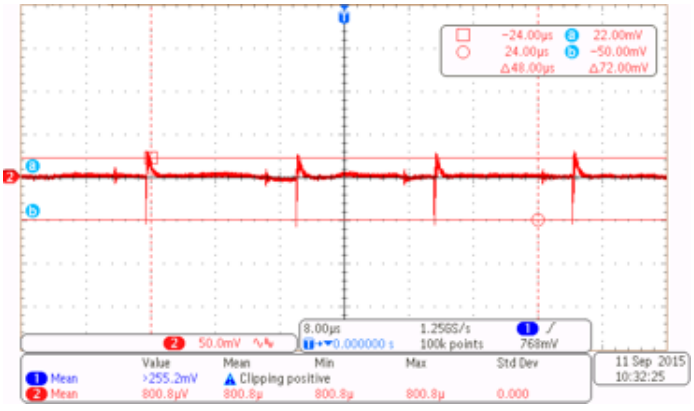


Figure 17. 5-V Output Voltage Ripple at Full Load

6.4 Transient Waveforms

6.4.1 Transient Load Response

For Figure 18 to Figure 20, V_{IN} = 230-V AC, and the load transient goes from no load to full load. The output load is switched using electronic load. Also, the red trace is the output voltage, 20 V/div, AC coupling, and the green trace is the output current, 1 A/div.

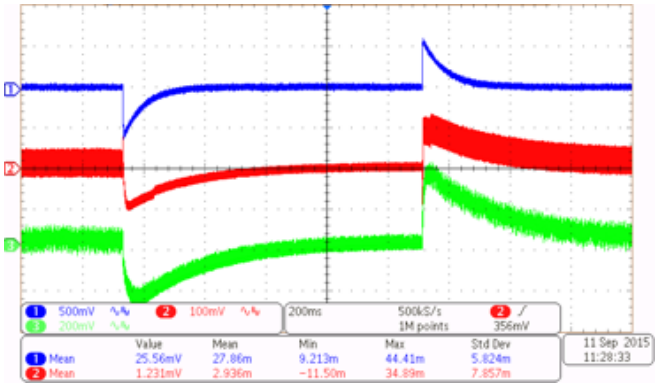


Figure 18. Step Load at 10-V Output (0.1 to 0.75 A)

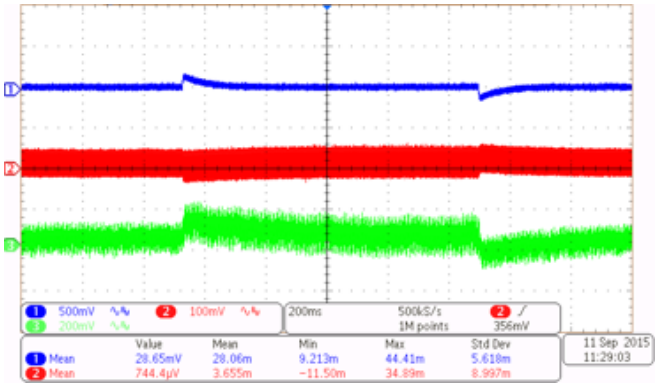


Figure 19. Step Load at 15-V Output (0 to 0.05 A)

NOTE: CH1 (15 V) 0.5 A/div, CH2 (10 V) 0.1 V/div, CH3 (5 V) 0.2 V/div

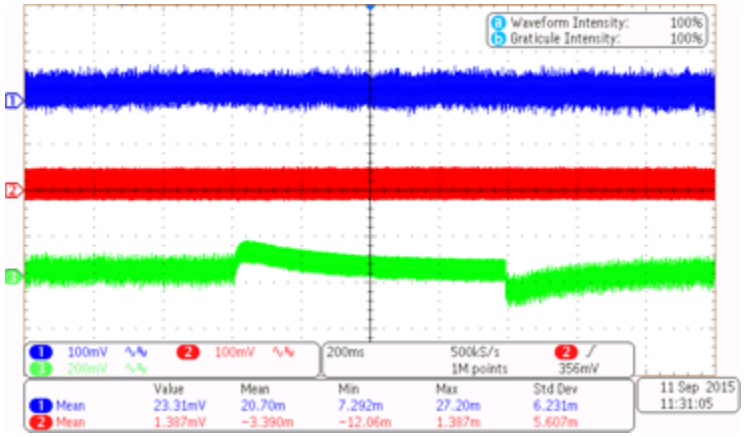


Figure 20. Step Load 5 V (0 to 0.05 A)

NOTE: CH1 (15 V) 0.1 A/div, CH2 (10 V) 0.1 V/div, CH3 (5 V) 0.2 V/div

6.5 Conducted Emissions

The conducted emission test of TIDA-00473 is done at full load condition.

6.5.1 TIDA-00473 Board With Resistive Load at Output

This test uses 230-V AC inputs with the full load connected to PSU with short leads. The conducted emissions in a pre-compliance test setup were compared against EN55022 class B limits and found to meet them Comfortably

The conducted emission test uses a pre-compliance meter as per the standard EN55022 class B limit. The test result shows that the board is passing the test with a good margin.

NOTE: The conduction emission results captured in Figure 21 are average and peak. The limits specified in the standard are average and quasi-peak.

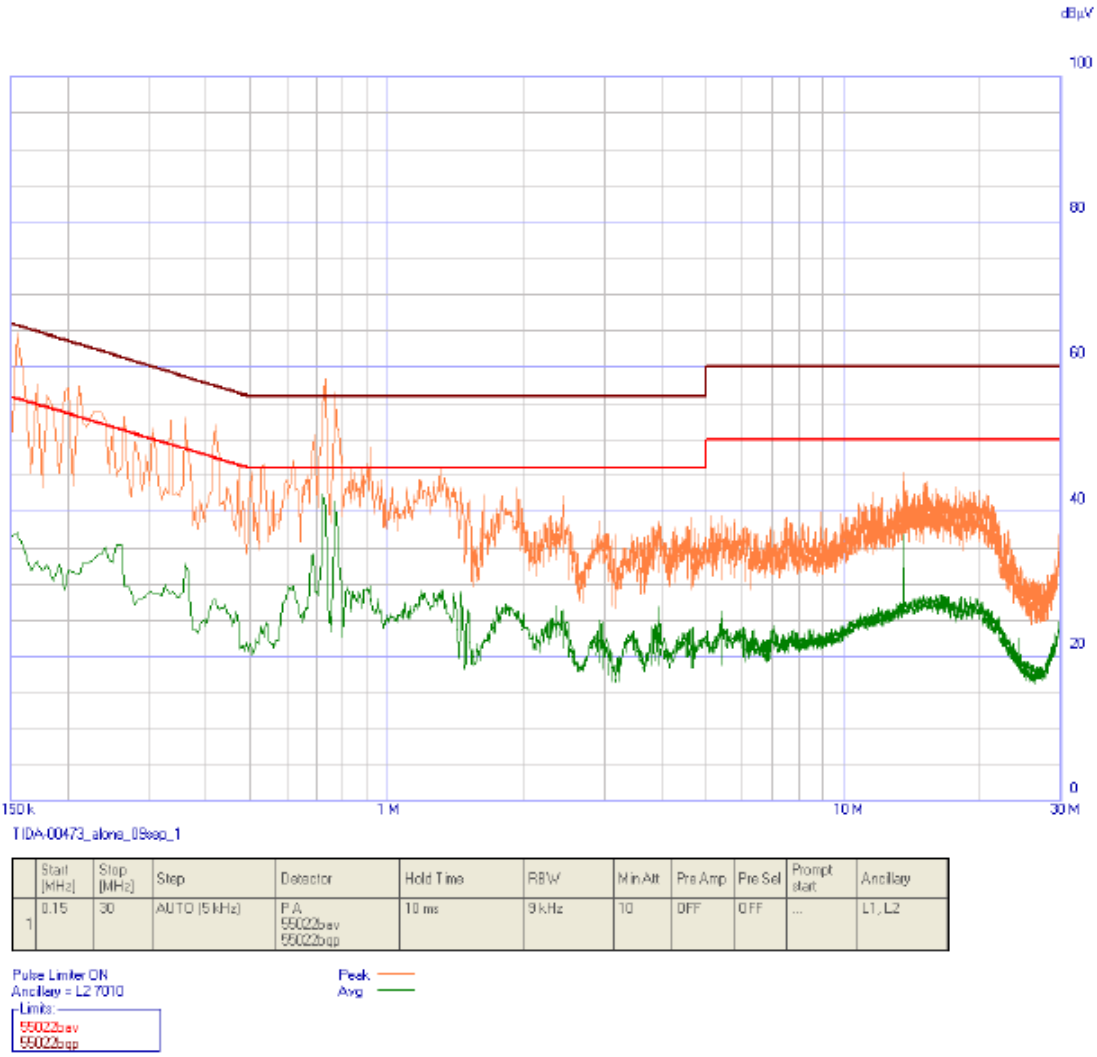


Figure 21. Conducted Emissions as per EN55022 Class B

6.5.2 Conducted Emission Test Results of TIDA-00473 and TIDA-00472 (250-W BLDC Motor Drive) Boards Connected Together

The conducted emission test is done with TIDA-00472 and TIDA-00473 boards connected together. Figure 22 shows the test results, and the board passes the EN55022 class B limits with a good margin.

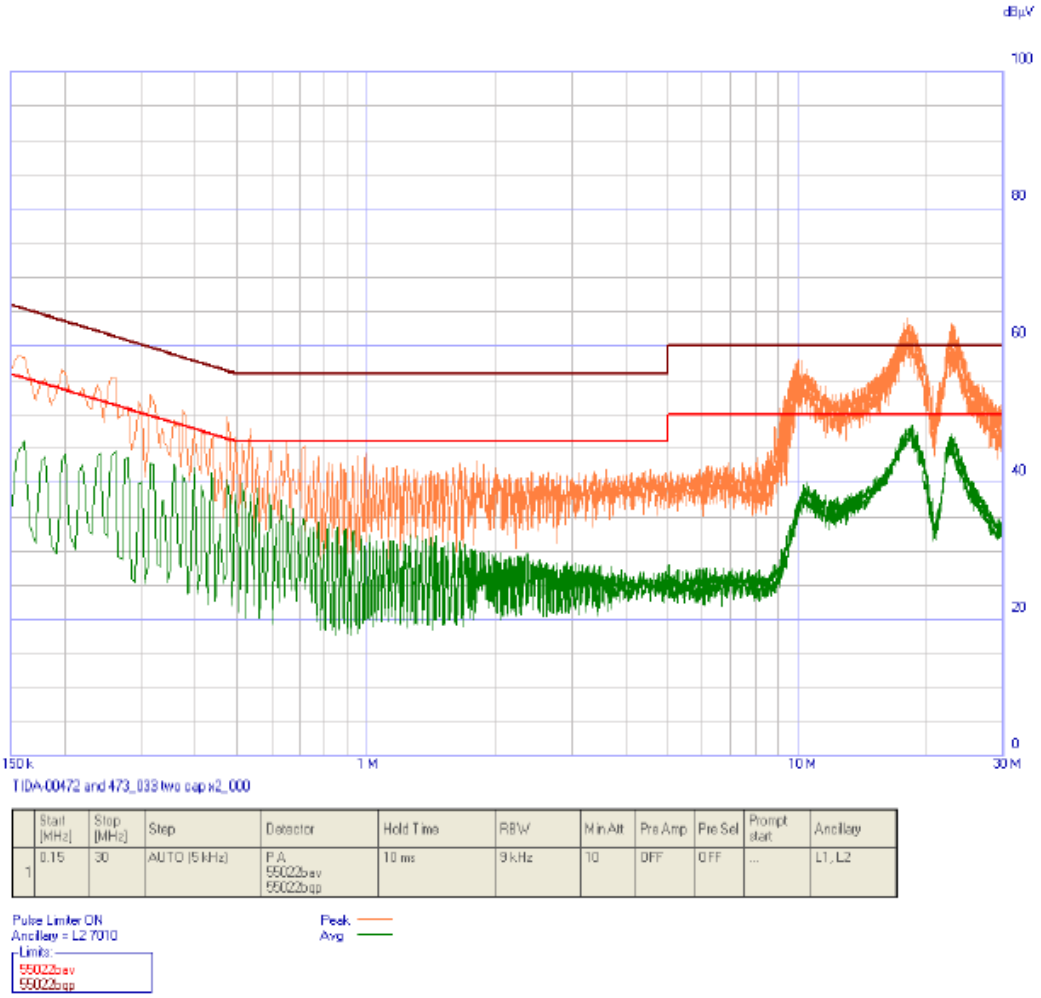


Figure 22. Conducted Emissions as per EN55022 Class B (TIDA-00473 and TIDA-00472 Connected Together)

6.6 Surge and EFT Test

Surge and EFT testing is done on the board as per EN55014. The test condition and test results are tabulated in Table 9.

Table 9. Surge and EFT Test Result

BASIC STANDARD	PORT	REQUIREMENTS FOR RESIDENTIAL, COMMERCIAL AND LIGHT-INDUSTRIAL ENVIRONMENTS	PERFORMANCE CRITERION REQUIRED	TEST RESULT
IEC/EN 61000-4-4: EFT	AC input	±1 kV, 5 kHz	B[1]	Passed with performance criterion A[2]
IEC/EN 61000-4-5: Surge	AC input	±2 kV line to earth, ±1 kV line to line	B	Passed with performance criterion A

(1) Temporary loss of function or degradation of performance, which ceases after the disturbance ceases
(2) Normal performance within limits specified by the design or manufacturer

6.7 Thermal Measurements

Thermal image of the board is captured at full load without any external cooling. The board runs for 15 minutes before capturing the thermal image.

Test setting 1: Input voltage: 90-V AC, input power: 10.4 W

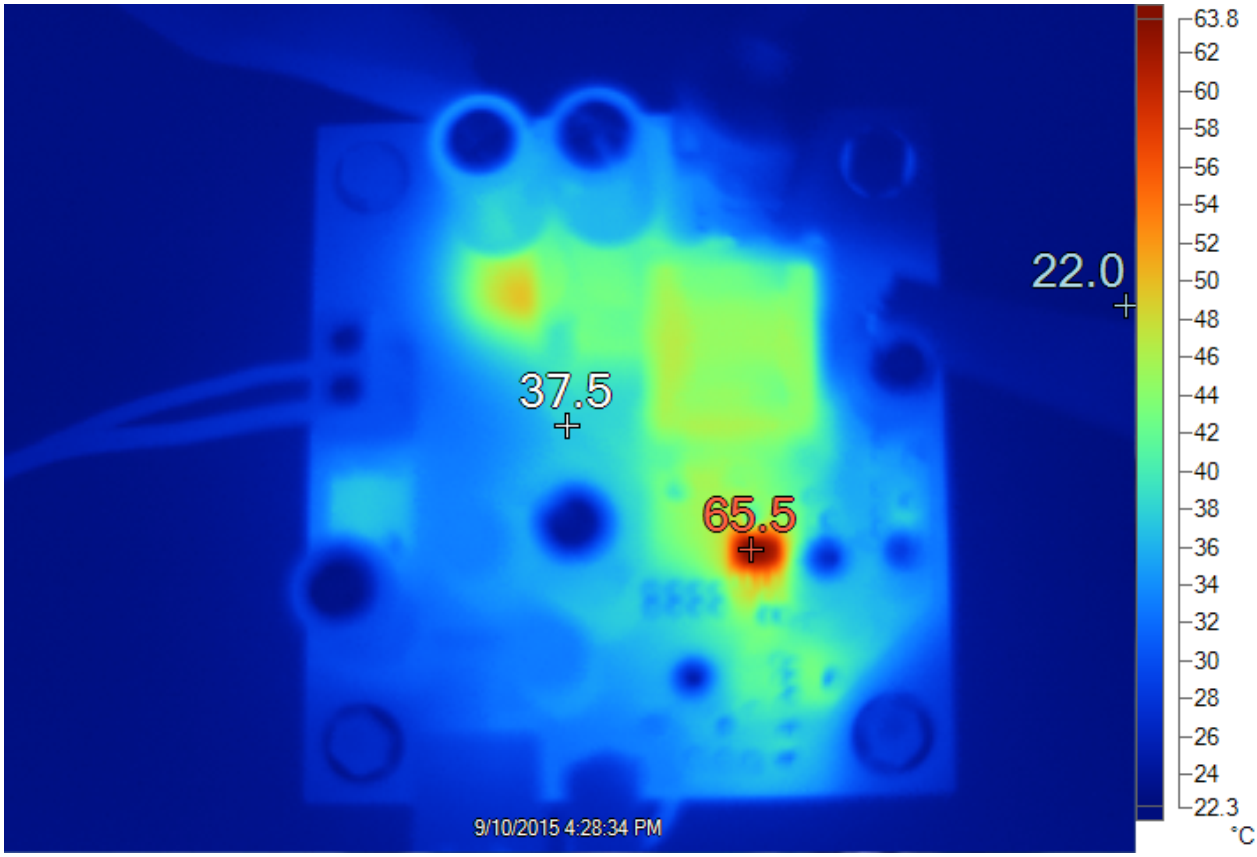


Figure 23. Top Side Temperatures at 90-V AC, 10.4-W Input Power

Table 10. Temperature at Different Points on Board at 90-V AC, 10.4 W

TEMPERATURE OBSERVED ON	TEMPERATURE
Ambient	22°C
Flyback controller (U1)	65.5°C
Transformer (T1)	43.9°C
Output diode snubber (R12)	46.1°C

Test setting 2: Input voltage: 230-V AC, input power: 10.4 W

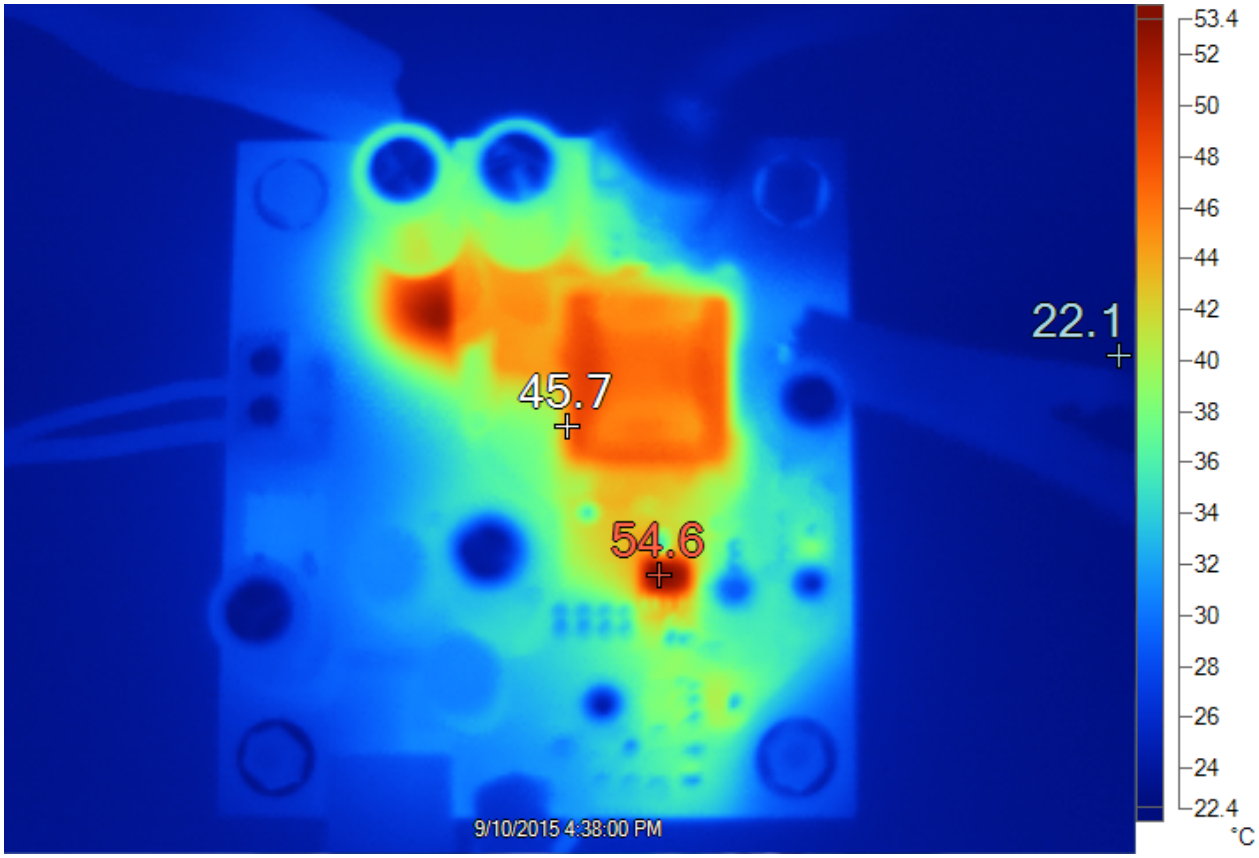


Figure 24. Top Side Temperatures at 230-V AC, 10.4-W Input Power

Table 11. Temperature at Different Points on Board at 230-V AC, 10.4 W

TEMPERATURE OBSERVED ON	TEMPERATURE
Ambient	22.1°C
Flyback controller (U1)	54.6°C
Transformer (T1)	45.7°C
Output diode snubber (R12)	52.8°C

7 Design Files

7.1 Schematics

To download the schematics, see the design files at TIDA-00473.

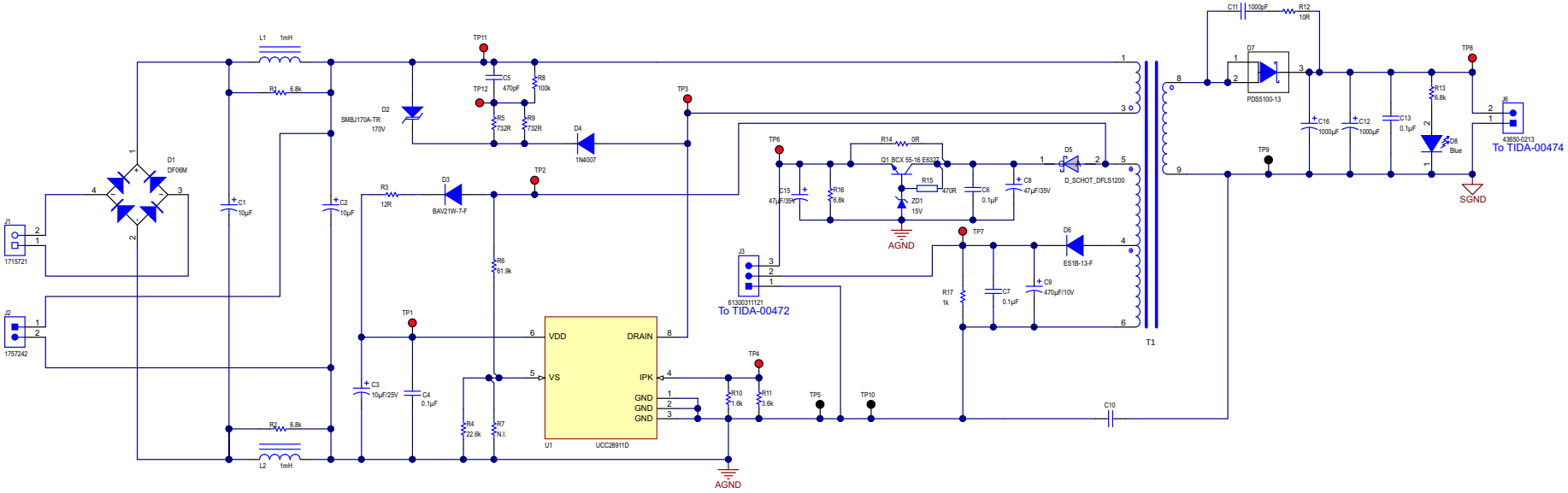


Figure 25. TIDA-00473 Schematic

7.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00473.

Table 12. BOM

QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER	MANUFACTURER PARTNUMBER	NOTE
1	PCB1	Printed Circuit Board	Any	TIDA-00473	Fitted
2	C1, C2	CAP, AL, 10 µF, 400 V, +/- 20%, ohm, TH	Nichicon	UCY2G100MPD1TD	Not Fitted
2	C12, C16	CAP, AL, 1000 µF, 25 V, +/- 20%, ohm, TH	Nichicon	UPM1E102MHD6	Fitted
1	C3	CAP, AL, 10 µF, 35 V, +/- 20%, TH	Nichicon	UVR1V100MDD1TA	Fitted
2	C8, C15	CAP, AL, 47 µF, 35 V, +/- 20%, TH	Nichicon	UVZ1V470MDD	Fitted
1	C9	CAP, AL, 470 µF, 10 V, +/- 20%, TH	Nichicon	UPW1A471MPD	Fitted
1	C4	CAP, CERM, 0.1 µF, 25 V, +/- 10%, X5R, 0603	AVX	06033D104KAT2A	Fitted
1	C5	CAP, CERM, 470 pF, 630 V, +/- 5%, C0G/NP0, 1206	TDK	C3216C0G2J471J	Fitted
3	C6, C7, C13	CAP, CERM, 0.1 µF, 50 V, +/- 5%, X7R, 0805	AVX	08055C104JAT2A	Fitted
1	C10	CAP, CERM, 1000 pF, 250 V, +/- 20%, E, Radial Disc D10.5x7mm	TDK	CS11-E2GA102MYNS	Fitted
1	C11	CAP, CERM, 1000 pF, 500 V, +/- 10%, X7R, 1206_190	Kemet	C1206C102KCRACTU	Fitted
1	D1	Diode, Switching-Bridge, 600 V, 1 A, TH	Diodes Inc.	DF06M	Not Fitted
1	D2	Diode, TVS, Uni, 170 V, 600 W, SMB	STMicroelectronics	SMBJ170A-TR	Not Fitted
1	D3	Diode, Switching, 200 V, 0.2 A, SOD-123	Diodes Inc.	BAV21W-7-F	Fitted
1	D4	Diode, Rectifier, 1000 V, 1 A, SMA	ON Semiconductor	MRA4007T3G	Fitted
1	D5	Diode, Schottky, 1A, 200V	Diodes	DFLS1200	Fitted
1	D6	Diode, Superfast Rectifier, 100 V, 1 A, SMA	Diodes Inc.	ES1B-13-F	Fitted
1	D7	Diode, Schottky, 100 V, 5 A, PowerDI5	Diodes Inc.	PDS5100-13	Fitted
1	D8	LED, Blue, SMD	Wurth Elektronik	150060BS75000	Optional
4	H1, H4, H7, H10	Bumpon, Hemisphere, 0.44 X 0.20, Clear	3M	SJ-5303 (CLEAR)	Fitted
4	H3, H6, H9, H12	Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	B&F Fastener Supply	NY PMS 440 0025 PH	Fitted
1	J1	Conn Term Block, 2POS, 5.08mm, TH	Phoenix Contact	1715721	Not Fitted
1	J2	Header (Shrouded), 5.08 mm, 2x1, Tin, R/A, TH	Phoenix Contact	1757242	Fitted
1	J6	43650-0213	Molex	43650-0213	Fitted
1	J3	Header, 2.54 mm, 3x1, Gold, TH	Wurth Elektronik	61300311121	Fitted

Table 12. BOM (continued)

QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER	MANUFACTURER PARTNUMBER	NOTE
2	L1, L2	Inductor, Shielded Drum Core, Metal Composite, 1 mH, 0.5 A, 1.7 ohm, TH	Wurth Elektronik	768772102	Not Fitted
1	Q1	BCX 55-16 E6327	Infineon Technologies	BCX 55-16 E6327	Fitted
1	R15	RES, 470, 1%, 0.1 W, 0603	Vishay-Dale	CRCW1206470RJNEA	Fitted
1	T1	750342999	Wurth Elektronik	750342999	Fitted
1	ZD1	BZV55C15	Microsemi	BZV55C15	Fitted
2	R1, R2,	RES, 6.8 k, 5%, 0.25 W, 1206	Vishay-Dale	CRCW12066K80JNEA	Not Fitted
2	R13, R16	RES, 6.8 k, 5%, 0.25 W, 1206	Vishay-Dale	CRCW12066K80JNEA	Optional
1	R14	RES, 0, 5%, 0.25 W, 1206	Vishay-Dale	CRCW12060000JNEA	Not Fitted
1	R17	RES, 1 k, 5%, 0.25 W, 1206	Vishay-Dale	CRCW12061K00JNEA	Optional
1	R6	RES, 76.8 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060376K8FKEA	Fitted
1	R3	RES, 12, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060312FKEA	Fitted
1	R4	RES, 27 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060327K00FKEA	Fitted
1	R7	RES, 510 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW0603510K00FKEA	Fitted
1	R10	RES, 1.6 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW06031K60FKEA	Fitted
1	R11	RES, 3.6 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW06033K60FKEA	Fitted
2	R5, R9	RES, 732, 5%, 0.25 W, 1206	Vishay-Dale	CRCW1206732RJNEA	Fitted
1	R8	RES, 100 k, 1%, 0.25 W, 1206	Vishay-Dale	CRCW1206100KFKEA	Fitted
1	R12	RES, 10, 5%, 0.25 W, 1206	Vishay-Dale	CRCW120610R0JNEA	Fitted
9	TP1, TP2, TP3, TP4, TP6, TP7, TP8, TP11, TP12	Test Point, Miniature, Red, TH	Keystone	5000	Fitted
3	TP5, TP9, TP10	Test Point, Miniature, Black, TH	Keystone	5001	Fitted
1	U1	High Voltage Flyback Switcher with Primary-side Regulation and Constant-Current Control, D0007A	Texas Instruments	UCC28911D	Fitted

7.3 Layout Guidelines

A careful PCB layout is critical and extremely important in a fast-switching circuit to provide appropriate device operation and design robustness. As with all switching power supplies, attention to detail in the layout can save much time in troubleshooting later on.

7.3.1 Power Stage Specific Guidelines

The following are key guidelines for routing power stage components:

- Minimize the loop area and trace length of the power path circuits, which contain high frequency switching currents. This will help in reducing EMI and improve converter overall performance.
- Keep the switch node as short as possible. A short and optimal trace width helps to reduce induced ringing caused by parasitic inductance.
- Keep traces with high dV/dt potential and high di/dt capability away from or shielded from sensitive signal traces, with adequate clearance and ground shielding.
- For each power supply stage, keep power ground and control ground separately. Tie them together (if they are electrically connected) in one point near DC input return or output return of the given stage correspondingly.
- When multiple capacitors are used in parallel for current sharing, keep the layout symmetrical across both leads of the capacitors. If the layout is not identical, the capacitor with the lower series trace impedance will see higher peak currents and become hotter (i2R).
- Place protection devices such as TVS, snubbers, capacitors, or diodes physically close to the device they are intended to protect, and route with short traces to reduce inductance.
- Choose the width of PCB traces based on acceptable temperature rise at the rated current as per IPC2152 as well as acceptable DC and AC impedances. Also, the traces should withstand the fault currents (such as short circuit current) before the activation of electronic protection such as fuse or circuit breaker.
- Determine the distances between various traces of the circuit according to the requirements of applicable standards. For this design, UL 60950-1 safety standard is followed to maintain the creepage and clearance from live line to neutral line and to safety ground.
- Adapt thermal management to fit the end-equipment requirements.

7.3.2 Controller Specific Guidelines

The following are key guidelines for routing of controller components and signal circuits:

- The optimum placement of decoupling capacitor is closest to the VCC and GND terminals of the device. Take care when minimizing the loop area formed by the bypass capacitor connection and the GND terminal of the IC.
- The reference ground for the control devices, a low current signal ground (SGND), should be a copper plane or island.
- Locate all controller support components at specific signal pins (VS and IPK) close to their connection pin. Connect the other end of the component to the SGND with shortest trace length.
- The trace routing for the voltage sensing and current sensing circuit components to the device should be as short as possible to reduce parasitic effects on the current limit and current/voltage monitoring accuracy. These traces should not have any coupling to switching signals on the board.
- Connect the SGND plane to high current ground (main power ground) at a single point that is at the negative terminal of DC IO capacitor respectively.

7.3.3 Layout Plots

To download the layer plots, see the design files at TIDA-00473.

7.4 Altium Project

To download the Altium project files, see the design files at TIDA-00473.

7.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00473.

7.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00473.

7.7 Design Calculator Spreadsheet

To download the design spreadsheet calculator for this reference design, see the link at TIDA-00473.

8 References

1. Texas Instruments, *UCC28910, UCC28911 High-Voltage Flyback Switcher with Primary-Side Regulation and Output Current Control*, UCC28911 Datasheet (SLUS769)
2. Texas Instruments, *Using the UCC28911EVM-718 7.5W Universal Off-Line Flyback Converter with Primary-Side Regulation*, UCC28911 User's Guide (SLUUBA1)

9 Terminology

TI Glossary: This glossary lists and explains terms, acronyms, and definitions (SLYZ022).

Specific terms used in the document:

PWM— Pulse width modulation

FETs, MOSFETs—Metal oxide semiconductor field-effect transistor

ESD— Electrostatic discharge

RMS— Root mean square

BLDC— Brushless DC motor

Capacitance terms in Farads:

C_{BULK}— Total input capacitance

C_{VDD}— Capacitance on the VDD terminal

C_{OUT}— Output capacitance

Duty cycle terms:

D_{MAX}— MOSFET on-time maximum duty cycle

Frequency terms in Hertz:

f_{LINE}— Minimum line frequency

$f_{TARGET(MAX)}$— Target full-load maximum switching frequency of the converter

f_{MIN}— Minimum switching frequency of the converter, add 15% margin over the fSW(min) limit of the device

$f_{SW(MIN)}$— Minimum switching frequency

Current terms in Amperes:

I_{OCC}— Converter output current target when operating in constant current mode

$I_{D\_PK(MAX)}$— Maximum transformer primary current peak

I_{TRAN}— Required positive load-step current

I_{RUN}— Maximum current consumption of the device

I_{VSLRUN}— VS terminal run current

Current and voltage scaling terms:

K_{AM}— Maximum-to-minimum peak-primary current ratio

Transformer terms:

L_P— Transformer primary inductance

N_{PA}— Transformer primary-to-auxiliary turns ratio

N_{PS}— Transformer primary-to-secondary turns ratio

Power terms in Watts:

P_{IN}— Converter maximum input power

P_{OUT}— Full-load output power of the converter

Resistance terms in Ohms:

R_{IPK}— primary current programming resistance

R_{PRL}— Preload resistance on the output of the converter

Timing terms in seconds:

$t_{DMAG(MIN)}$— Minimum secondary rectifier conduction time

$t_{ON(MIN)}$— Minimum MOSFET on time

Voltage terms in Volts:

V_{BULK}— Highest bulk capacitor voltage for stand-by power measurement

V_{DSPK}— Peak MOSFET drain-to-source voltage at high line

V_F— Secondary rectifier, DOUT, forward voltage drop at near-zero current

V_{VDD}— Voltage value on VDD terminal

V_{OCC}— Target lowest converter output voltage in constant-current regulation

ΔV_{UVLO}— $VDD_{ON} - VDD_{OFF}$

AC voltage terms in V_{RMS}:

$V_{IN(MAX)}$— Maximum AC input voltage to the converter

$V_{IN(MIN)}$— Minimum AC input voltage to the converter

Efficiency terms:

η— Converter overall efficiency

10 About the Author

YUAN "JASON" TAO is a Systems Engineer at Texas Instruments, where he is responsible for developing reference design solutions for the industrial segment. Yuan brings to this role his extensive experience in power electronics, high frequency DC-DC converter, and analog circuit design. Yuan earned his Master of IC Design and Manufacture degree from Shanghai Jiao Tong University in 2007.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (November 2015) to B Revision	Page
• Changed title	1

IMPORTANT NOTICE FOR TI REFERENCE DESIGNS

Texas Instruments Incorporated ('TI") reference designs are solely intended to assist designers ("Designer(s)") who are developing systems that incorporate TI products. TI has not conducted any testing other than that specifically described in the published documentation for a particular reference design.

TI's provision of reference designs and any other technical, applications or design advice, quality characterization, reliability data or other information or services does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such reference designs or other items.

TI reserves the right to make corrections, enhancements, improvements and other changes to its reference designs and other items.

Designer understands and agrees that Designer remains responsible for using its independent analysis, evaluation and judgment in designing Designer's systems and products, and has full and exclusive responsibility to assure the safety of its products and compliance of its products (and of all TI products used in or for such Designer's products) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to its applications, it has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any systems that include TI products, Designer will thoroughly test such systems and the functionality of such TI products as used in such systems. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

Designers are authorized to use, copy and modify any individual TI reference design only in connection with the development of end products that include the TI product(s) identified in that reference design. HOWEVER, NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of the reference design or other items described above may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI REFERENCE DESIGNS AND OTHER ITEMS DESCRIBED ABOVE ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING THE REFERENCE DESIGNS OR USE OF THE REFERENCE DESIGNS, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNERS AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS AS DESCRIBED IN A TI REFERENCE DESIGN OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THE REFERENCE DESIGNS OR USE OF THE REFERENCE DESIGNS, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

TI's standard terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products. Additional terms may apply to the use or sale of other types of TI products and services.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265