PMP40281 Test Results

1 General

1.1 Purpose

This test report is to provide the detailed data for evaluating and verifying the PMP40281 which employs TI's new LLC Controller ---- UCC25630X. PMP40281 is only a control card for the essential functions for a LLC converter. It must be connected to a LLC power stage for the full system evaluation.

1.2 Reference Documentation

Schematic: PMP40281_Sch.pdf

Gerber: PMP40281_GerberNCdrills.zip

Layer Plot: PMP40281_PCBlayers.pdf

Assembly Drawing: PMP40281_Assy.pdf

CAD File: PMP40281_CAD.zip

BOM: PMP40281_BOM.pdf

1.3 Test Equipment

Multi-meter (voltage): Fluke 287C

AC Source: Chroma 61503

DC Source: Chroma 62012P-600-8

E-Load: Chroma 63105A module

Oscilloscope: Tektronix DPO3054

Power Board: UCC25630-1EVM-291

2 Pin Definitions

Pin functions

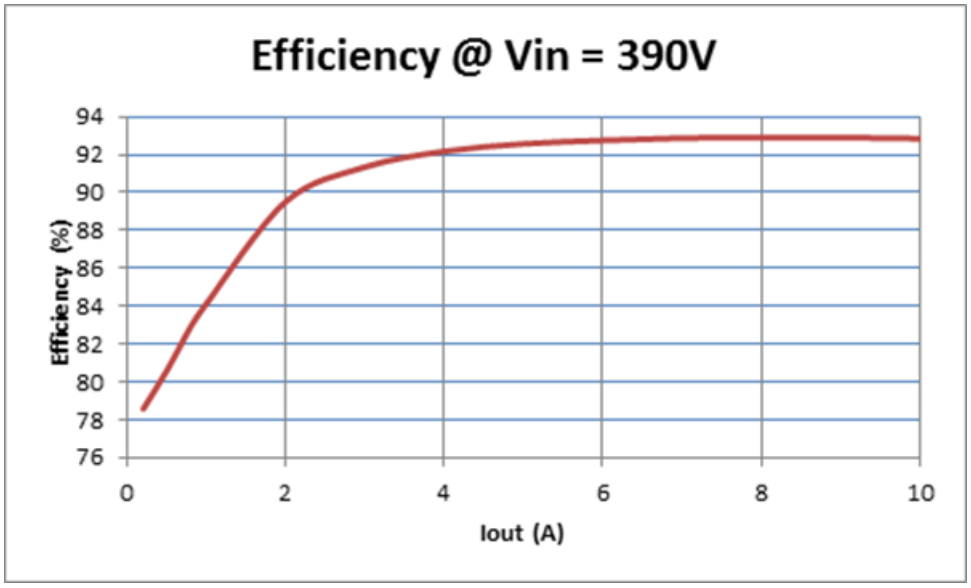
PIN		I/O	Description
NUMBER	NAME		
1	ACL	I	AC Line input. Combined with ACN, they are used to detect the AC voltage and perform X cap discharging. **Connect this pin to AC Line terminal directly**
2	ACN	I	AC Neutral input. Combined with ACL, they are used to detect the AC voltage and perform X cap discharging. **Connect this pin to AC Neutral terminal directly**
3	VBLK	I	Input voltage Sensing. **Connect this pin to the input bulk capacitor of LLC converter**
4	VCR	I	**Tie to resonant capacitor node**, it senses the resonant capacitor voltage and resonant current
5	HS	I	**Connect to intermediate node of LLC half bridge**, return path of HO. High voltage switching node
6	HO	O	Output of HIGH side driver. **Tie to Gate of HIGH side FET**. A gate resistor could be inserted between this pin and gate of HIGH side FET to control the switching speed
7	NC		No connection
8,12	GND	I	Ground reference for all signals. **Connect to source of low side FET**
9	LO	O	Output of LOW side driver. **Tie to Gate of LOW side FET**. A gate resistor could be inserted between this pin and gate of LOW side FET to control the switching speed
10	RVCC	O	**To VCC of PFC controller**. It is used to supply a 12V DC voltage to PFC controller. If PFC controller doesn't need it, left it as floating
11	BSW	I	Sense the bias winding voltage for output OVP. **Connect to the bias winding before rectifier diode**. Switching node
13	FB	I	**Connect to opto-coupler output for output feedback**. The current is injected into part directly
14	VCC	I	Bias power from bias winding. Connect this pin to the bulk filtering capacitor

			of bias rail after the rectifier diode. If the capacitance of this bulk cap on power board is small, install C13 on PMP40281

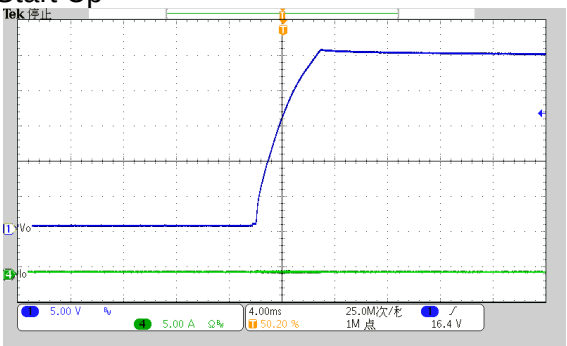
3 Performance Data and Waveform

Note: PMP40281 is only a daughter card for the control portion. The system performance is mainly related to the connected power board and the compensation network which is on the power board as well. The results below are only the example when PMP40281 is connected to UCC25630-1EVM-291.

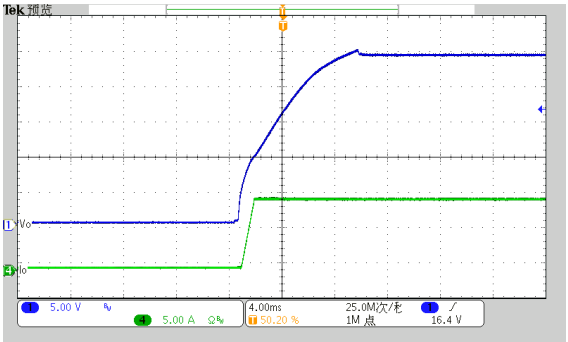
3.1 Efficiency



3.2 Start Up

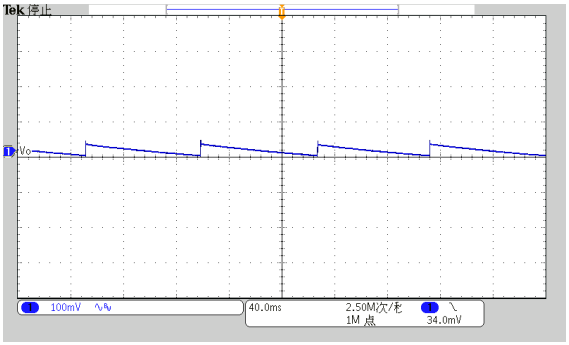


Vin=390V and No Load
CH1: Vo 5V/Div
CH4: Io 5A/Div

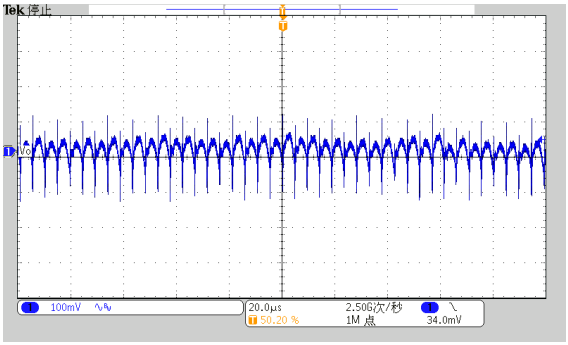


Vin=390V and Full Load
CH1: Vo 5V/Div
CH4: Io 5A/Div

3.3 Output Voltage Ripple



Vin=390V and No Load
CH1: Vo (AC Coupled) 100mV/Div



Vin=390V and Full Load
CH1: Vo (AC Coupled) 100mV/Div

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