ADC081000

Ultra-High Speed ADCs Revolutionize Digital Receiver Design

Technology Edge

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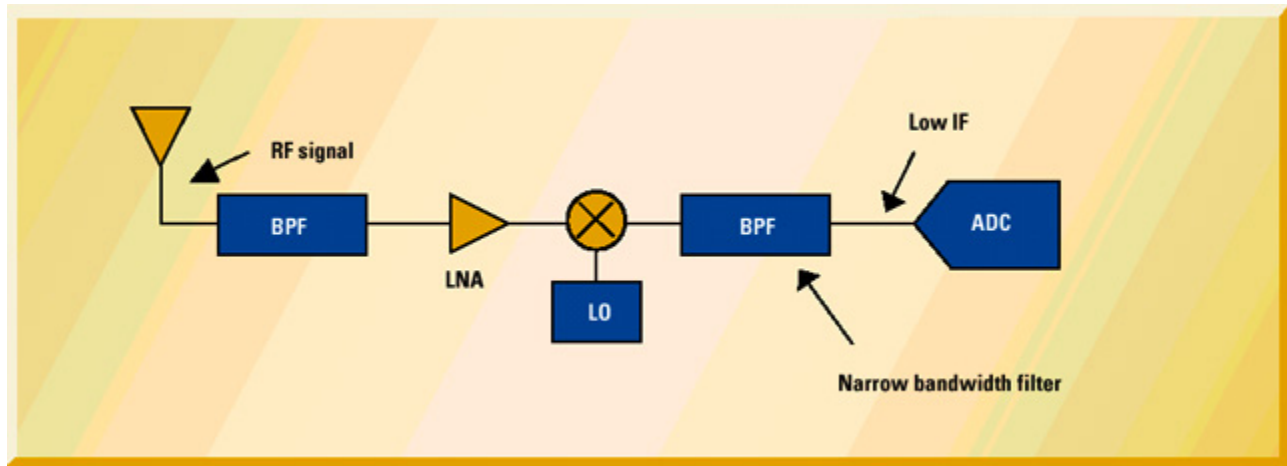*By Paul McCormack, Applications Engineer*

Figure 1: Conventional receiver (front end)

This article demonstrates how ultra high-speed, high-analog input bandwidth ADCs can be used in digital receivers to replace RF tuners and also to offer functionality not possible with current receivers. The conventional receiver architecture requires an RF tuner for channel selectivity in the analog domain prior to digitization and digital signal processing. The limiting factors of such an architecture are the analog input bandwidth and sampling frequency of the ADC. Until now, it has not been possible to obtain cost-effective ADCs with 1 GHz + analog input bandwidth and 1 GSPS + sampling frequency. Replacing RF tuners with a high-performance ADC such as the ADC081000 allows simultaneous digitization of the entire RF input signal. This also results in a reduction in power consumption, cost and area associated with receivers containing multiple bulky RF tuners.

The ADC081000 is an 8-bit 1 GSPS, 1.6 GHz, analog input bandwidth ADC. Manufactured on a 0.18 µm CMOS process, it is the first of its kind on the market. The majority of ultra high-speed ADCs to date are manufactured with BiCMOS processes. Compared with CMOS transistors, bipolar devices have lower offset voltages and higher gain, making them the traditional choice - particularly at high frequencies - for designing analog front ends. However, due to higher current requirements, the resultant power consumption of a bipolar device is much higher than its CMOS equivalent. In real terms, the ADC081000 consumes approximately 1.4W. The lowest power BiCMOS equivalent ADC on the market represents a thermal nightmare in terms of heat dissipation and heat sink requirements, as it consumes over 3W. Not compromising dynamic performance, the ADC081000 meets the dynamic range specifications required of communications systems and high performance test instrumentation and delivers over 7.5 ENOB well past Nyquist.

Conventional Receivers

The RF signal received at the antenna is first down converted for digitization. Figure 1 shows a simple RF down conversion stage that converts the input RF frequency directly to the first IF. Normally the IF is undersampled, i.e. sampled at less than the Nyquist rate. It is worth mentioning that the process of harmonic folding that occurs in undersampling applications results in every sampled image 'folding' back into the frequency spectrum below FS/2 (FS = ADC sampling frequency). For example, the process of undersampling mixes the 36 MHz input at the ADC output down to 4 MHz at its output (2 FS - FIN = 4 MHz).

The ADC analog input bandwidth is usually quite small (10 – 400 MHz) so for a wide bandwidth system, channel selectivity has to be performed prior to digitization as shown in Figure 1.
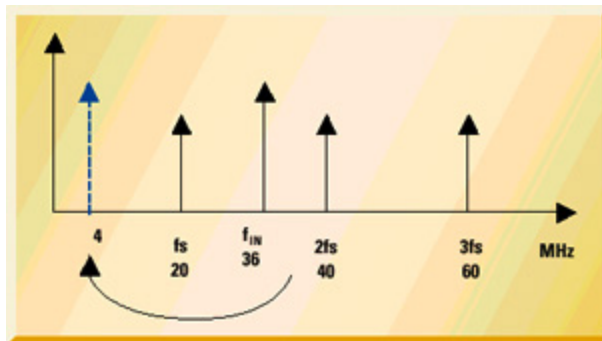
Figure 2: Undersampling in the ADC mixes fIN to < FS/2.

System Limitation
The ADC is the limiting block in signal chain. Due to its low analog input bandwidth, channels must be filtered in the analog domain before ADC digitization.
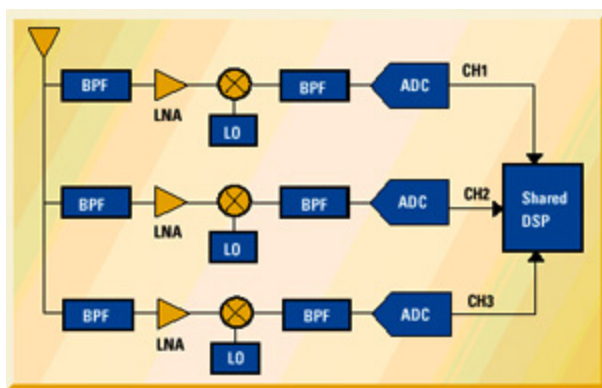

Figure 3: Multiple tuner approach

Using a multiple tuner approach, three channels can be simultaneously digitized. This is a costly solution due to the number of down-conversion stages required, and the system is still limited by the sampling frequency and analog input bandwidth of the ADCs.

In Figure 4, the ADC081000 has sufficient analog input bandwidth to digitize the entire input signal range. Channel selectivity can now be performed in the digital domain. This eliminates the need for multiple tuners prior to the ADC as shown in Figure 3.
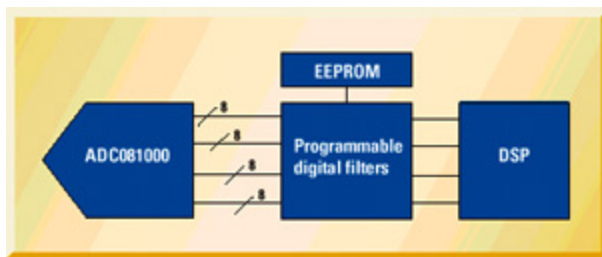

Figure 4

Figure 5 demonstrates how sampling at a much higher frequency such as 1 GSPS makes it possible to filter the digital data and retrieve the information modulated onto any of the carriers in a multi carrier system. Note that the carrier frequencies above FS/2 mix down to below FS/2, e.g. a carrier at 850 MHz mixes down to 150 MHz. The sampling frequency can be offset from 1 GSPS to accurately control the harmonic folding and thereby aid the subsequent digital filtering process.

The digital filters perform channel selectivity. All of the digitized channels are available at the ADC outputs and the filter coefficients for X number of channels are stored in the EEPROM.
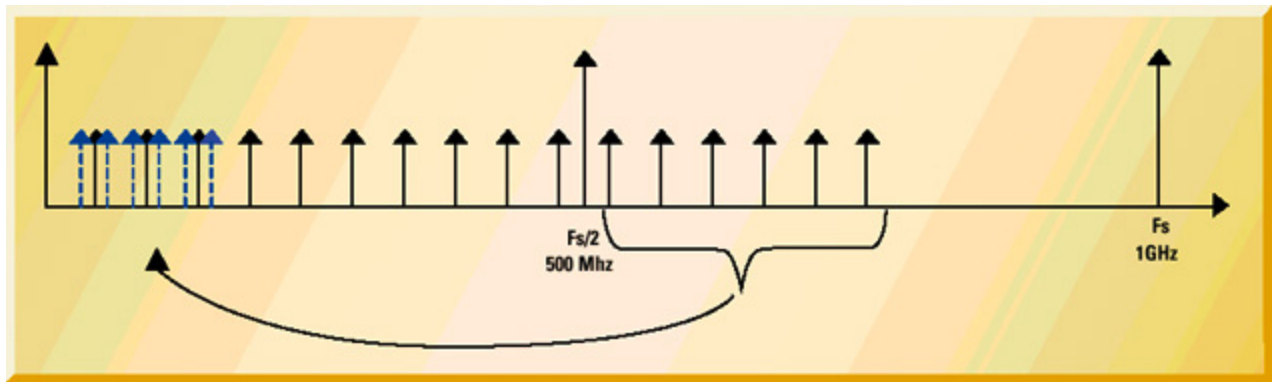
Figure 5: Sampling at 1 GSPS benefits channel selectivity

ADC081000 benefits in digital receiver applications	
Analog input bandwidth	1.6 GHz
Sampling frequency	1 GSPS
Low voltage and low power	1.4W at 1.9V
Small size (considerable saving over multiple tuner approach)	LQFP-128

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