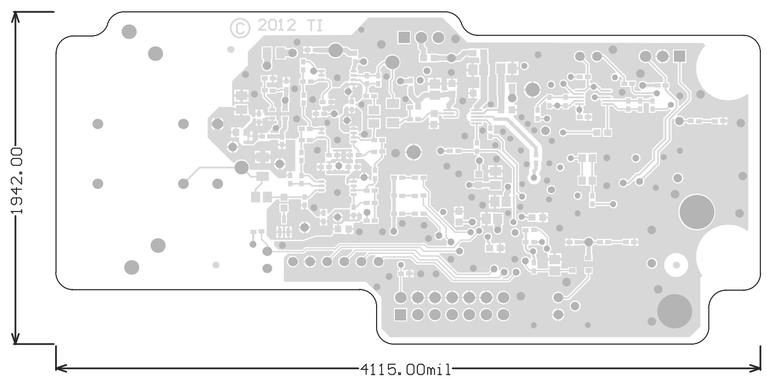

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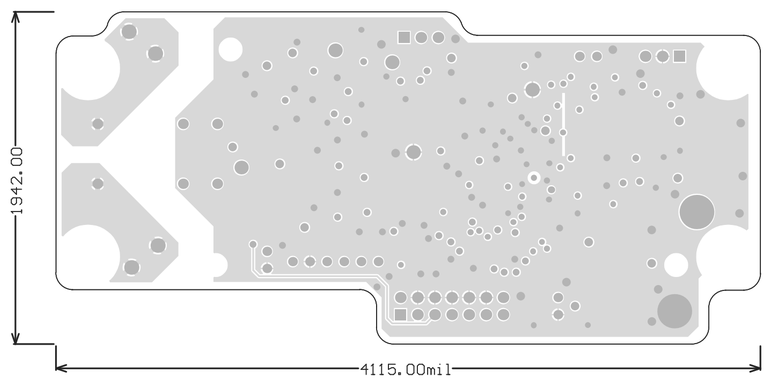
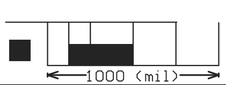
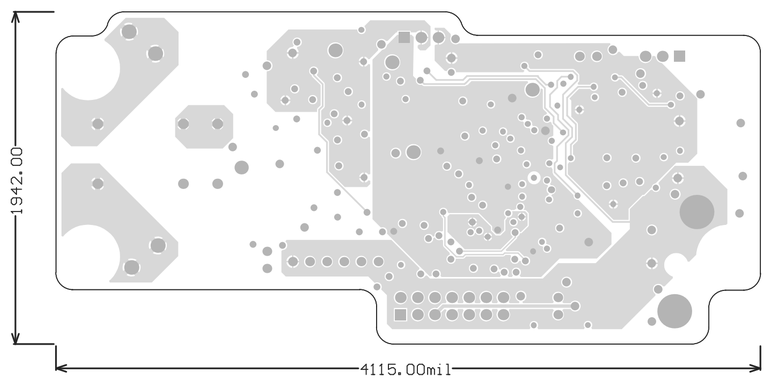
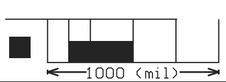
ALL ARTWORK VIEWED FROM TOP SIDE	PROJECT NAME = SM73201 - ARC EVAL	
LAYER NAME = M2 Board Dimensions	ARTWORK # = 880600728 002REV A	
PLOT NAME = Top Layer	GENERATED : 6/18/2012 2:53:29 PM	NATIONAL SEMICONDUCTOR



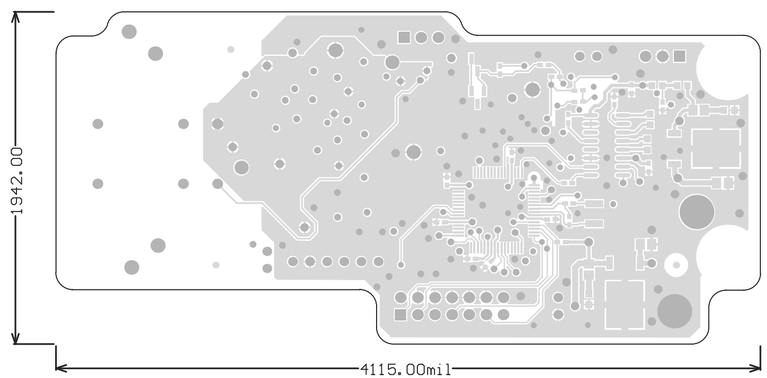


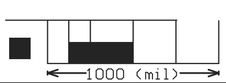
ALL ARTWORK VIEWED FROM TOP SIDE	PROJECT NAME = SM73201 - ARC EVAL	
LAYER NAME = M2 Board Outline	ARTWORK # = 880600728 002REV A	
PLOT NAME = Mid-Layer 1	GENERATED : 6/18/2012 2:53:31 PM	NATIONAL SEMICONDUCTOR



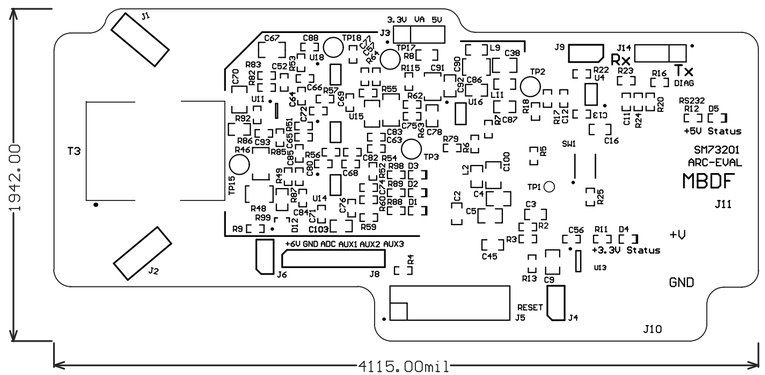


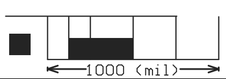
ALL ARTWORK VIEWED FROM TOP SIDE	PROJECT NAME = SM73201 - ARC EVAL	
LAYER NAME = M2 Board Dimensions	ARTWORK # = 880600728 002REV A	
PLOT NAME = Mid-Layer 2	GENERATED : 6/18/2012 2:53:32 PM	NATIONAL SEMICONDUCTOR



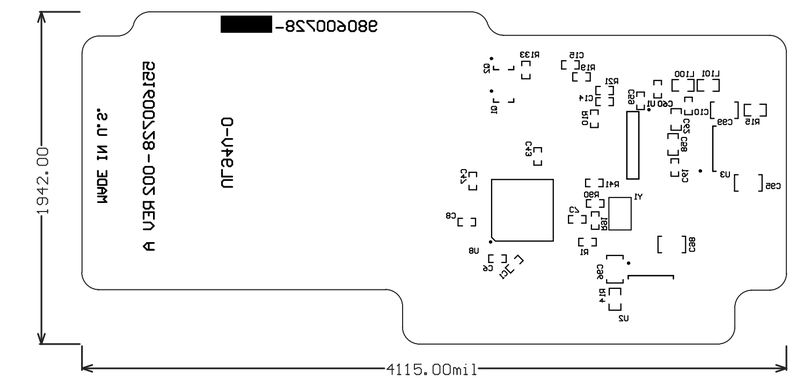


ALL ARTWORK VIEWED FROM TOP SIDE	PROJECT NAME = SM73201 - ARC EVAL	
LAYER NAME = M2 Board Dimensions	ARTWORK # = 880600728 002REV A	
PLOT NAME = Bottom Layer	GENERATED : 6/18/2012 2:53:33 PM	NATIONAL SEMICONDUCTOR





ALL ARTWORK VIEWED FROM TOP SIDE	PROJECT NAME = SM73201 - ARC EVAL	
LAYER NAME = MapBoardDimensions	ARTWORK # = 880600728 002REV A	
PLOT NAME = Top Silkscreen Overlay	GENERATED : 6/18/2012 2:53:34 PM	NATIONAL SEMICONDUCTOR



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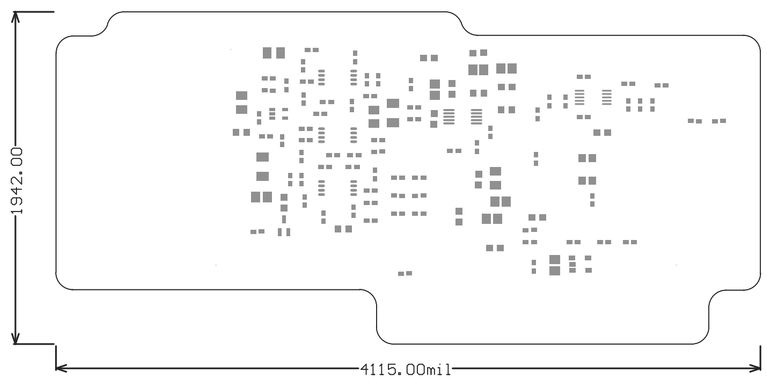
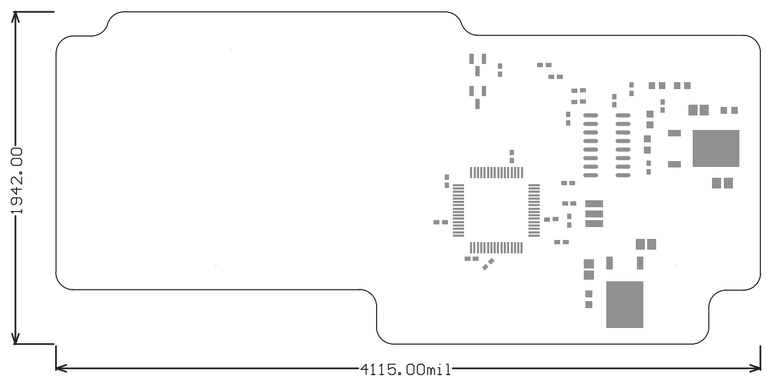
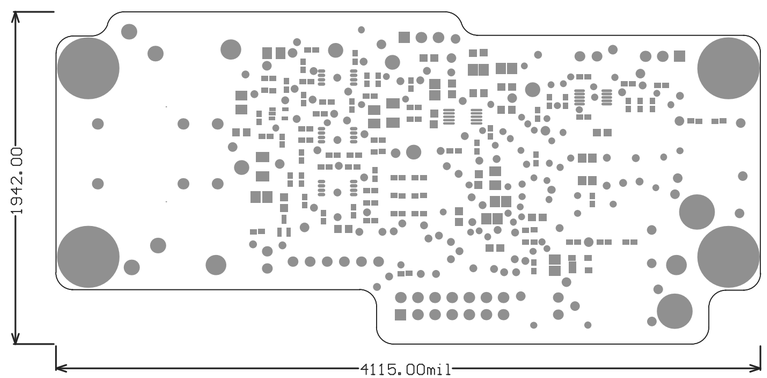
ALL ARTWORK VIEWED FROM TOP SIDE	PROJECT NAME = SM73201 - ARC EVAL	
LAYER NAME = Bottom Silkscreen Overlay	ARTWORK # = 880600728 002REV A	
PLOT NAME = Bottom Silkscreen Overlay	GENERATED : 6/18/2012 2:53:36 PM	NATIONAL SEMICONDUCTOR



ALL ARTWORK VIEWED FROM TOP SIDE	PROJECT NAME = SM73201 - ARC EVAL	
LAYER NAME = M2 Board Dimensions	ARTWORK # = 880600728 002REV A	
PLOT NAME = Top Paste Mask Print	GENERATED : 6/18/2012 2:53:37 PM	NATIONAL SEMICONDUCTOR

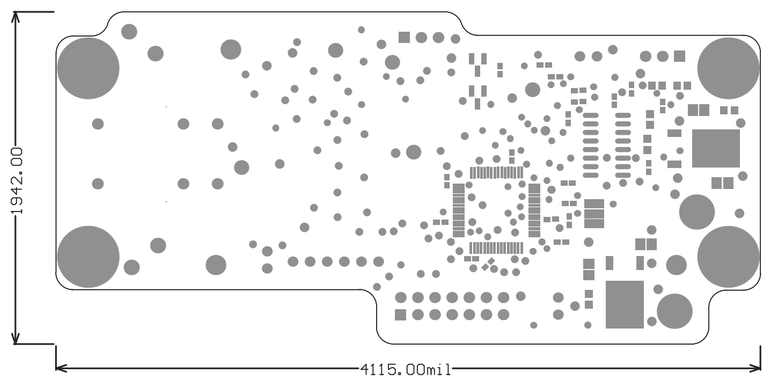


ALL ARTWORK VIEWED FROM TOP SIDE	PROJECT NAME = SM73201 - ARC EVAL	
LAYER NAME = M2 Board Dimensions	ARTWORK # = 880600728 002REV A	
PLOT NAME = Bottom Paste Mask Print	GENERATED : 6/18/2012 2:53:38 PM	NATIONAL SEMICONDUCTOR



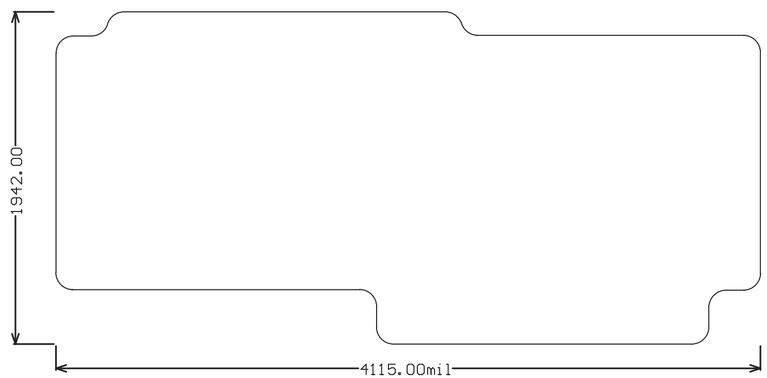
1000 (mil)

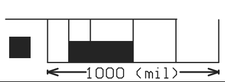
ALL ARTWORK VIEWED FROM TOP SIDE	PROJECT NAME = SM73201 - ARC EVAL	
LAYER NAME = M2 Board Dimensions	ARTWORK # = 880600728 002REV A	
PLOT NAME = Top Solder Mask Print	GENERATED : 6/18/2012 2:53:38 PM	NATIONAL SEMICONDUCTOR



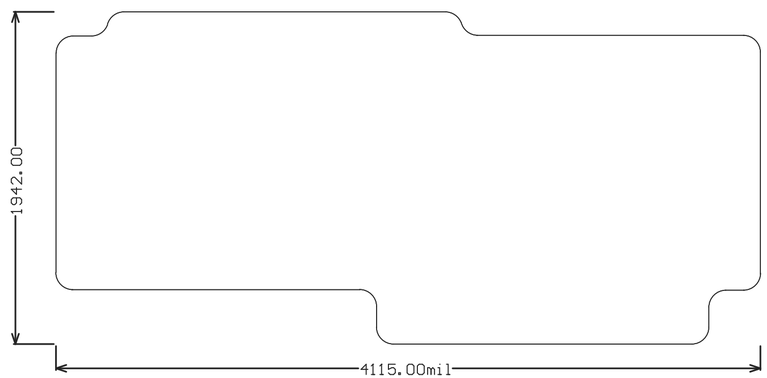
1000 (mil)

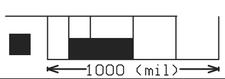
ALL ARTWORK VIEWED FROM TOP SIDE	PROJECT NAME = SM73201 - ARC EVAL	
LAYER NAME = M2 Board Dimensions	ARTWORK # = 880600728 002REV A	
PLOT NAME = Bottom Solder Mask Print	GENERATED : 6/18/2012 2:53:39 PM	NATIONAL SEMICONDUCTOR



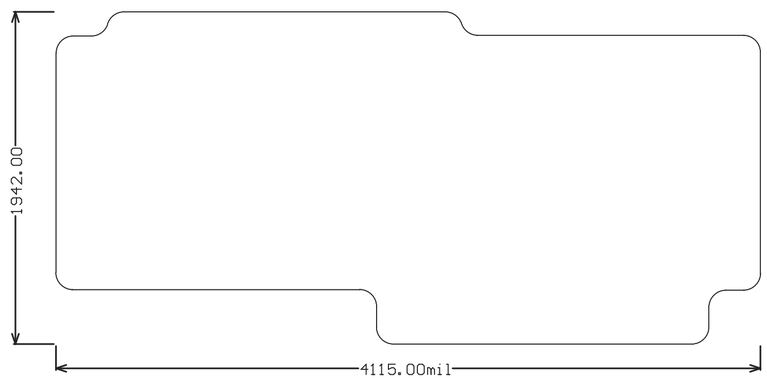


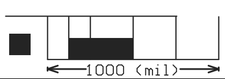
ALL ARTWORK VIEWED FROM TOP SIDE	PROJECT NAME = SM73201 - ARC EVAL	
LAYER NAME = M2 Board Outline	ARTWORK # = 880600728 002REV A	
PLOT NAME = M1 Board Outline	GENERATED : 6/18/2012 2:53:40 PM	NATIONAL SEMICONDUCTOR



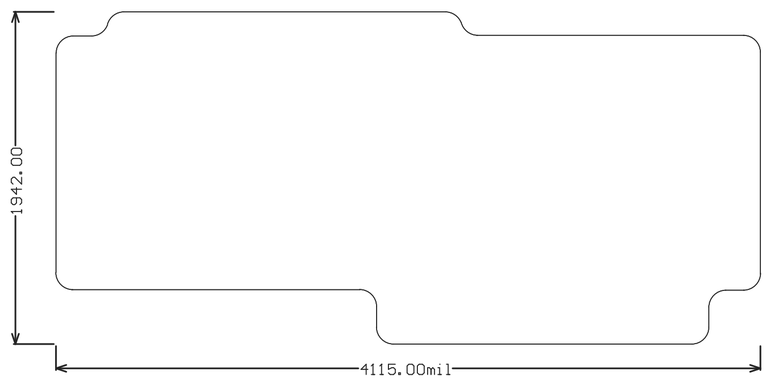


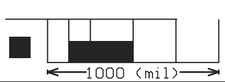
ALL ARTWORK VIEWED FROM TOP SIDE	PROJECT NAME = SM73201 - ARC EVAL	
LAYER NAME = M2 Board Dimensions	ARTWORK # = 880600728 002REV A	
PLOT NAME = M2 Board Dimensions	GENERATED : 6/18/2012 2:53:41 PM	NATIONAL SEMICONDUCTOR



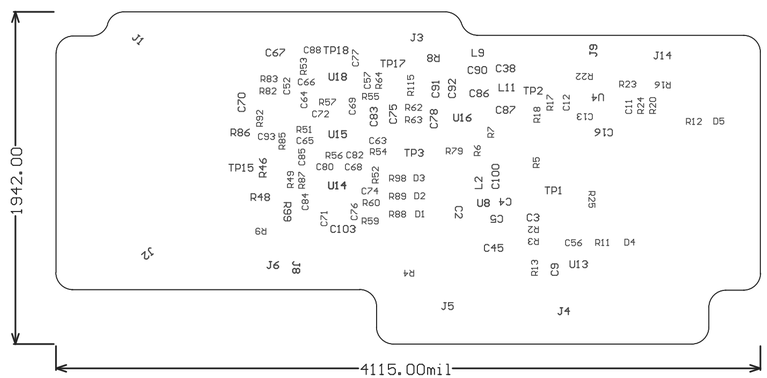


ALL ARTWORK VIEWED FROM TOP SIDE	PROJECT NAME = SM73201 - ARC EVAL	
LAYER NAME = M2 Board Outline	ARTWORK # = 880600728 002 REV A	
PLOT NAME = M3 3D STEP Top	GENERATED : 6/18/2012 2:53:41 PM	NATIONAL SEMICONDUCTOR





ALL ARTWORK VIEWED FROM TOP SIDE	PROJECT NAME = SM73201 - ARC EVAL	
LAYER NAME = M2 Board Outline	ARTWORK # = 880600728 002REV A	
PLOT NAME = M4 3D STEP Bottom	GENERATED : 6/18/2012 2:53:42 PM	NATIONAL SEMICONDUCTOR



1000 (mil)

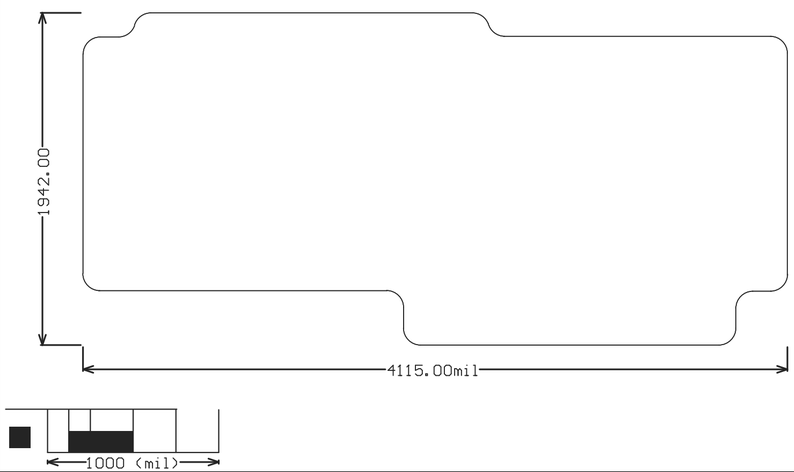
COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED, AND MAY NOT BE IN BILL OF MATERIALS
ASSEMBLY VARIANT: [No Variations]

PCB ARTWORK FOR TOP SIDE	PROJECT NAME = SM73201 - ARC EVAL	
LAYER NAME = M2 Board Outline	ARTWORK # = 880600728.002 REV A	
PLOT NAME = M5 Assembly Top	GENERATED : 6/18/2012 2:53:43 PM	NATIONAL SEMICONDUCTOR

1000 (mil)

COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED, AND MAY NOT BE IN BILL OF MATERIALS
ASSEMBLY VARIANT: [No Variations]

ALL ARTWORK VIEWED FROM TOP SIDE	EVAL	PROJECT NAME = [illegible]	PCB VIEWED FROM BOTTOM SIDE EVAL
LAYER NAME = M2 **Board Outline**		PART NO = [illegible]	REV A LAYER NAME =
PLOT NAME = M2 Assembly Bottom	PM 2:53:45	GENERATED :: 6/18/2013	2:53:44 PM Bottom Assembly M2 NATIONAL SEMICONDUCTOR



ALL ARTWORK VIEWED FROM TOP SIDE	PROJECT NAME = SM73201 - ARC EVAL	
LAYER NAME = M2 Board Dimensions	ARTWORK # = 880600728 002REV A	
PLOT NAME = M9 Title Sheet	GENERATED : 6/18/2012 2:53:45 PM	NATIONAL SEMICONDUCTOR

National Semiconductor

PROJECT TITLE:
SM73201 - ARC EVAL

FILE NAME:
SM73201-ARC TQFP.PcbDoc

FAB DRAWING NUMBER:
551600728-002REV A

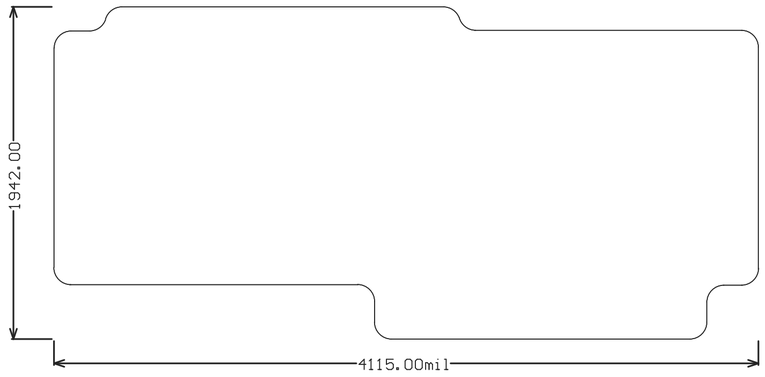
DESIGNED FOR:
National Semiconductor

SCALE: 1.00

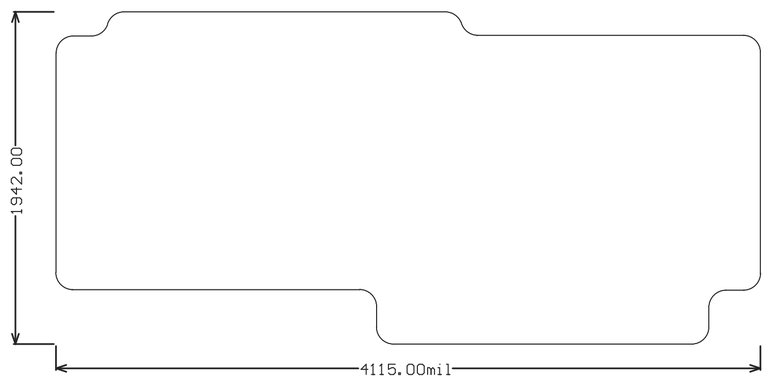
ALTIUM DESIGNER VERSION:
10.0.0.24016

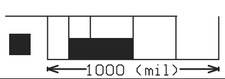
Fabrication File: 885016006 20-002 REV A

1. MATERIAL: PER IPC-4101/24
   1A. LAMINATE: RoHS AND LEAD-FREE ASSEMBLY COMPLIANT FR4 MATERIALS
   1B. FINISHED BOARD: .0014 +/-.0005 INCH TOP LAYER. AND .0014 +/-.0005 INCH BOTTOM LAYER, COPPER.
   1B. FINISHED BOARD: .0014 +/-.0005 INCH INSIDE LAYERS , COPPER.
   1C. ALL COPPER LAYERS MUST BE SPACED PER LAYER STACKUP DETAIL IN .PCBDOC FILE. SEE PICTURE AT THE BOTTOM OF THIS DOCUMENT.
   1D. BOARD THICKNESS IS MEASURED INCLUDING TOP AND BOTTOM SIDES FINISHED COPPER. ANY TIN, TIN/LEAD OR GOLD PLATING, SOLDERMASK AND SILKSCREEN LEGEND MUST NOT BE INCLUDED IN FINISHED BOARD THICKNESS.
   1E. ALL INNER LAYERS MUST BE OXIDE COATED.
2. THE CONDUCTOR PATTERN MUST BE ETCHED USING ARTWORK 880600620-002 REV A SUPPLIED WITHIN FABRICATION FILES' ARCHIVE 885600620-001 REV A OR GREATER.
3. ALL CONDUCTOR LAYERS MUST BE REGISTERED WITHIN +/- .005 INCH FROM TRUE POSITION.
4. ETCH TOLERANCES:
   4A. ALL EXTERNAL LAYERS CONDUCTOR WIDTH MUST BE WITHIN +/- .0015 INCH OR +/- 15% OF GERBER DATA, WHICHEVER IS SMALLER.
   4B. ALL INTERNAL LAYERS CONDUCTOR WIDTH MUST BE WITHIN +/- .0010 INCH OR +/- 15% OF GERBER DATA, WHICHEVER IS SMALLER.
5. BOARD MUST BE NC DRILLED USING DRILL DATA SUPPLIED.
6. DRILL TOLERANCES AND HOLE SIZES ARE FOR FINISHED BOARD:
   ALL .007 INCH DIAMETER PLATED THROUGH HOLES ARE + .001/-.010 INCH.
   ALL PLATED THROUGH HOLES TO .080 INCH ARE +/- .003 INCH.
   ALL PLATED THROUGH HOLES OVER .081 INCH ARE +/- .005 INCH.
   THERE ARE 4 NON-PLATED THROUGH HOLES, 4 HOLES HAVE DRILL 200 MIL,
   ALL NON-PLATED THROUGH HOLES ARE +/- .005 INCH.
7. ALL HOLES MUST BE REGISTERED WITHIN +/-.003 INCH FROM TRUE POSITION.
8. MINIMUM ANNULAR RING MUST BE .002 INCH.
9. PLATING:
   9A. PER MIL-C-14550, PLATED THROUGH HOLES MUST BE PLATED WITH .0008 MIN. TO .0012 INCH MAX. THICK COPPER.
   9B. FINISH: IMMERSION GOLD: 2 TO 8 MICROINCHES GOLD OVER 120-240 MICROINCHES OF ELECTROLESS NICKEL.
10. WARP AND TWIST OF FINISHED BOARDS MUST NOT EXCEED .007 INCH PER INCH.
11. SOLDERMASK: PER IPC-SM-840
   11A. SOLDERMASK BOTH TOP AND BOTTOM SIDES.
   11B. SOLDERMASK MUST CLEAR ALL LANDS SHOWN ON GERBER SOLDERMASK LAYERS.
   11C. COLOR **RED** & SOLVENT FREE.
   11D. LIQUID PHOTO-IMAGEABLE MUST BE .0002 MIN. TO .0008 MAX. INCH THICK MEASURED OVER COPPER PLATING.
12. SILKSCREEN TOP AND BOTTOM SIDES USING A GLOSSY WHITE, NONCONDUCTIVE, EPOXY BASED INK. NO SILKSCREEN ALLOWED ON TIN-LEAD OR GOLD AREAS, ON PADS OR IN HOLES.
13. ROUTE BOARD OUTLINE, PER DRAWING DIMENSIONS.
14. VENDOR MUST ENTER VENDOR'S IDENTITY, DATE CODE AND ANY OTHER IDENTIFICATION MARKS ON BOTTOM SIDE ETCH APPROXIMATELY WHERE SHOWN.
15. OTHER VENDOR NOMENCLATURE OR MARKINGS SHOULD NOT BE ETCHED OR SILKSCREENED ON BOARD WITHOUT PRIOR PERMISSION.
16. ALL VENDOR IN-PROCESS MARKINGS, QA STAMPS, ETC. MUST BE PLACED ON THE BOTTOM SIDE OF BOARD.
17. FINISHED BOARD MUST MEET UL94V-0 RATING AND RoHS COMPLIANCE.



ALL ARTWORK VIEWED FROM TOP SIDE	PROJECT NAME = SM73201 - ARC EVAL	
LAYER NAME = M20 Board Dimensions	ARTWORK # = 880600728 002REV A	
PLOT NAME = M10 Fab Notes	GENERATED : 6/18/2012 2:53:46 PM	NATIONAL SEMICONDUCTOR

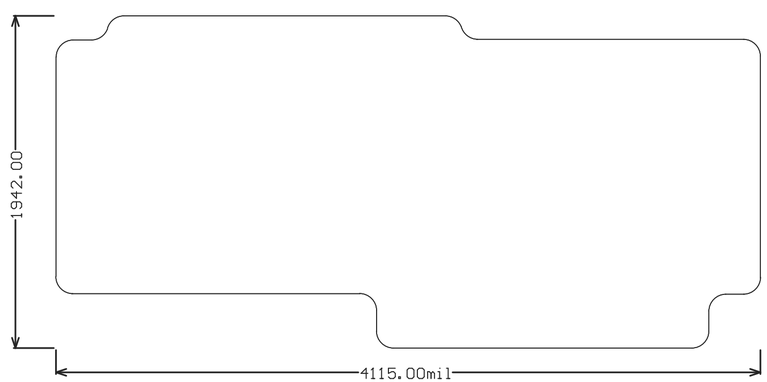


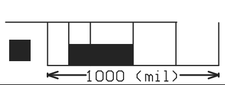


ALL ARTWORK VIEWED FROM TOP SIDE	PROJECT NAME = SM73201 - ARC EVAL	
LAYER NAME = M12 Board Dimensions	ARTWORK # = 880600728 002REV A	
PLOT NAME = M11 Gerber Information	GENERATED : 6/18/2012 2:53:48 PM	NATIONAL SEMICONDUCTOR

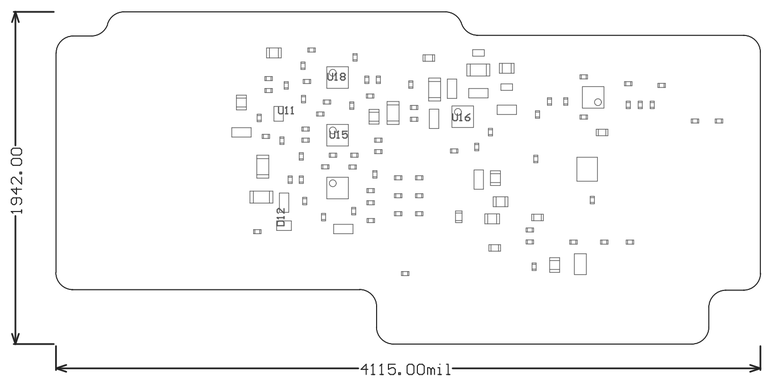
Layer Stack Up Detail for: SM73201 - ARC.PcbDoc

Layer Name	Gerber Document	Copper Thickness	Dielectric Material	
Top Solder Mask	(.GTS)		Solder Resist	
Top Layer	(.GTL)	1.4mil		
			FR-4	20.0mil
Mid-Layer 1	(.G1)	1.4mil		
			PrePreg	17.0mil
Mid-Layer 2	(.G2)	1.4mil		
			FR-4	20.0mil
Bottom Layer	(.GBL)	1.4mil		
Bottom Solder Mask	(.GBS)		Solder Resist	

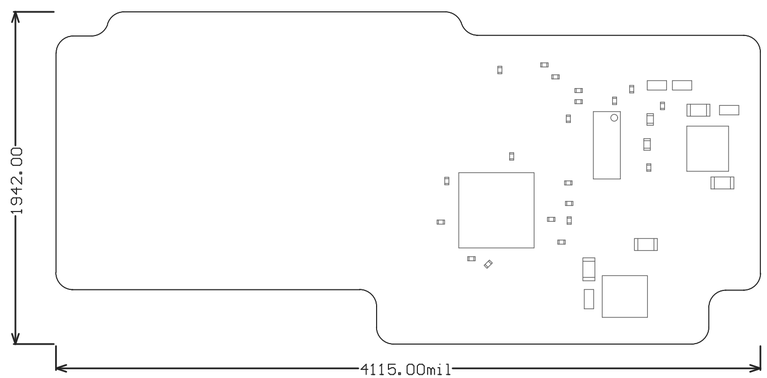


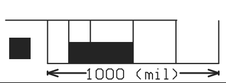


ALL ARTWORK VIEWED FROM TOP SIDE	PROJECT NAME = SM73201 - ARC EVAL	
LAYER NAME = M12 Board Dimensions	ARTWORK # = 880600728 002 REV A	
PLOT NAME = M12 Stackup	GENERATED : 6/18/2012 2:53:49 PM	NATIONAL SEMICONDUCTOR

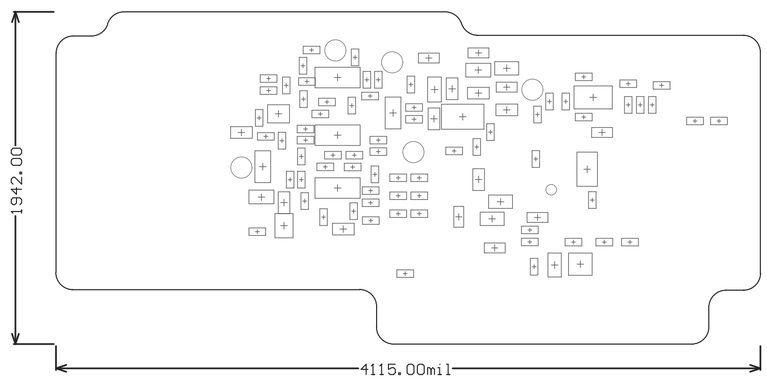


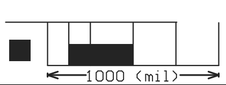
ALL ARTWORK VIEWED FROM TOP SIDE	PROJECT NAME = SM73201 - ARC EVAL	
LAYER NAME = M23 Board Dimensions Top	ARTWORK # = 880600728 002REV A	
PLOT NAME = M13 Component Bodies Top	GENERATED : 6/18/2012 2:53:49 PM	NATIONAL SEMICONDUCTOR



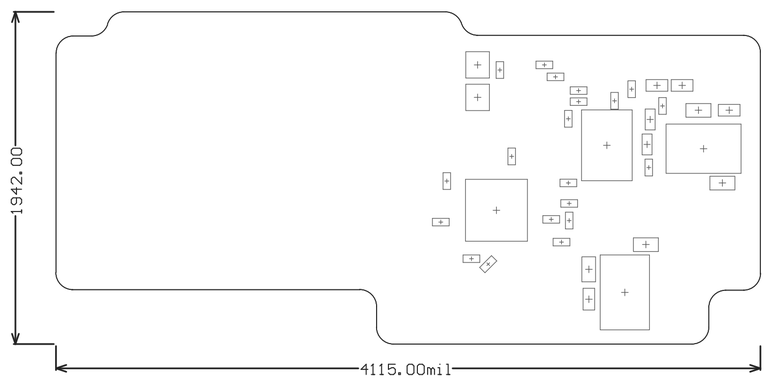


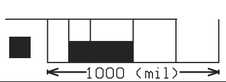
ALL ARTWORK VIEWED FROM TOP SIDE	PROJECT NAME = SM73201 - ARC EVAL	
LAYER NAME = M14 Component Bodies Bottom	ARTWORK # = 880600728 002REV A	
PLOT NAME = M14 Component Bodies Bottom	GENERATED : 6/18/2012 2:53:50 PM	NATIONAL SEMICONDUCTOR



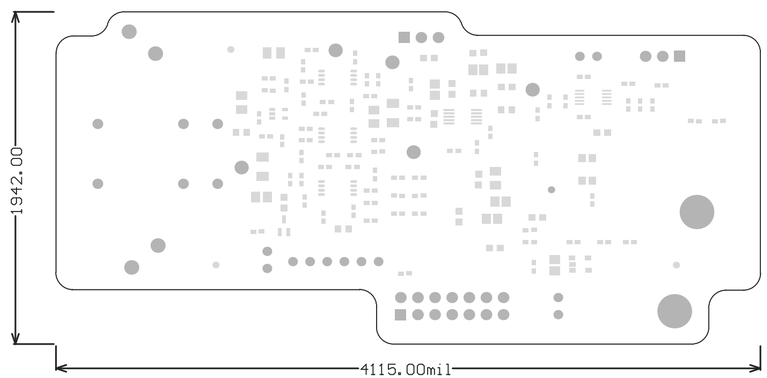


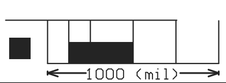
ALL ARTWORK VIEWED FROM TOP SIDE	PROJECT NAME = SM73201 - ARC EVAL	
LAYER NAME = M25 Board Outline Tops	ARTWORK # = 880600728 002REV A	
PLOT NAME = M15 Courtyards Top	GENERATED : 6/18/2012 2:53:51 PM	NATIONAL SEMICONDUCTOR



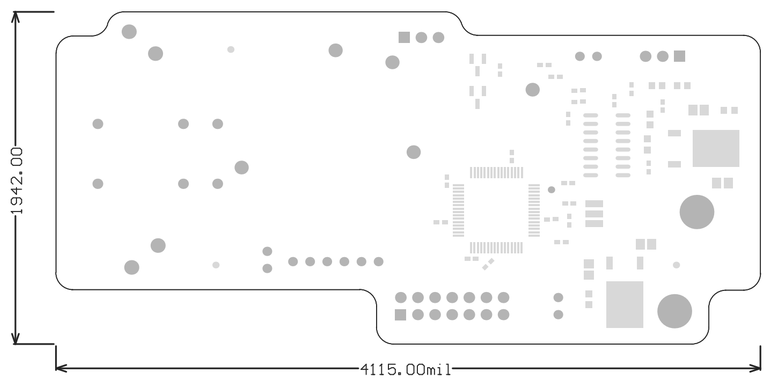


ALL ARTWORK VIEWED FROM TOP SIDE	PROJECT NAME = SM73201 - ARC EVAL	
LAYER NAME = M26Board Outline8.com	ARTWORK # = 880600728 002REV A	
PLOT NAME = M16 Courtyards Bottom	GENERATED : 6/18/2012 2:53:52 PM	NATIONAL SEMICONDUCTOR



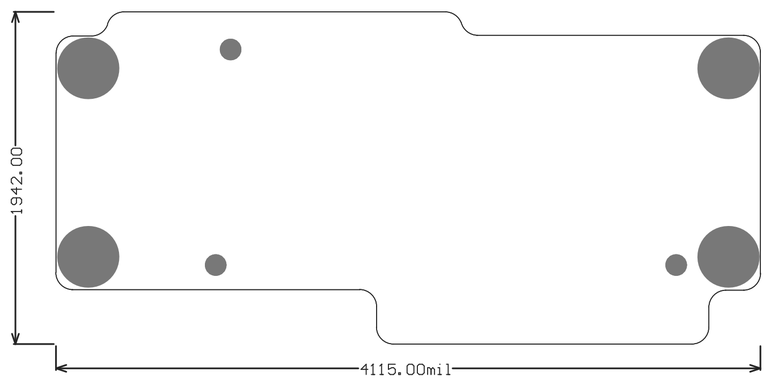


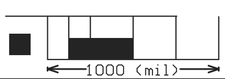
ALL ARTWORK VIEWED FROM TOP SIDE	PROJECT NAME = SM73201 - ARC EVAL	
LAYER NAME = M2 Board Outline	ARTWORK # = 880600728 002REV A	
PLOT NAME = Top Pad Master	GENERATED : 6/18/2012 2:53:53 PM	NATIONAL SEMICONDUCTOR



1000 (mil)

ALL ARTWORK VIEWED FROM TOP SIDE	PROJECT NAME = SM73201 - ARC EVAL	
LAYER NAME = M2 Board Dimensions	ARTWORK # = 880600728 002REV A	
PLOT NAME = Bottom Pad Master	GENERATED : 6/18/2012 2:53:54 PM	NATIONAL SEMICONDUCTOR



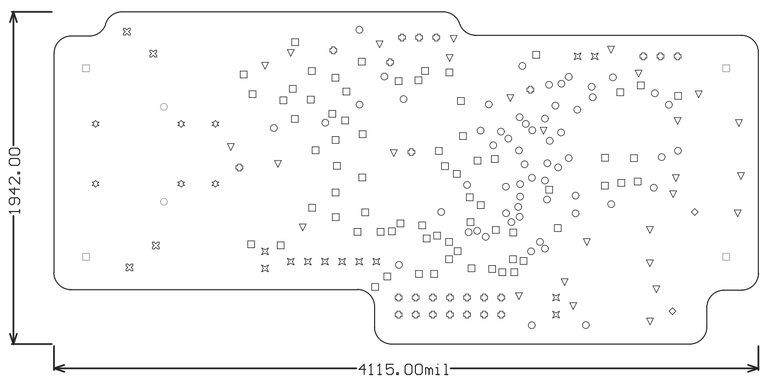


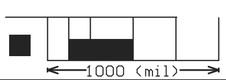
ALL ARTWORK VIEWED FROM TOP SIDE	PROJECT NAME = SM73201 - ARC EVAL	
LAYER NAME = M2 Board Dimensions	ARTWORK # = 880600728 002REV A	
PLOT NAME = Keep Out Layer	GENERATED : 6/18/2012 2:53:55 PM	NATIONAL SEMICONDUCTOR

Symbol	Hit Count	Tool Size	Physical Length	Rout Path Length	Plated	Hole Type
○	60	15mil (0.381mm)			PTH	Round
□	71	20mil (0.508mm)			PTH	Round
▽	28	28mil (0.711mm)			PTH	Round
⊠	12	35mil (0.889mm)			PTH	Round
◌	25	40mil (1.016mm)			PTH	Round
☼	6	42mil (1.067mm)			PTH	Round
⊠	4	65mil (1.651mm)			PTH	Round
◇	2	165mil (4.191mm)			PTH	Round
□	4	200mil (5.08mm)			NPTH	Round
○	2	100mil (2.54mm)	550mil (13.97mm)	450mil (11.43mm)	PTH	Slot
	214 Total					

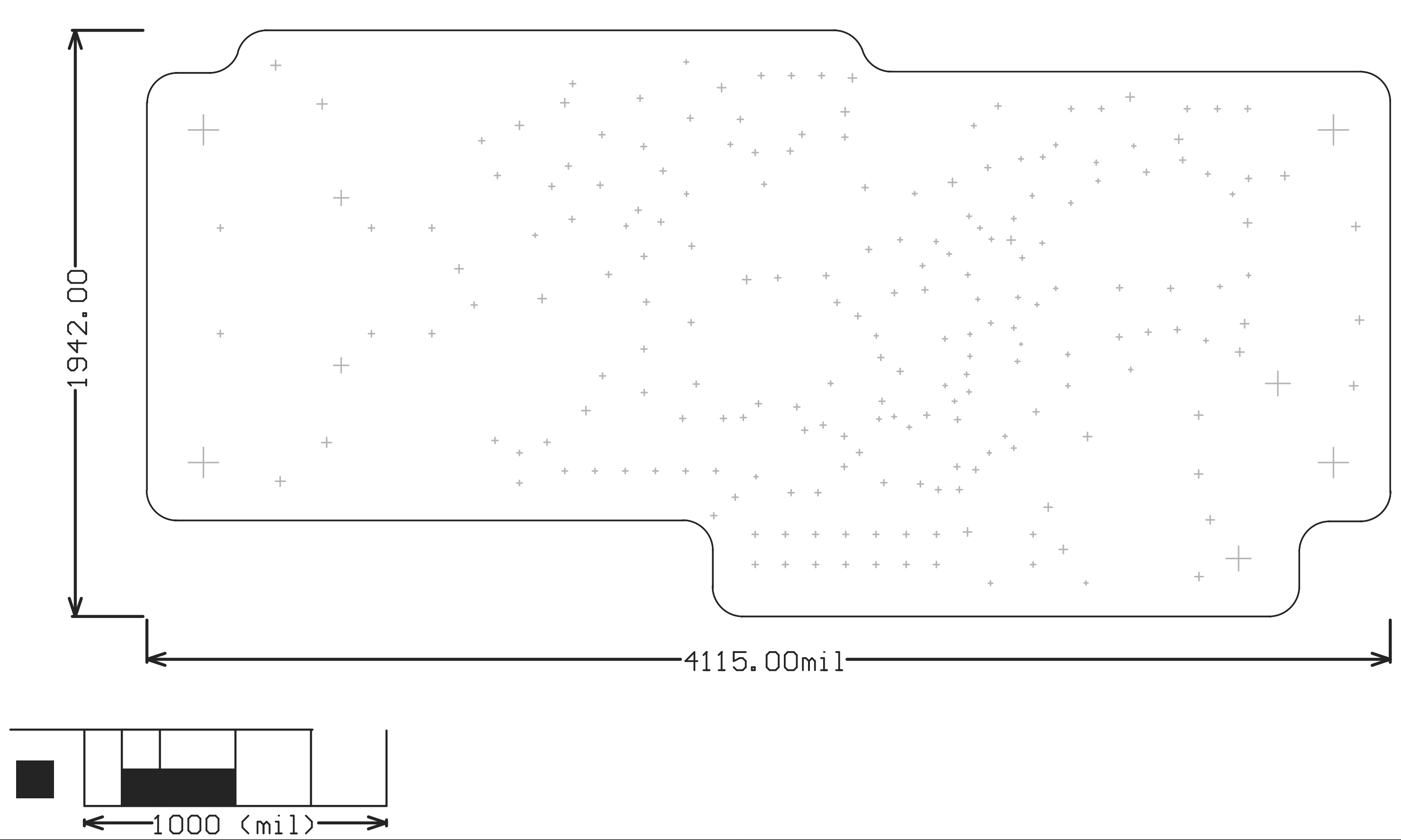
Slot definitions : **Rout Path Length** = Calculated from tool start centre position to tool end centre position.
Physical Length = Rout Path Length + Tool Size = Slot length as defined in the PCB layout

Drill Table





ALL ARTWORK VIEWED FROM TOP SIDE	PROJECT NAME = SM73201 - ARC EVAL	
LAYER NAME = [illegible]	ARTWORK # = 880600728 002REV A	
PLOT NAME = Drill Drawing For (Bottom Layer to Top Layer)	CREATED: 6/18/2012 2:53:55 PM	NATIONAL SEMICONDUCTOR



ALL ARTWORK VIEWED FROM TOP SIDE	PROJECT NAME = SM73201 - ARC EVAL	
LAYER NAME = Drill Guide / Board Outline / M2 Board Dimensions	ARTWORK # = 880600728 002REV A	
PLOT NAME = Drill Guide For (Bottom Layer,Top Layer)	GENERATED : 6/18/2012 2:53:56 PM	NATIONAL SEMICONDUCTOR