ABSTRACT

Contents
1 Affected Products ............................................................................................................ 1
2 Summary .......................................................................................................................... 2
3 TI Recommendations ........................................................................................................ 3

List of Figures
1 DLPC910 Row Operation (Current) ................................................................................... 2
2 DLPC910 Row Operation (New Implementation) ............................................................... 3

1 Affected Products
Any DLPC910 controller configured with the DLPR910A programmable read-only memory (PROM).
2 Summary

If the DLPC910 controller is configured using the DLPR910A PROM, when row cycles are sent continuously (no clocks between row cycles) while DVALID is held HIGH continuously, data will be incorrectly sent to the DMD. This includes No-Op row cycles.

This issue affects the DLPC910 controller for the DLP9000X digital micromirror device (DMD) and the DLP6500 DMD when configured with the DLPR910A PROM.

The DLPR910A PROM release (revised from DLPR910) includes modifications to the DLPC910 controller firmware. This DLPR910A update makes the DLPC910 controller compatible with both the original DLP9000X, DLP6500 and DLP9000XB, DLP6500B versions.

A consequence of these modifications is a change to the method of sending row commands continuously. Figure 1 shows the current timing diagram for DVALID during a row cycle:

NOTE: N is the number of clock edges per row cycle for the DMD. This is 40 for the DLP9000X(B) and 64 for the DLP6500(B).

Immediate action: Please see the “TI Recommendations” section (Section 3) of this technical advisory for details.
3 TI Recommendations

TI recommends implementing the solution shown in Figure 2 for all row cycle commands when using the DLPC910 controller configured with the DLPR910A PROM:

![Diagram of DLPC910 Row Operation (New Implementation)](image)

NOTE: Setting DVALID to LOW for the last clock cycle does not affect data read in the last two clock transitions. The firmware will finish the correct number of DIN_(A/B/C/D) reads for the specific DMD started by the rising edge of DVALID at the beginning of the row cycle.

In systems that will not send continuous row cycle commands no change is required, but it is recommended.

Further, this change is recommended for all versions of the DLPR910 PROM.
IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Texas Instruments Incorporated ("TI") technical, application or other design advice, services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using any particular TI Resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications (and of all TI products used in or for your applications) with all applicable regulations, laws and other applicable requirements. You represent that, with respect to your applications, you have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. You agree that prior to using or distributing any applications that include TI products, you will thoroughly test such applications and the functionality of such TI products as used in such applications. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

You are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT. AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING TI RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY YOU AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

You agree to fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of your non-compliance with the terms and provisions of this Notice.

This Notice applies to TI Resources. Additional terms apply to the use and purchase of certain types of materials, TI products and services. These include; without limitation, TI's standard terms for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm), evaluation modules, and samples (http://www.ti.com/sc/docs/sampterms.htm).

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2018, Texas Instruments Incorporated