

## EXTRACT AND DIGITIZE AC SIGNALS WITH A SINGLE A/D CONVERTER

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Unwanted portions of a signal, such as a DC pedestal, can be difficult to reject in a single supply circuit. A DC pedestal voltage most typically appears at the output of an operational amplifier with a small signal riding on top of it. This pedestal voltage is required in the analog domain to insure that the small signal that contains the pertinent information never falls below the ground potential, where clipping will occur. In order to digitize this type of signal, the DC offset forces the designer to use extremely high resolution (20 plus bits), wide dynamic range A/D converters to capture the small signal that is of interest to a reasonable resolution such as 12 bits. The  $\Delta\Sigma$  converters, ADS1210, ADS1211, ADS1212, or ADS1213, are appropriate for this function. An alternative to using a high resolution converter would be to add an analog stage where the signal is level shifted to eliminate the DC offset. Unfortunately, this may complicate matters further in creating a situation where dual supplies are required.

A better solution to rejecting the DC pedestal voltage while still digitizing the small signal is to use one device and a few passive elements. The circuit configuration, shown in Figure 1, shows how to use a differential input, 12-bit, A/D converter, two resistors and a capacitor to accomplish this final goal. In Figure 1, the single-ended output of a standard single-supply operation amplifier, such as an OPA234, is connected to the inputs of a differential-input A/D converter through an R || C network. The R || C network in conjunction with the inputs of the A/D converter is designed to reject lower frequency portions of the signal while still digitizing the signal's higher frequencies.

In Figure 1, a single supply amplifier, A<sub>1</sub>, is used as a buffer in the signal path. The output signal of the amplifier is split in two. The first signal path is through a resistor (R<sub>2</sub>) to the non-inverting input of the differential input, 12-bit A/D converter (pin 2 of the ADS7817). The second signal path is

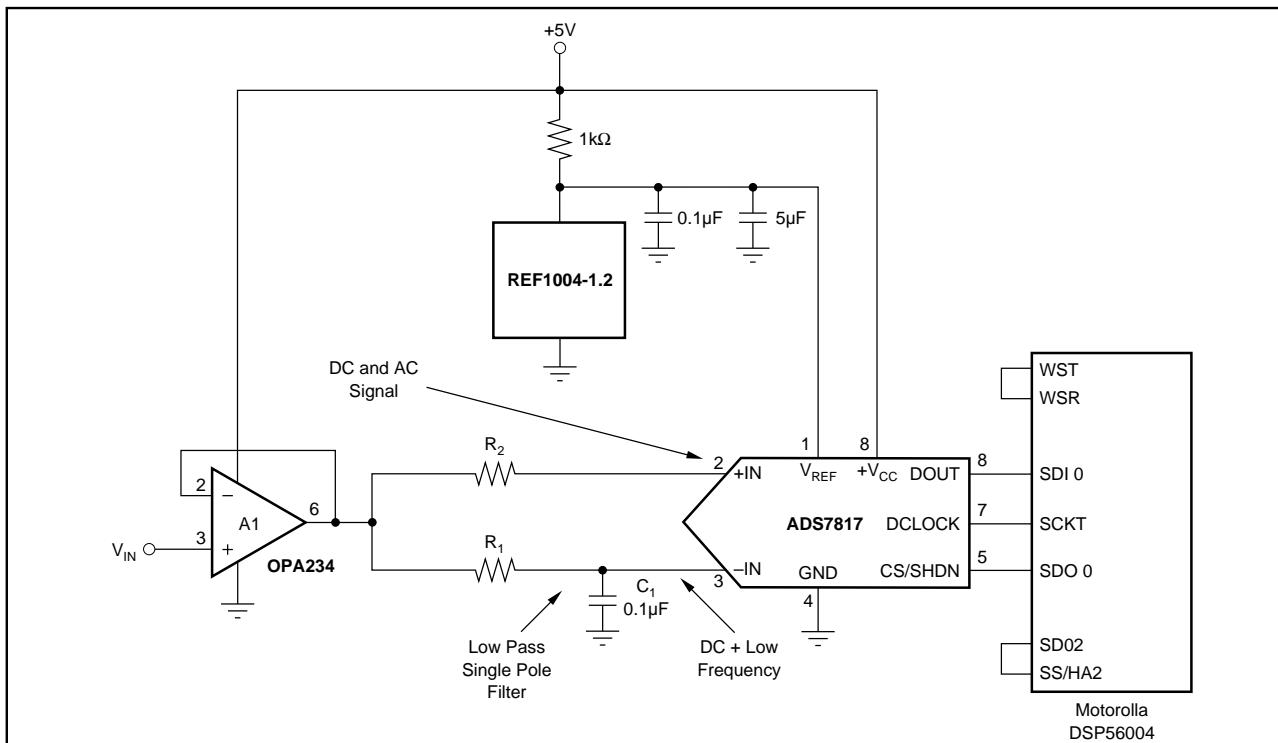


FIGURE 1. The ADS7817 in Conjunction with an R || C Network is Used to Reject DC Pedestal Voltages in a Single Supply Environment and Digitize the ac Portion of the Analog Signal. The REF1004-1.2 is a 1.2 voltage reference for the A/D converter, providing a full-scale range of 2.4Vp-p and theoretical LSB size of 0.6mV.

through an  $R \parallel C$  low pass filter (which is implemented with  $R_1$  and  $C_1$ ) and then to the inverting input of the ADS7817 (pin 3). In this circuit, the unfiltered signal is presented to the non-inverting input of the A/D converter and the DC portion of the signal is presented to the inverting input of the A/D converter. The 12-bit A/D converter will digitize the difference between its two inputs, consequently rejecting the DC portion of the signal.

A low pass filter that is implemented with  $R_1$  and  $C_1$  which blocks higher frequencies while allowing the DC voltage component of the signal to come through to the converter's inverting input. The input impedance at the inputs of the A/D converter is balanced with the addition of  $R_2$ .  $R_1$  should be equal to  $R_2$ . A large mismatch in these two resistors can cause offset errors in the conversion. Using metal-film resistors specified to 1% is acceptable. Additionally, the magnitude of  $R_1$  and  $R_2$  has an effect on the accuracy versus conversion speed of the A/D converter. As the resistor value of  $R_1$  and  $R_2$  increase, the INL and DNL errors also increase as shown in Figure 2. In contrast, the magnitude of  $C_1$  does not cause offset errors.

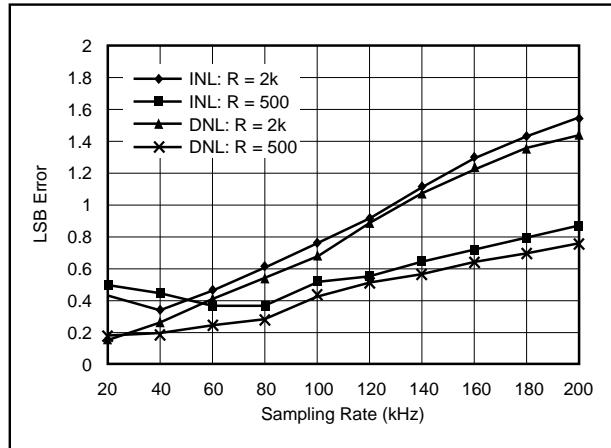


FIGURE 2. If the Resistors ( $R_1$  and  $R_2$ ) are High Enough They can Cause Errors at Higher Sampling Frequencies.

The input voltage range ADS7817 A/D converter is  $-300\text{mV}$  to  $(V_{CC} + 300\text{mV})$  for the non-inverting input ( $+IN$ ) and  $-300\text{mV}$  to  $(V_{CC} - 1\text{V})$  for the inverting input ( $-IN$ ). Since the inverting input does not swing all the way to the positive power supply rail, it is used for the input terminal of the DC component of the input signal.

The differential input range of the A/D converter is equal to:

$$-V_{REF} \leq (V_{+IN} - V_{-IN}) \leq +V_{REF},$$

where

$V_{REF}$  is the reference voltage of the ADS7817 (pin 1)

$V_{+IN}$  is the signal voltage at the non-inverting input of the ADS7817 (pin 2)

$V_{-IN}$  is the signal voltage at the inverting input of the ADS7817 (pin 3)

Now that the DC element of the signal has been extracted, the ADS7817 voltage reference can be used to accurately digitize the remaining small signal. The reference voltage to the converter is used to control the LSB size of the 12-bit converter. At a full-scale voltage reference of  $2.5\text{V}$ , the converter has an input range of  $5\text{Vp-p}$  and is accurate to 12 bits. As the reference voltage is lowered the input range is decreased as well as the theoretical LSB size. While the theoretical LSB size becomes smaller, there are limitations to the effective number of bits that the converter can output with a given reference voltage. The effective number of bits versus the reference voltage is shown in Figure 3. Table I shows the relationship between the reference voltage, theoretical LSB size and effective LSB size. It is useful to note that any changes in the reference voltage will not change the absolute input ranges of either input.

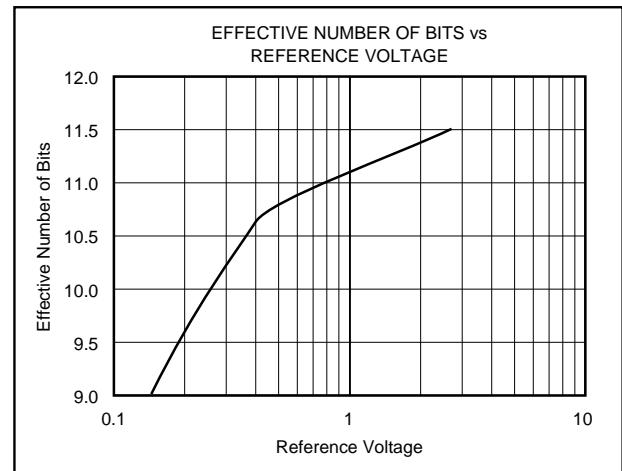


FIGURE 3. Effective Number of Bits Versus Reference Voltage for the ADS7817, 12-Bit A/D Converter.

REFERENCE VOLTAGE ( $V_{REF}$ in Volts)	INPUT VOLTAGE RANGE ( $V_{+IN} - V_{-IN}$ )	THEORETICAL LSB SIZE (mV)	EFFECTIVE LSB SIZE (mV, typ)
2.5	-2.5V to +2.5V	1.22	1.73
1.0	-1.0V to +1.0V	0.488	0.911
0.4	-0.4V to +0.4V	0.195	0.481
0.2	-0.2V to +0.2V	0.0977	0.515

TABLE I. The ADS7817 Reference Voltage can be Adjusted in Order to Change the Effective LSB Size of a Typical Low Grade Part.

As illustrated in Table I, the combination of DC rejection with the  $R \parallel C$  network on the front end of the converter and the adjustment of the converter's voltage reference to  $400\text{mV}$  will digitize the analog signal to a  $515\mu\text{V}$  level of accuracy (10.6 bits) with an LSB size of  $195\mu\text{V}$  (12 bits).

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