

ADS8342 SAR ADC Inputs

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ABSTRACT

Successive approximation register analog-to-digital converters (SAR ADCs) present a challenging load to the circuitry that drives the analog inputs. Specifications in data sheets may mislead the user into thinking that analog inputs, for example, are static, when in fact they create a highly dynamic load that requires specially designed buffer circuitry. This article looks at the architecture of modern SAR ADCs, specifically the ADS8342, and examines the sampling and conversion processes in detail. This analysis highlights the considerations needed for designing input buffer circuitry to drive these ADCs with optimal results.

Contents

1	The SAR ADC Structure	1
2	The Sampling Process in Detail	2
3	Charge Distribution During the Sampling Process	6
4	Conversion	7
5	Conclusion.....	9

List of Figures

1	Representative SAR Input Stage	2
2	Initial Phase of the Sampling Period	3
3	Resetting the Value of the Capacitive Conversion Network	3
4	Sampling of the Input Signal	4
5	Initial Phase of the Conversion Cycle.....	5
6	Capacitive Conversion Network for 16-Bit SAR ADS8342	5
7	Simplified Circuit of SAR ADS8342	6

1 The SAR ADC Structure

Figure 1 presents the simplified structure of the ADS8342 showing the converter core and front-end input circuitry. The negative input signal to the ADC core, V_{IN-} , is connected to the signal ground or COMMON pin. The positive input signal to the ADC core, V_{IN+} , comes from the four-position multiplexer. In this way, the ADS8342 is able to sample four different input signals. At the core of the ADC, the 16-bit capacitive conversion network of the ADS8342 is replaced with three representative capacitors. Looking at these three bits, we will examine an equivalent 3-bit conversion sequence. The most significant bit (MSB) capacitor for ADS8342 has a value of 20pF. The next capacitor to the MSB capacitor will have half its value, or 10pF. In this example we have a 3-bit converter so the least significant bit (LSB) capacitor will have one quarter of the MSB capacitor value, or 5pF. To make conversion ideal, a termination capacitor having the same value as the LSB capacitor is added. The effect of this is that the sum of all the capacitors below the MSB becomes 20pf, the same as the MSB.

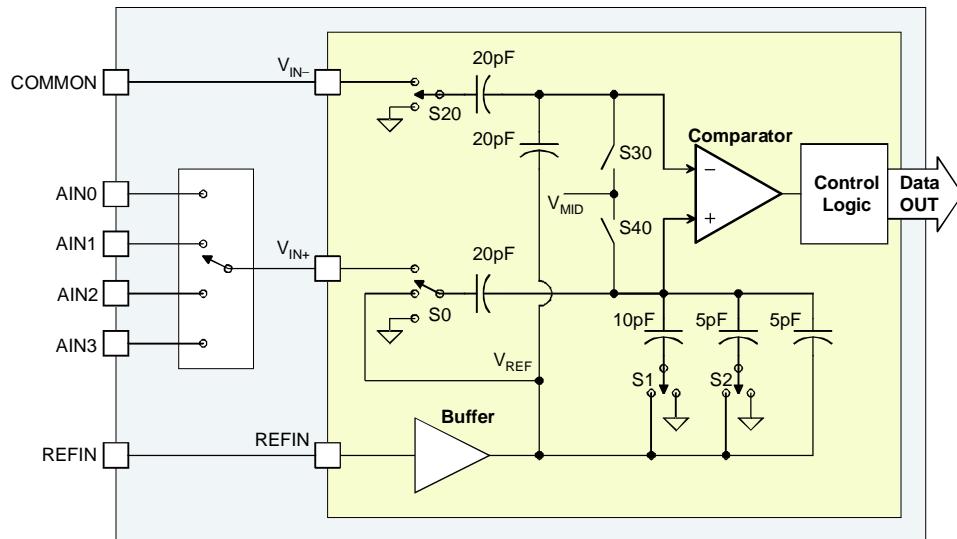


Figure 1. Representative SAR Input Stage

The positive analog input, V_{IN+} , is sampled by the MSB capacitor through switch S0 and the capacitive conversion network composed of three capacitors and two switches, S1 and S2. The negative analog input, V_{IN-} , is sampled by two MSB-valued capacitors in series through switch S20.

The external reference voltage is applied to the REFIN input and is buffered by the internal buffer, then distributed to all switches that are part of the conversion process. On the other hand, switches S30 and S40 are connected to the middle voltage V_{MID} .

The comparator input signals are connected in parallel to switches S30 and S40. During conversion, the comparator output will be processed by the control logic, which will properly set up switches S0, S1 and S2.

Note that this type of architecture is for the ADS8342 and similar, bipolar input range parts. Other parts may be similar but not identical.

2 The Sampling Process in Detail

At the end of the conversion process, the ADS8342 will automatically go into the sampling process. The position of the switches S0, S1 and S2 in the capacitive conversion network are unknown. Switch S0 can be closed to either ground or the reference voltage. The status of the switches depends of the results of the previous conversion.

We know that during conversion, switch S20 is always connected to the ground. The sampling process will initiate closing switches S30 and S40. This shorts the comparator inputs and connects them to the middle voltage V_{MID} . This beginning of the sampling cycle is shown in Figure 2.

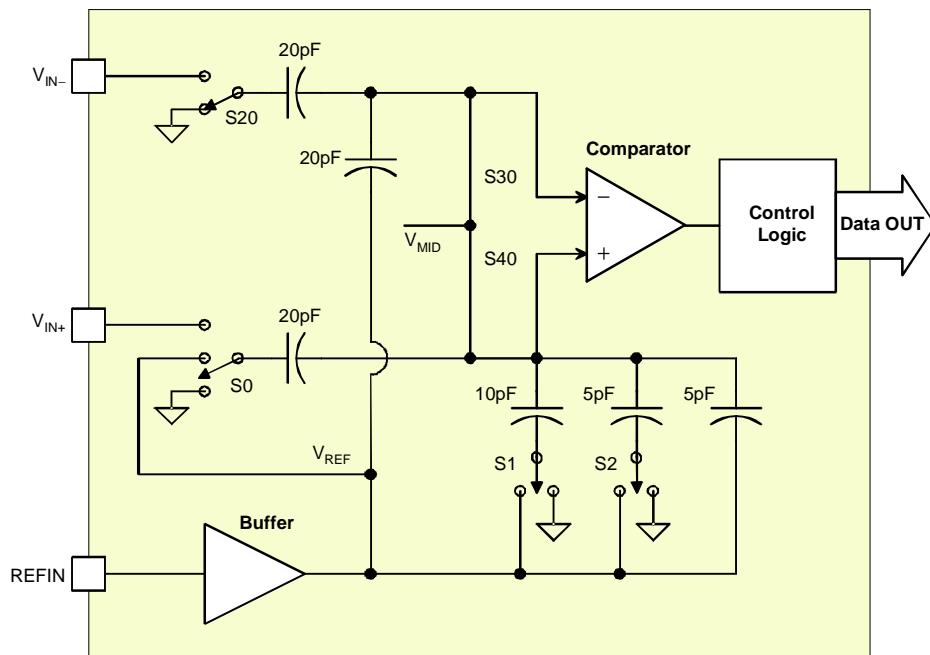


Figure 2. Initial Phase of the Sampling Period

Because the positions of switches S1 and S2 are unknown, the equivalent capacitance of the network is also unknown. For proper sampling, the capacitive conversion network must have an equivalent capacitance that is equal to the MSB capacitor. To obtain this value, switches S1 and S2, in the following step, must connect their associated capacitors to the reference voltage. (In this way, the positive input, as well as the negative input, of the comparator will be connected over the MSB capacitor equivalent value to V_{REF} .) This will reset the capacitor conversion network value and is shown in [Figure 3](#).

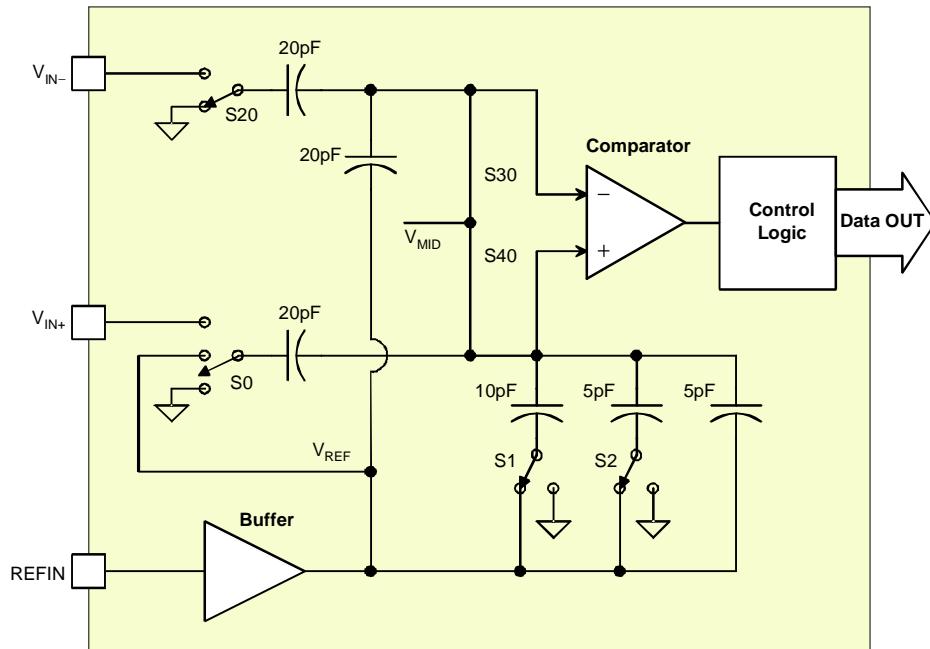


Figure 3. Resetting the Value of the Capacitive Conversion Network

The Sampling Process in Detail

Up to this point, all changes only affect the internal operation of the ADS8342. The analog input signals were not affected by these changes. In the next step, input switches S0 and S20 close, and the input signal will be sampled on the input MSB capacitors. This period is the most critical period for the input buffer circuit. To obtain accurate results from the conversion, the input buffer must be capable of charging the sampling MSB capacitors to the proper value during the sampling period. The sampling of the input signal is shown in [Figure 4](#).

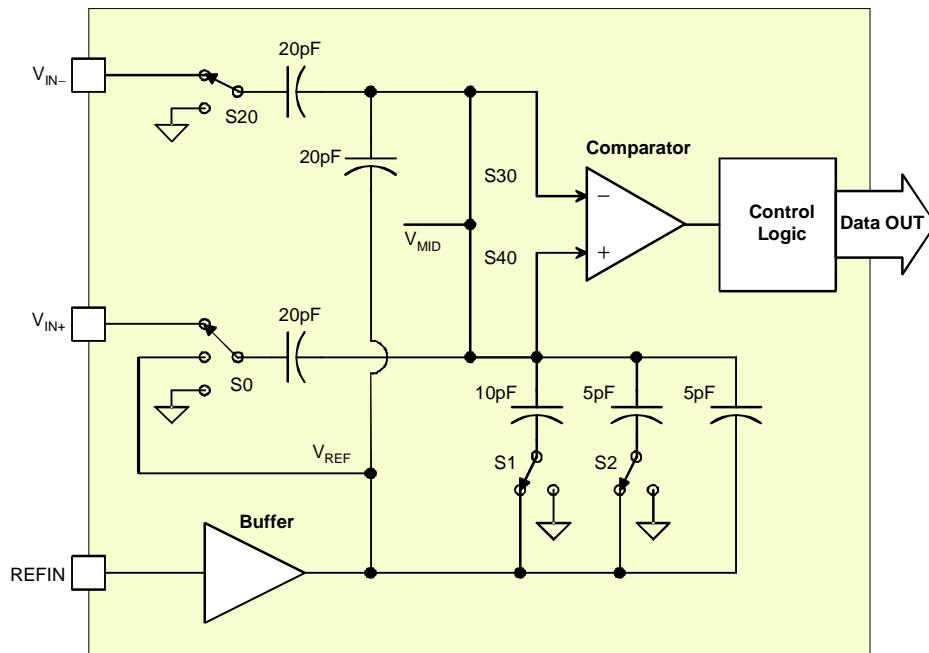


Figure 4. Sampling of the Input Signal

After charging the sampling capacitor with the input voltage, the preparation for the conversion cycle starts by opening switches S30 and S40. Once these two switches are open, the charge on the sampling capacitors will be frozen. This leads to the end of the sampling period, with the disconnection of the MSB capacitors from the analog inputs V_{IN+} and V_{IN-} and connecting them to ground with switches S0 and S20. The end of the sampling period and start of the conversion cycle is shown in [Figure 5](#).

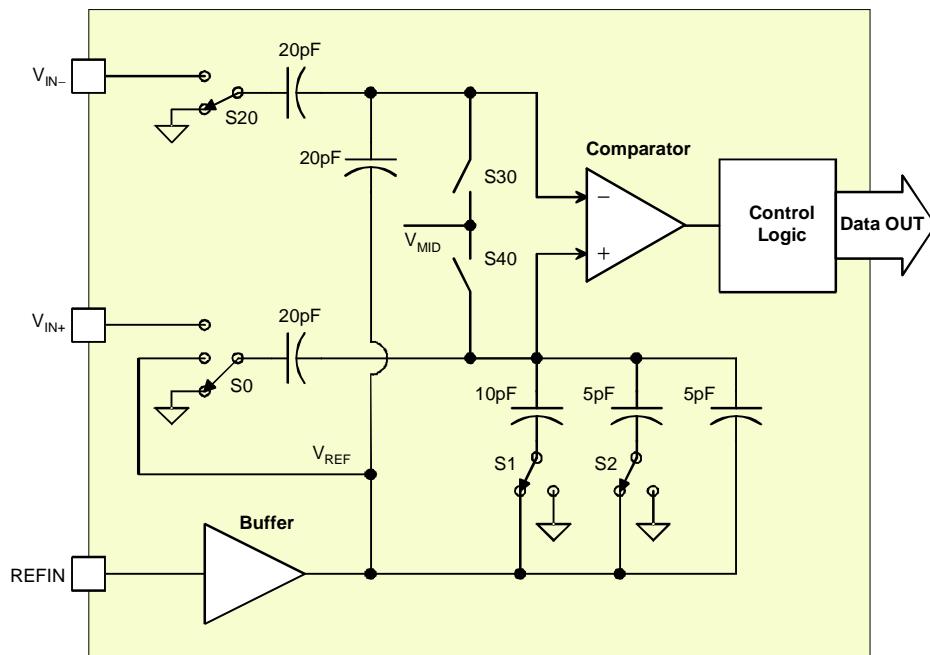


Figure 5. Initial Phase of the Conversion Cycle

This representative analysis is done on a 3-bit ADC and a capacitive conversion network composed of three capacitors and two switches. This capacitive conversion network can be replaced with the real one from the ADS8342 as shown in [Figure 6](#).

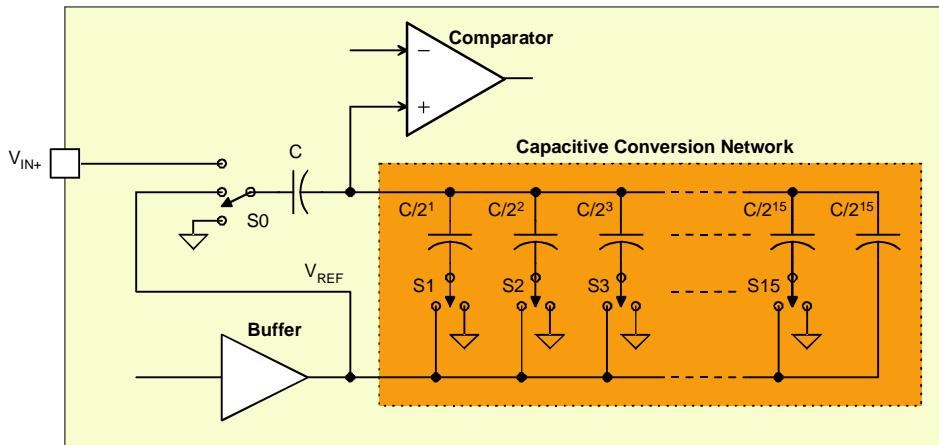


Figure 6. Capacitive Conversion Network for 16-Bit SAR ADS8342

The sampling or MSB capacitor connected to switch S0 has the standardized value C or 20pF. The capacitive conversion network as presented in [Figure 6](#) has an equivalent capacitive value equal to the value of the MSB capacitor, C. For the 16-Bit SAR ADS8342, the capacitive conversion network will be composed of 16 capacitors and 15 switches. The first capacitor has a value that is one-half of the standardized MSB capacitor value, or $(0.5 \times C)$. The second capacitor has a value that is one-fourth the value of C, the third one has a value that is one-eighth the value of C, and so on. The last two capacitors each have a value that is $1/2^{15^{\text{th}}}$ part of the value of C. The resolution of the SAR ADC is equivalent to the number of switches and capacitors that are in the capacitive conversion network, and their respective values.

Charge Distribution During the Sampling Process

3 Charge Distribution During the Sampling Process

To explain the question of charge distribution during the sampling and conversion period, we will use the simplified circuit of the ADS8342 as shown in [Figure 7](#). This circuit is a combination of the circuits from [Figure 2](#) and [Figure 6](#).

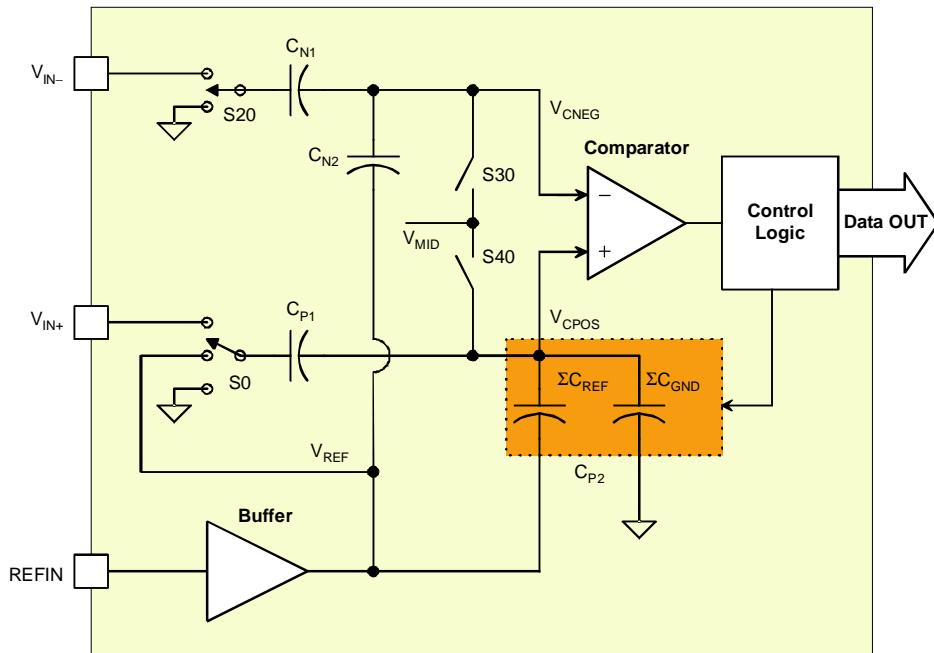


Figure 7. Simplified Circuit of SAR ADS8342

In order to analyze this circuit, we will start by describing the position of the sampling or MSB capacitor. The MSB capacitor (C_{P1}) is connected to switch $S0$ and the positive input, and has the standardized value C , or 20pF. The sampling capacitor (C_{N1}) that is connected to switch $S20$ and the negative input also has the standardized value C . The capacitive conversion network as presented in [Figure 6](#) has an equivalent capacitive value equal to the value of the MSB capacitor C , and is presented as capacitor C_{P2} in [Figure 7](#). The position of switches $S1$ to $S15$ is unknown, so the sum of all capacitors connected to the reference voltage will be presented as ΣC_{REF} , and all capacitors connected to ground as ΣC_{GND} . The comparator negative input has voltage V_{CNEG} and positive input V_{CPPOS} .

The measured signal is connected to the positive input V_{IN+} and negative input V_{IN-} . As described in [Section 2](#), the sampling of the input signal starts by closing switches $S30$ and $S40$. In this way, the positive input voltage V_{CPPOS} to the comparator is equal to the middle voltage, V_{MID} . Simultaneously, the negative input voltage V_{CNEG} to the comparator is also equal to V_{MID} . The next step is to close switches $S1$ to $S15$ to V_{REF} . Switches $S0$ and $S20$ remain open. Now the ADC is ready to sample the input signal. The sampling process starts by closing input switches $S0$ and $S20$ to the input analog signal.

After a transition period, the voltages stabilize and the new situation is present. The existing configuration from [Figure 7](#) demonstrates the positive charge, Q_{PS} , that charges capacitors C_{P1} and C_{P2} . [Equation 1](#) explains this charge distribution sequence.

$$Q_{PS} = C_{P1} \cdot (V_{MID} - V_{IN+}) + C_{P2} \cdot (V_{MID} - V_{REF}) \quad (1)$$

Following the same procedure, the negative charge Q_{NS} that charges capacitors C_{N1} and C_{N2} is described by [Equation 2](#).

$$Q_{NS} = C_{N1} \cdot (V_{MID} - V_{IN-}) + C_{N2} \cdot (V_{MID} - V_{REF}) \quad (2)$$

The next step in the sampling process starts by opening switches $S30$ and $S40$. In this way, the negative V_{CNEG} and positive V_{CPPOS} input voltages into the comparator are not tied together anymore. The charge Q_{PS} on the capacitors C_{P1} and C_{P2} , as well as the charge Q_{NS} on the capacitors C_{N1} and C_{N2} , will be frozen.

Next, the input switches S0 and S20 open. To initiate the comparison or the conversion process, switches S0 and S20 will be close to ground. The positive comparator input voltage V_{CPOS} will have a new value, V_X . Now the charge of the two capacitors C_{P1} and C_{P2} can be described by [Equation 3](#).

$$Q_{PC1} = C_{P1} \cdot (V_X - V_{GND}) + C_{P2} \cdot (V_X - V_{REF}) \quad (3)$$

Following the same procedure, the charge of capacitors C_{N1} and C_{N2} and the negative comparator input voltage V_{CNEG} will have the new value V_Y , and can be described by [Equation 4](#).

$$Q_{NC1} = C_{N1} \cdot (V_Y - V_{GND}) + C_{N2} \cdot (V_Y - V_{REF}) \quad (4)$$

The charges of capacitors C_{P1} and C_{P2} during the sampling and conversion processes are the same. Combining [Equation 1](#) and [Equation 3](#), the result is [Equation 5](#).

$$C_{P1} \cdot (V_{MID} - V_{IN+}) + C_{P2} \cdot (V_{MID} - V_{REF}) = C_{P1} \cdot (V_X - V_{GND}) + C_{P2} \cdot (V_X - V_{REF}) \quad (5)$$

Solving [Equation 5](#) for V_X is shown in [Equation 6](#).

$$V_X = V_{MID} - \frac{C_{P1}}{C_{P1} + C_{P2}} \cdot V_{IN+} + \frac{C_{P1}}{C_{P1} + C_{P2}} \cdot V_{GND} \quad (6)$$

Substituting V_{GND} with 0, the result is [Equation 7](#).

$$V_X = V_{MID} - \frac{C_{P1}}{C_{P1} + C_{P2}} \cdot V_{IN+} \quad (7)$$

A similar procedure is then applied to the negative side of the input stage. If the charges of capacitors C_{N1} and C_{N2} during the sampling and conversion are the same, we can combine [Equation 2](#) and [Equation 4](#), as presented in [Equation 8](#).

$$C_{N1} \cdot (V_{MID} - V_{IN-}) + C_{N2} \cdot (V_{MID} - V_{REF}) = C_{N1} \cdot (V_Y - V_{GND}) + C_{N2} \cdot (V_Y - V_{REF}) \quad (8)$$

Solving [Equation 8](#) for V_Y is shown in [Equation 9](#).

$$V_Y = V_{MID} - \frac{C_{N1}}{C_{N1} + C_{N2}} \cdot V_{IN-} + \frac{C_{N1}}{C_{N1} + C_{N2}} \cdot V_{GND} \quad (9)$$

Substituting V_{GND} with 0, the result is given in [Equation 10](#).

$$V_Y = V_{MID} - \frac{C_{N1}}{C_{N1} + C_{N2}} \cdot V_{IN-} \quad (10)$$

4 Conversion

When the sampling of the input signal ends, the conversion process begins by opening switches S30 and S40, capturing the input analog signal. Next, the sample switches S0 and S20 are opened, as explained in [Section 3](#). Descriptions in this section refer to [Figure 7](#).

4.1 The Negative Input Signal

First, let us look at the negative input signal side. We will refer to the comparator negative input node at S30 as V_{CNEG} . The negative input signal side is set up as an input-signal-voltage-dependent reference for the comparator. Switch S20 switches from V_{IN-} to V_{GND} . The charge stored in the negative input signal side capacitors C_{N1} and C_{N2} , during conversion Q_{NC} , is ideally the same as the charge stored during sampling Q_{NS} . As a result, the charge sum on capacitors C_{N1} and C_{N2} is conserved.

Capacitors C_{N1} and C_{N2} are equal and have the same value. The negative input comparator voltage V_Y (referring to [Equation 10](#)) is now V_{CNEG} , and is constant during the entire conversion period; it can be described by [Equation 11](#). Additionally, because V_{MID} is connected to the analog ground, it is replaced with 0.

$$V_{CNEG} = \frac{-C_{N1}}{C_{N2} + C_{N2}} \cdot V_{IN-} \quad (11)$$

In the case of the ADS8342, V_{IN-} is connected and equal to V_{GND} ; consequently, very little charge redistribution occurs on the negative input signal side during and after sampling.

4.2 The Positive Input Signal

The conversion process is made by comparing the dynamic signal V_{CPOS} with the constant voltage V_{CNEG} described by [Equation 11](#). In [Figure 7](#), capacitor C_{P2} is an equivalent presentation of the sum of the capacitors, ΣC_{REF} , connected to the reference voltage V_{REF} , and the sum of the capacitors, ΣC_{GND} , connected to the ground voltage V_{GND} , over associated switches S1 through S15 (see [Figure 6](#)). During the conversion, the distribution of the capacitors ΣC_{REF} and ΣC_{GND} will change, so that the difference between voltages V_{CPOS} and V_{CNEG} is minimized.

On the positive input signal side, the transition from sampling into testing the MSB is similar to the negative input signal side. We will refer to the comparator positive input node at S40 as V_{POS} (see [Figure 5](#)). The positive input signal side is set up as a variable input signal voltage for the comparator. Switch S0 switches from V_{IN+} to V_{GND} and switches S1 through S15 remain connected to V_{REF} (see [Figure 6](#)). The charge stored in the positive input signal side capacitors C_{P1} and C_{P2} , during conversion Q_{PC} , is ideally equivalent to the charge stored during sampling Q_{PS} . The charge on the total capacitor array is the same during conversion as during sampling. C_{P1} and C_{P2} is conserved. Thus, the V_{POS} is used in [Equation 12](#) to describe the charge on the capacitive conversion network during the conversion process.

$$Q_{PC1} = (C_{P1} + C_{P2}) \cdot V_{CPOS} - \Sigma C_{REF} \cdot V_{REF} - \Sigma C_{GND} \cdot V_{GND} \quad (12)$$

4.3 Testing the Bits

At the end of the first clock cycle, voltages V_{CPOS} and V_{CNEG} are compared by the comparator, resolving the value of the MSB to either a 1 or a 0. This value will be latched into the SAR control logic. If the value is 1, the C_{P1} capacitor remains connected over switch S0 to V_{GND} . If the value is 0, it will be connected over the same switch to V_{REF} .

To understand the rest of the conversion process, we need to refer to the capacitive conversion network presented in [Figure 7](#). At the same clock edge, the control logic of the SAR converter shifts to test the next most significant bit, which will be referred to as bit2. Switch S1 from [Figure 6](#) switches from V_{REF} to ground. The charge on the capacitor array will again be redistributed, placing a load on the reference buffer.

The state of the capacitor array is now a function of the decision made during the MSB test. Each bit test that follows will be a function of the preceding bit test. The voltage on V_{CPOS} becomes dependent on which capacitors from the capacitive conversion network are connected to V_{REF} and which are connected to V_{GND} . Under these conditions, combining [Equation 1](#) and [Equation 12](#), the positive input voltage V_{CPOS} to the comparator can be described by [Equation 13](#) through [Equation 15](#).

$$-C_{P1} \cdot V_{IN+} - C_{P2} \cdot V_{REF} = (C_{P1} + C_{P2}) \cdot V_{CPOS} - \Sigma C_{REF} \cdot V_{REF} - \Sigma C_{GND} \cdot V_{GND} \quad (13)$$

$$V_{CPOS} = \frac{-C_{P1}}{C_{P1} + C_{P2}} \cdot V_{IN+} - \frac{C_{P2}}{C_{P1} + C_{P2}} \cdot V_{REF} + \frac{\Sigma C_{REF}}{C_{P1} + C_{P2}} \cdot V_{REF} \quad (14)$$

$$V_{CPOS} = \frac{-C_{P1}}{C_{P1} + C_{P2}} \cdot V_{IN+} - \left(1 - \frac{C_{P1}}{C_{P1} + C_{P2}}\right) \cdot V_{REF} + \frac{\Sigma C_{REF}}{C_{P1} + C_{P2}} \cdot V_{REF} \quad (15)$$

In each of these equations, ΣC_{REF} (as explained previously) represents the sum of all capacitors at the comparator positive input tied to the reference voltage V_{REF} .

4.4 The End of Conversion

This testing sequence continues until the final bit is tested. We can assume that at the end of the conversion, the negative input signal into the comparator V_{CNEG} is equal to the positive input signal into the comparator V_{CPPOS} . Combining [Equation 11](#) and [Equation 15](#), we can relate V_{CPPOS} and V_{CNEG} by [Equation 16](#). The purpose of the conversion is to drive the positive input signal into the comparator V_{CPPOS} to the same value of V_{CNEG} .

$$\frac{-C_{N1}}{C_{N1} + C_{N2}} \cdot V_{IN-} = \frac{-C_{P1}}{C_{P1} + C_{P2}} \cdot V_{IN+} - \left(1 - \frac{C_{P1}}{C_{P1} + C_{P2}}\right) \cdot V_{REF} + \frac{\Sigma C_{REF}}{C_{P1} + C_{P2}} \cdot V_{REF} \quad (16)$$

It is interesting to note that for any given resolution, with any given input signal, the state of the capacitors at the end of conversion is given by [Equation 17](#), which is obtained by solving [Equation 16](#) for the input signal, or ($V_{IN+} - V_{IN-}$). The values of capacitors C_{N1} and C_{P1} are equal and will be replaced with C_1 ; because the values of C_{N2} and C_{P2} are equal, as well, these will be replaced with C_2 .

$$V_{IN+} - V_{IN-} = \frac{C_1 + C_2}{C_1} \cdot \left[\frac{\Sigma C_{REF}}{C_1 + C_2} - \left(1 - \frac{C_1}{C_1 + C_2}\right) \right] \cdot V_{REF} \quad (17)$$

Moreover, because C_1 and C_2 have the same value, we can replace them with C in [Equation 18](#), giving us a final equation that describing the conversion process.

$$V_{IN+} - V_{IN-} = \left(\frac{\Sigma C_{REF}}{C} - 1 \right) \cdot V_{REF} \quad (18)$$

The more positive the value of the input signal, or ($V_{IN+} - V_{IN-}$), the greater the proportion of capacitors that are tied to the reference voltage V_{REF} . At positive full-scale, $V_{IN+} - V_{IN-} = +V_{REF}$, and all capacitors from the capacitor conversion network will be tied to V_{REF} . Alternately, if $V_{IN+} - V_{IN-} = -V_{REF}$, then no capacitors are tied to V_{REF} , or all of them are tied to V_{GND} .

Since that $\Sigma C_{REF} / C$ is in the range of 0 to 2, then we can see that the input analog signal $V_{IN+} - V_{IN-}$ is in the range from $-V_{REF}$ up to $+V_{REF}$, from [Equation 18](#).

Note that the ADS842 complements the most significant bit in the output code. The MSB indicates negative signals with a '1'. If the MSB is a '1' internally, indicating the input signal is positive, it will be a '0' in the output code.

5 Conclusion

This application report has highlighted several key considerations for designing input buffer circuitry in order to drive SAR ADCs with optimum performance. The first step in designing driver or buffer circuits for analog input into the ADC is a full understanding of the input structure operation. This understanding leads to a complete grasp of the performance requirements for the buffer circuit. It is not simply looking at the circuit that will enable better design; the dynamic circuit input requires careful layout and component selection, which is not obvious at first glance.

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