**ABSTRACT**

High-speed digital-to-analog converters (DACs) most often use a transformer-coupled output stage. In applications where this configuration is not practical, a single op amp differential to single-ended stage has often been used. This application note steps through the exact design equations required to achieve gain matching from each output as well as a matched input impedance to each of the DAC current outputs. An example high-speed design is shown using the very wideband, current feedback OPA695 op amp with additional suitable parts included in a summary table.

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1  Typical High-Speed DAC Output Interface Circuits

Emerging high speed DACs use a complementary current-steering output structure. This design generates a differential signal current determined by the input coding sitting on top of an average common-mode current determined by one-half of the maximum tail current (which is sometimes an adjustable feature in the DAC). Most data sheet characterizations are taken with a very simple transformer output interface. A typical circuit from the DAC5675A (a 14-bit, 400MSPS device) is shown in Figure 1.

![Figure 1. Typical Output Interface for a High-Speed, Current Steering Output DAC](image)

This particular DAC wants to sink current from a supply voltage that is equal to the positive supply voltage of the DAC. It also has limited compliance voltage below that level—in this case, only a 1V swing below \( AV_{DD} \) is allowed. Other DACs drive current into ground and look for a ground-referenced external load to convert the current to a voltage. A circuit similar to that shown in Figure 1 is nearly always used to develop the DAC performance specifications.

Where a transformer interface is not suitable, a single amplifier differential to single-ended conversion may be implemented. This configuration would be useful where lower frequencies, or a DC-coupled interface, are required out of the DAC. Additionally, a single SOT23 amplifier is more suitable where minimal board area for the interface is desired. Figure 2 illustrates a typical interface shown in some DAC data sheets.

![Figure 2. DC-Coupled, Differential to Single-Ended DAC Interface](image)

This 20mA peak output current DAC is looking for a 25Ω termination impedance, and is driving current into ground—thus, the ground-referenced load resistors. This relatively simple-looking circuit is, however, not giving a matched gain nor a matched input impedance for the two current source outputs. As DAC speeds have increased, the resistor values around this amplifier stage need to be relatively low in order to avoid parasitic bandlimiting. This condition causes this simple equal resistor design approach to be increasingly in error if matched voltage swings at the DAC outputs are desired. \( C_{OPT} \) is used to slow the DAC update edge rates as an optional element.
While this design may still yield acceptable results in the application, it is a simple matter to adjust these resistor values slightly to get perfect gain match from the two output currents to the amplifier output and also provide exactly the same apparent resistive load to each output. Implementing this adjustment also moves in the direction of giving better channel linearity and, therefore, lower distortion. Achieving matched gain magnitudes also moves the mid-scale DC output (when both output currents are equal to $I_p / 2$) closer to 0V at the op amp output. The designs here assumed bipolar supplies for the op amp where a 0V output is desired when each DAC channel is at $(I_p / 2)$ (mid-scale). While there might be other, more dominant, distortion mechanisms that mask this improvement, it is preferable to remove this unmatched output voltage swing as a possible source of imbalance.

To balance this design, start with the full design circuit of Figure 3, and write the gain and input impedance equations looking into each port. Define the desired gain as $G$ (which will be an impedance) and input impedance $Z_i$ (which will also be an impedance).

![Figure 3. Analysis Circuit for Single Amplifier (Differential to Single-Ended Conversion)](image)

From a solution standpoint, there are six resistors to find here and only four design targets. Consequently, a single unique solution is not possible without two more targets. To simplify this design, we will select a feedback resistor value and then also simply select $R_2$ as a scaled version of $R_1$. An alternative condition on the non-inverting network might be to get matched source impedances for the op amp bias current to reduce output DC offset (if the op amp is a voltage feedback type). Since a current feedback amplifier was anticipated here, with unmatched input bias currents, no source matching constraint was imposed.

The feedback resistor is a common gain element to both DAC current outputs and needs to be selected for best bandwidth if a current feedback amplifier is used in the circuit of Figure 3. Even if a voltage feedback amplifier is used, $R_2$ needs to be set at a relatively low value for high-speed designs in order to minimize interaction with inverting input parasitic capacitance. On the non-inverting input side, the DAC $I^+$ current sees a relatively simple input impedance to generate the voltage at $R_1$. This voltage is then attenuated to the $V^+$ input by $R_2$ and $R_3$. Getting from the voltage at $R_1$ ($V_1$) to the $V^+$ input also needs to be done with relatively low resistor values to avoid parasitic bandlimiting due to the input capacitance at $V^+$.

The design proceeded with an assumption that $R_2$ will be set to a ratio of $R_1$. An added consideration in scaling the $R_2$ to $R_3$ divider is that these resistor values must be low enough that the apparent source impedance looking out of $V^+$ does not become a dominant noise contributor, either because of the Johnson noise of the resistors or the gain provided to the non-inverting input noise current by the equivalent source impedance $(R_3 || [R_1 + R_2])$. 

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**Wideband Complementary Current Output DAC to Single-Ended Interface: Improved Matching for the Gain and Compliance Voltage Swing**

SBAA135—June 2005
2 Detailed Design Equations

Starting at the I+ input, the input impedance will be:
\[ Z_i = R_1 \parallel (R_2 + R_3) \]  

(1)

Once we have that impedance, and set it equal to the target value of \( Z_i \), there will be a simple resistor divider to the V+ input that we will define as \( \alpha = R_3 / (R_2 + R_3) \).

\[ V_{I+} = \alpha Z_i \]  

(2)

A simple approach would then assume that \( V^- = V^+ \). For a voltage feedback amplifier, that is normally a good assumption if the loop gain is high. For a current feedback amplifier, there is a buffer between the two inputs that has a gain slightly less than 1.00 (1). That slight gain loss is included in this analysis as a \( \beta \) term; therefore, the gain from the current source at the non-inverting input to the op amp output will be:

Non-inverting gain:
\[ \frac{V_O}{I^+} = \alpha Z_i \beta \left( 1 + \frac{R_F}{R_G + R_4} \right) = G \]  

(3)

Where \( G \) is the desired gain in ohms.

The approximate value of this buffer gain can be derived from the reported CMRR for the current feedback amplifier chosen. Equation 4 gives the conversion from CMRR to buffer gain for a current feedback amplifier:

\[ \beta = \left( 1 - 10^{-\text{CMRR}/20} \right) \]  

(4)

Note that this non-inverting gain includes the termination resistor to ground on the inverting input side (\( R_4 \)). This term has often been neglected in setting up these circuits because \( R_4 \) is often \( << R_G \). In higher speed circuits, this becomes less true as \( R_G \) becomes lower and \( R_4 \) needs to be included in the equation for the \( I^+ \) gain.

On the inverting side, the gain for \( I^- \) is relatively simple. By superposition, we get a current divider to set the current into \( R_G \), then the \( R_F \) resistor as the gain to the output. This value will again be set to the target gain of \( G \); note also that this value is actually an inverting gain, where a current into the input gives a negative-going output. Equation 5 assumes this condition, and works only with the gain magnitude.

Inverting gain:
\[ \frac{V_O}{I^-} = \frac{R_4}{R_4 + R_G} R_F = G \]  

(5)

The inverting input impedance is a more interesting question. At first look, it would appear to simply be the parallel combination of \( R_4 \parallel R_G \). However, if we think about what voltage will be generated at this DAC output pin (\( V_2 \)), we need to consider that an inverted current version is simultaneously going into the other side of the circuit, producing an inverted voltage swing at \( V^- \). This dependent source will have the effect of slightly reducing the apparent impedance of the \( R_G \) resistor when we realize that \( V^- \) is moving simultaneously in the opposite direction of \( V_2 \). Figure 4 shows the analysis circuit for this inverting input impedance.

![Figure 4. Inverting Z4 Analysis Circuit](image-url)
Steps to resolve the apparent input impedance looking into $R_4$:

$$I_b = \frac{V_2}{R_4} + \frac{V_2 - V^-}{R_G}$$

[where $I_b$ is the signal portion of $I^-$ in Figure 3]

(6)

but:

$$V^- = -I_bZ_i\alpha\beta$$  [non-inverting input $Z_i$ used here]

(7)

from the non-inverting side. Grouping terms, we get:

$$I_b\left(1 - \frac{Z_i\alpha\beta}{R_G}\right) = V^-\left(\frac{1}{R_4} + \frac{1}{R_G}\right)$$

(8)

Then:

$$\text{Inverting } Z_i = \frac{V_2}{I_b} = (R_4 \parallel R_G)\left(1 - \frac{Z_i\alpha\beta}{R_G}\right)$$

(9)

with the non-inverting $Z_i$ assumed equal to the inverting (as a design goal), and after some manipulations to isolate $Z_i$:

$$Z_i = \frac{R_G}{1 + \frac{R_G}{R_4} + \alpha\beta}$$

(10)

Using the two gain equations and the inverting input impedance Equation 10, a solution for $R_G$ may be derived as the solution to the quadratic Equation 11 (see Appendix A).

$$R_G^2 + R_G\left(R_F - 2G - \frac{Z_iR_F}{G}\right) - Z_iR_F\left(\frac{R_F}{G} - 1\right) = 0$$

(11)

Once $R_G$ is determined to simultaneously satisfy the two gain and inverting input impedance equations (Equation 11), we can work backwards to calculate values for the remaining elements. Specifically, set $R_4$ to get the desired gain for the inverting input current, according to Equation 12, by solving Equation 5 for $R_4$:

$$R_4 = \frac{R_G}{G - 1}$$  [from Appendix A, Equation A–3]

(12)

Then set $\alpha\beta$ to get the non-inverting gain by solving Equation 3 for $\alpha\beta$:

$$\alpha\beta = \frac{G}{Z_i\left(1 + \frac{R_F - G}{R_G}\right)}$$

(13)

Using the known value for $\beta$ (or set $\beta = 1$ for a voltage feedback amplifier), we can solve for $\alpha$ by dividing the result above by $\beta$.

Then from $\alpha$ and $Z_i$:

$$R_1 = Z_i\left(1 + \frac{1 - \alpha}{\lambda}\right)$$

(14)

This calculation finds the necessary resistor to ground at $I^+$. Then, to set $R_2$ and $R_3$, simply pick $R_2$ = some ratio of $R_1$ (typically, 2 or lower, defined as $\lambda$):

$$R_2 = \lambda R_1$$  just pick $\lambda$

(15)

(Choose $\lambda < 1$ to reduce apparent source impedance for the $V^+$ input; choose $\lambda > 1$ if $R_1$ as the dominant portion of the non-inverting input $Z_i$ is desired.)

$$R_3 = \frac{\lambda\alpha R_1}{1 - \alpha}$$

(16)
3 Example Design Using Very Wideband Current Feedback Amplifiers

To see the difference that this more detailed design approach gives, consider a design using the OPA695 wideband current feedback amplifier where the DAC wants to see a 25Ω load impedance to ground on each output, and we want 50Ω gain to the op amp output for each half of the output signal. This design should give a 100Ω total gain from the I_D (as defined here) to the output voltage. The OPA695 is looking for a feedback resistor in the 500Ω region and quotes a typical CMRR of 56dB. That 56dB CMRR translates into a β = 0.99842 for the buffer gain across from V+ to V− (Equation 4). With a 500Ω feedback, the OPA695 will give > 600MHz bandwidth.

As an initial design, consider the more typical approach shown in Figure 5. Here, the termination resistors (R_1 and R_2) are simply set to 25Ω; the amplifier resistors are set to 500Ω and 250Ω to achieve a gain of 2 x 25Ω = 50Ω to the output for both I+ and I− (approximately, as we will see).

![Figure 5. Initial Design Using the OPA695](image)

Now, use the equations developed above to adjust the resistors slightly to improve the gain match and input impedance match to the desired targets. This adjustment is shown in Figure 6, where the feedback resistor stays at 500Ω; all the other values have adjusted slightly. This new design is showing resistor values to two decimal places. This precision is not possible in practice, but was carried through here to allow a comparative simulation to be made showing ideal conditions. Here, R_2 = 2 x R_1 was selected.

![Figure 6. Improved Design Using the OPA695](image)
The ideal gain for $I_B$ to $V_O$ should be $100\Omega$, or 40dB in log terms. Figure 7 illustrates the simulated gain for the designs in Figure 5 and Figure 6, showing that the values of Figure 6 approach the desired 40dB gain much more closely.

**Figure 7. Simulated Frequency Response Comparison**

If the two input impedances are matched, adding $V_1$ and $V_2$ should yield 0V (recognizing that with matched magnitudes of input $Z$, the signal voltages will be inverted from each other at $V_1$ and $V_2$). Figure 8 compares the swept frequency addition of $(V_1 + V_2)$ in log terms. This value is simply the difference in the apparent input impedance at each current source output. The 9dB of the initial design translates into a 2.8$\Omega$ difference, while the −46dB of the improved design at low frequencies translates into a 0.005$\Omega$ difference. For a 20mA output DAC, the design of Figure 5 would see a 56mV difference in the $V_{PP}$ on the output current sources, while the result of Figure 6 would be only 0.1mV difference in the voltages ($V_{PP}$) appearing at each DAC output. As we can see, the improved design of Figure 6 does a much better job of achieving matched input impedances at the two DAC outputs. To the extent that a small portion of the final distortion might be a result of an unmatched voltage swing on the two DAC outputs, this improved design should remove that unmatched voltage swing as a possible source of distortion.

**Figure 8. Simulated Difference in the Input Voltage**

The improved design is showing a low frequency delta of −46dB, which translates into a 0.005$\Omega$ difference in the input impedances. The increasing slope of the improved curve of Figure 8 traces out the rolloff in the open-loop transimpedance gain for the OPA695 (a current feedback amp). As frequency increases, more inverting error current is required to generate the output voltage. This error current increase also acts to increase the apparent input impedance looking into $V_2$. This effect is very slight, and only becomes significant at very high frequencies. The improved plot in Figure 8 only shows a delta input impedance that rises above 1$\Omega$ (0dB) beyond 200MHz.
Another way to look at this input impedance match is to simply look at the apparent impedance at $V_1$ and $V_2$ over frequency. We can see a frequency dependence as a result of the parasitic input capacitances on the two op amp input pins and the loop gain rolloff at very high frequency. Figure 9 shows the input impedance for the simple design of Figure 5.

![Figure 9. Input Impedance at $V_1$ and $V_2$ for Original Design](image)

This plot clearly indicates that the two input impedances are quite mismatched—even at low frequencies. Figure 10 shows the input impedance for the improved design of Figure 6.

![Figure 10. Improved Design Impedance at $V_1$ and $V_2$](image)

This plot illustrates a better match on each side to the 25Ω target, with an increasing deviation above 300MHz.

4 Bandwidth and Noise Considerations

So far, this discussion has been directed at improving the input impedance match and getting the target gains from each DAC output current to the amplifier output. The specific resistor values chosen also influence the AC characteristics for the final design. In general, higher resistor values produce more noise to the output pin of the op amp. If the amplifier is a current feedback type, the value of the feedback resistor always controls the bandwidth. Increasing $R_F$ from its recommended value bandlimits the design, while decreasing it peaks the frequency response up, thereby extending the bandwidth.
Figure 11 shows the spot-noise calculation circuit for any op amp.

![Spot-noise calculation circuit](image)

\[ 4kT = 16E - 20J \cdot \frac{T}{290^K}, \text{T is temperature in Kelvin} \]

- \( E_{NI} = \text{Op Amp Input Noise Voltage} \)
- \( I_{BN} = \text{Op Amp Non-inverting Input Noise Current} \)
- \( I_{BI} = \text{Op Amp Inverting Noise Current} \)
- \( E_{RS} = \text{Source Resistor Noise Voltage} = \sqrt{4kTR_S} \)
- \( E_{RF} = \text{Feedback Resistor Noise Voltage} = \sqrt{4kTR_F} \)
- \( I_{RG} = \text{Gain Setting Resistor Noise Current} = \frac{4kT}{\sqrt{R_G}} \)

**Figure 11. Output Noise Analysis Circuit**

For the design of Figure 3, the \( R_S \) resistor is \((R_3 \parallel [R_1 + R_3])\), and the \( R_G \) resistor for this noise calculation is the sum of the \( R_G + R_4 \). The other term needed is the noise gain, \( G_N \). This term is the non-inverting voltage gain, and is equal to:

\[
1 + \frac{R_F}{(R_G + R_4)} = G_N
\]

for the circuit of Figure 3. With all of these terms known, the total spot output noise density is given by Equation 18 (2):

\[
E_O = \sqrt{E_{Ni}^2 + (I_{BN}R_S)^2 + 4kTR_S} \cdot G_N^2 + (I_{BI}R_F)^2 + 4kTR_FG_N \]

(18)

All current feedback op amps have a relatively high inverting input current noise, while most (but not all) have a relatively high non-inverting input current noise. To limit the contribution of these current noise terms, it is preferable to use relatively low resistor values for both the feedback resistor and the terms that make up \( R_S \) in Equation 18. To reduce the source \( R_S \) on the non-inverting input, the next design scales the \( R_2 \) resistor to target a lower value than \( R_1 \) and still achieve the required impedance and gain targets.
5 Improved Component Selection and Results with Standard 1% Values

Let us repeat the design above and extend the bandwidth by picking a lower value for $R_F$; then reduce the noise as well, by selecting an $R_2 = 0.2 \times R_1$ (instead of $R_2 = 2 \times R_1$ that was used previously). Then, adjust the resistors to standard 1% values and repeat the input impedance and gain simulations over frequency.

Select $R_F = 402 \Omega$. Continue to target a gain of 50Ω for each output and 25Ω input impedance. Table 1 shows the exact values for the design and the standard 1% values used in simulation.

<table>
<thead>
<tr>
<th>RESISTOR</th>
<th>EXACT VALUE (Ω)</th>
<th>ENTER STANDARD 1% (Ω)</th>
<th>COMPUTED RESULTS USING 1% VALUES</th>
</tr>
</thead>
<tbody>
<tr>
<td>R1</td>
<td>53.63</td>
<td>53.6</td>
<td>Non-inverting $Z_i = 24.87\Omega$ (Eq. 1)</td>
</tr>
<tr>
<td>R2</td>
<td>10.73</td>
<td>10.7</td>
<td>Non-inverting Gain = 49.51Ω (Eq. 3)</td>
</tr>
<tr>
<td>R3</td>
<td>36.11</td>
<td>35.7</td>
<td>Inverting Input $Z_i = 25.22\Omega$ (Eq. 10)</td>
</tr>
<tr>
<td>R4</td>
<td>31.28</td>
<td>31.6</td>
<td>Inverting Gain = 50.29Ω (Eq. 5)</td>
</tr>
<tr>
<td>$R_G$</td>
<td>220.24</td>
<td>221</td>
<td></td>
</tr>
<tr>
<td>$R_F$</td>
<td>402.00</td>
<td>402</td>
<td></td>
</tr>
</tbody>
</table>

The total output noise for the OPA695 interface alone is $11nV/\sqrt{Hz}$, using these reduced resistor values. The total output noise for the circuit values shown in Figure 6 ($R_F = 500\Omega$ and $R_2 = 2 \times R_1$) is $13.4nV/\sqrt{Hz}$ using the analysis of Figure 11.

Substitute the 1% values shown above into the circuit of Figure 3, then simulate the frequency response and input impedance difference over frequency. Figure 12 shows the frequency response (together with the earlier frequency responses) with this reduced $R_F$ design. Figure 13 shows the $20\log (|V_1 + V_2|)$ for the two earlier designs and this 1% standard value design superimposed.

NOTE (1): 40dB is 100Ω gain from a single $I_b$ output from the DAC.

Figure 12. Frequency Response Curves
Working with this lower 402Ω feedback has extended the bandwidth quite a bit with minimal peaking. The upper curve in Figure 12 is showing less than ±0.5dB deviation from 40dB gain through 500MHz, with a −3dB bandwidth of 700MHz.

As for input impedance matching, this 1% standard value design comes in at a −9dB level—this translates into the approximate 0.3Ω input impedance mismatch shown in Table 1. It then follows the high frequency curve of the ideal valued design above 100MHz.

6 Conclusions

Using a bit more effort to design the single amplifier differential to single-ended interface for a DAC output can yield a more balanced design. The equations shown here adjust the resistor values slightly and balance the voltage swing seen by the DAC, thereby removing an imbalanced voltage swing as a possible source of spurious-free dynamic range (SFDR) degradation. From the exact values shown in Figure 6, standard values should be selected that are close to the specified values and still produce an improved performance over the simple design of Figure 5. Table 2 summarizes the key specifications for a range of high-speed amplifiers that may be used in this application. The table is sorted in ascending 2VPP output bandwidth order. A design spreadsheet implementing the equations in this application note is available for download with this application note.

The spreadsheet, set to the values used for the reduced $R_F$ and 1% standard value design of Table 1, is shown in Appendix B.

7 References

## Table 2. Typical High-Speed Amplifiers for High-Speed DAC Interface Requirements

<table>
<thead>
<tr>
<th>PART NO.</th>
<th>VFB or CFB</th>
<th>RECOMMENDED RF (Ω)</th>
<th>GAIN OF 2 BANDWIDTH (MHz)</th>
<th>SUPPLY CURRENT (mA)</th>
<th>CMRR (dB)</th>
<th>BUFFER GAIN (^{(\beta)})(^{(2)})</th>
<th>SLEW RATE (\text{2V}_{\text{pp}}) BW (V/µs)</th>
<th>APPROX. 2(\text{V}_{\text{pp}}) BW (MHz)</th>
<th>INPUT NOISE TERMS</th>
<th>POWER SUPPLY RANGE (V_{\text{S}+} - V_{\text{S}-})</th>
<th>MINIMUM (V)</th>
<th>MAXIMUM (V)</th>
<th>COMMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>THS4031</td>
<td>VFB</td>
<td>330</td>
<td>100</td>
<td>7.5</td>
<td>95</td>
<td>1</td>
<td>100</td>
<td>23</td>
<td>1.60</td>
<td>1.20</td>
<td>1.20</td>
<td>9.00</td>
<td>32.00</td>
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<tr>
<td>OPA820</td>
<td>VFB</td>
<td>402</td>
<td>250</td>
<td>5.6</td>
<td>85</td>
<td>1</td>
<td>240</td>
<td>54</td>
<td>2.50</td>
<td>1.70</td>
<td>1.70</td>
<td>4.00</td>
<td>12.60</td>
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<td>VFB</td>
<td>604</td>
<td>170</td>
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<td>1</td>
<td>300</td>
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<td>5.80</td>
<td>0.05</td>
<td>0.05</td>
<td>2.70</td>
<td>5.50</td>
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<td>0.9996</td>
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<td>9.00</td>
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<td>VFB</td>
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<td>150</td>
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<td>95</td>
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<td>VFB</td>
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<td>120</td>
<td>4.3</td>
<td>80</td>
<td>1</td>
<td>600</td>
<td>120</td>
<td>9.50</td>
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<td>3.70</td>
<td>2.90</td>
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<td>CFB</td>
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<td>1.00</td>
<td>10.00</td>
<td>9.00</td>
<td>32.00</td>
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<td>CFB</td>
<td>1200</td>
<td>150</td>
<td>0.94</td>
<td>60</td>
<td>0.9990</td>
<td>540</td>
<td>122</td>
<td>4.40</td>
<td>5.10</td>
<td>11.60</td>
<td>3.50</td>
<td>12.60</td>
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<td>OPA684</td>
<td>CFB</td>
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<td>820</td>
<td>160</td>
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<td>1000</td>
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<td>95</td>
<td>1</td>
<td>800</td>
<td>180</td>
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<td>3.80</td>
<td>3.80</td>
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<td>5.50</td>
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<td>1210</td>
<td>210</td>
<td>9.5</td>
<td>78</td>
<td>0.9999</td>
<td>7300</td>
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<td>17.00</td>
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<td>32.00</td>
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<td>402</td>
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<td>65</td>
<td>1</td>
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<td>220</td>
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<td>3.30</td>
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<td>402</td>
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<td>56</td>
<td>0.9984</td>
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<td>225</td>
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<td>653</td>
<td>1.80</td>
<td>18.00</td>
<td>22.00</td>
<td>4.00</td>
<td>12.60</td>
</tr>
</tbody>
</table>

(1) Sorted according to ascending \(2V_{\text{pp}}\) output bandwidth.  
(2) CFB amplifiers only.
Appendix A  Derivation of the Quadratic in \( R_G \)

To solve for \( R_G \):
\[
\frac{R_4}{R_G + R_4} = \frac{G}{R_F} \quad \text{[from inverting gain]}
\] (A-1)

Invert this to:
\[
1 + \frac{R_G}{R_4} = \frac{G}{G}
\]
(A-2)

And solve:
\[
R_4 = \frac{R_G}{\frac{R_F}{G} - 1} \quad \text{[use this as Equation 12, page 5]}
\] (A-3)

\[
\alpha \beta Z_i \left( 1 + \frac{G}{R_4} \right) = G \quad \text{[from non-inverting gain]}
\] (A-4)

where:
\[
\frac{R_F}{R_G + R_4} = \frac{G}{R_4} \quad \text{replaces}: \quad \frac{R_F}{R_G + R_4} \quad \text{[from Equation 3, page 4]}
\]
(A-5)

Substituting Equation A-3 in place of \( R_4 \) in Equation A-4 gives:
\[
\alpha \beta Z_i \left( 1 + \frac{G}{\frac{R_F}{R_G}} \left( \frac{R_F}{G} - 1 \right) \right) = G
\]
(A-6)

\[
\alpha \beta Z_i \left( 1 + \frac{R_F - G}{R_G} \right) = G \quad \text{solve for } \alpha \beta
\]
(A-7)

\[
\alpha \beta = \frac{G}{Z_i \left( 1 + \frac{R_F - G}{R_G} \right)}
\]
(A-8)

Using the expression for inverting \( Z_i \) (Equation 9, page 5):
\[
\frac{R_G}{1 + \frac{R_G}{R_4} + \alpha \beta} = Z_i
\]
(A-9)

Putting Equation A-2 and Equation A-8 into this calculation produces:
\[
\frac{R_G}{\frac{R_F}{G} + \frac{G}{Z_i \left( 1 + \frac{R_F - G}{R_G} \right)}} = Z_i
\]
(A-10)

We can now solve for \( R_G \) from Equation A-10.
From Equation A-10, multiply denominator through:

\[
R_G = Z_i \frac{R_F}{G} + \frac{G}{1 + \frac{R_F - G}{R_G}} = Z_i \frac{R_F}{G} + \frac{R_G}{R_G + R_F - G}
\]  
(A-11)

Multiply:

\[
(R_G + R_F - G)
\]  
(A-12)

through both sides:

\[
R_G(R_G + R_F - G) = R_G G + Z_i \frac{R_F}{G}(R_G + R_F - G)
\]  
(A-13)

Expand the terms:

\[
R_G^2 + R_G(R_F - G) = R_G G + R_G \left( \frac{Z_i R_F}{G} \right) + R_F^2 \frac{Z_i}{G} - Z_i R_F
\]  
(A-14)

Group the terms for a polynomial solution:

\[
R_G^2 + R_G \left( R_F - 2G - \frac{Z_i R_F}{G} \right) - \left( \frac{Z_i R_F^2}{G} - Z_i R_F \right) = 0
\]  
(A-15)

Taking the positive solution to the quadratic in \( R_G \):

\[
R_G = \frac{G - \frac{R_F}{2} \left( 1 - \frac{Z_i}{G} \right) + \sqrt{\left( G - \frac{R_F}{2} \left( 1 - \frac{Z_i}{G} \right) \right)^2 + Z_i R_F \left( \frac{R_F}{G} - 1 \right)}}{}
\]  
(A-16)

One constraint from Equation A-8 is that \( \alpha \beta \) must be < 1. Solve for Equation A-8 to equal 1:

\[
\frac{G}{Z_i \left( 1 + \frac{R_F - G}{R_G} \right)} = 1
\]  
(A-17)

\[
G = Z_i \left( 1 + \frac{R_F - G}{R_G} \right)
\]  
(A-18)

Isolate on \( G \):

\[
\frac{G}{Z_i} + \frac{G}{R_G} = 1 + \frac{R_F}{R_G}
\]  
(A-19)

\[
G \left( \frac{1}{Z_i} + \frac{1}{R_G} \right) = 1 + \frac{R_F}{R_G}
\]  
(A-20)

To get a solution:

\[
G < \left( 1 + \frac{R_F}{R_G} \right) \frac{R_G Z_i}{R_G + Z_i} = \frac{R_F + R_G}{1 + \frac{R_G}{Z_i}} = Z_i \left( \frac{R_F + R_G}{Z_i + R_G} \right)
\]  
(A-21)

To get larger \( G \), increase \( R_F \).
Appendix B  Design Spreadsheet (Example)

The bold numeric entries indicate where design targets need to be entered, while the green cells are computed values.

To use the spreadsheet, follow this procedure:

- Select the part number from the table on the part list sheet.
- Enter the gain for each DAC output (in Ω), the desired input impedance for each DAC, the desired feedback resistor value and then the ratio of $R_2 / R_1$.
- Select if the buffer gain loss should be considered.

All resistor values are then computed, and the total output noise (for the amplifier design only) is shown. Then, enter the closest standard resistor values and the actual design results will be re-computed.
## Appendix B

**DAC Complementary to single ended design spreadsheet.**

**MICHAEL STEFFES - MAY, 2005**

**Design Procedure and Assumptions:**
- Select Part Number (OBAM05)
- Must be as close as it appears in the first column of the Part Data

### Design Example:

**Desired single ended gain:** 5000

1. **Non-inverting input network** has too many R's for this condition - just need to set
   - Feedback resistor value
   - Set arbitrary ratio of 2xR1
   - The lower this is, the lower the total output noise will be.

### Now compute some intermediate computations

<table>
<thead>
<tr>
<th>Variable</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>ZIFF05</td>
<td>100050</td>
</tr>
</tbody>
</table>

### Do you want to account for CFB buffer gain loss across the input stage?

- **CMRR for the selected amplifier**
- **Compute buffer gain from CMRR if it is a CFB device:**

### Now set up the coefficients for the 2nd order Rg polynomial

<table>
<thead>
<tr>
<th>g0</th>
<th>g1</th>
<th>g2</th>
</tr>
</thead>
<tbody>
<tr>
<td>-70752</td>
<td>101</td>
<td>1</td>
</tr>
</tbody>
</table>

**Rg**

1. Solve the quadratic for Rg:
   - **Approximate maximum 0 given Rg, Rf: 5,533 ohms**

   **Use this to iterate up or down on 0 to get a solution with non-negative resistors**

### Now use this Rg value to continue solution

**Inverting input termination resistance R4:**

- **Non-inverting input termination R3, alpha:**
  - 0.771 Alpha - this yields no solution

**Then, non-inverting input termination R1:**

- **Then, with alpha set to 0.771:**

   **Remember:**
   - **Change up above if desired**

### Now go back and compute each others input 2 and gain to output gain

**On the non-inverting side -**

**SUMMARY DESIGN VALUES**

<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rf (ohms)</td>
<td>5000</td>
</tr>
<tr>
<td>Ra (ohms)</td>
<td>1000</td>
</tr>
<tr>
<td>RB (ohms)</td>
<td>36.1</td>
</tr>
<tr>
<td>R1 (ohms)</td>
<td>31.2</td>
</tr>
<tr>
<td>R2 (ohms)</td>
<td>220.0</td>
</tr>
<tr>
<td>RA (ohms)</td>
<td>402.0</td>
</tr>
</tbody>
</table>

**Noise terms for amplifier**

<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>ENC (mV)</td>
<td>100</td>
</tr>
<tr>
<td>ENC (mV)</td>
<td>100</td>
</tr>
<tr>
<td>ENC (mV)</td>
<td>100</td>
</tr>
<tr>
<td>ENC (mV)</td>
<td>100</td>
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<tr>
<td>ENC (mV)</td>
<td>100</td>
</tr>
<tr>
<td>ENC (mV)</td>
<td>100</td>
</tr>
</tbody>
</table>

**Solution for Rg becomes**

**ZIFF05: 5,533 ohms**

**Gain to Vo:**

- **50 ohms**

**On the inverting side:**

**ZIFF05:**

- **25 ohms**

**Gain to Vo:**

- **50 ohms**

**Enter**

**Exact Standard**

<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rf (ohms)</td>
<td>5000</td>
</tr>
<tr>
<td>Ra (ohms)</td>
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<td>RB (ohms)</td>
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<tr>
<td>R2 (ohms)</td>
<td>220.0</td>
</tr>
<tr>
<td>RA (ohms)</td>
<td>402.0</td>
</tr>
</tbody>
</table>

**Compensate for feedback resistor**

Then from B.5

**Rf = Z

ZIFF05**

**Also, get a solution**

**0 = \frac{R2 + Rf}{1 + \frac{Rg}{P}}**

---

**Figure B-1. Design Spreadsheet Example**
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<tr>
<th>Products</th>
<th>Applications</th>
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<tbody>
<tr>
<td>Amplifiers</td>
<td>Audio</td>
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<td>Data Converters</td>
<td>Automotive</td>
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<td>Broadband</td>
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<td>Interface</td>
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