1 Introduction

Texas Instruments' TLV320AIC33 (AIC33) audio device is a low-power, high-performance stereo input and stereo output coder/decoder (codec). This device is ideal for portable audio and telephony applications, in which an embedded operating system (OS), such as Windows CE (WinCE), often resides and operates. This application report discusses the I²C and I²S drivers, including the hardware connection between the TLV320AIC33EVM and the SC32442A Samsung application processor platform, the Windows CE 5.0 driver code and structure, and the respective installations.

2 Connections

The AIC33 device must be wired and connected to a host processor, where the device driver code is ported and executed. The two buses (or ports) for AIC33 operation are the control bus and the audio data bus. The control bus on the AIC33 is an I²C bus. The audio data streams through the I²S bus on the AIC33.
In developing the AIC33 drivers for this application, the TI AIC33EVM board and the Samsung platform with the SC32442A application processor (see Ref 4) were used.

On the \( ^{2}\text{C} \)-controlled AIC33, the seven digital signals that are essential for running the audio driver are:

- the \( ^{2}\text{C} \) bus, two wires: SCL and SDA (at J16 or J17 of the AIC33EVM board);
- the main audio codec clock, MCLK (at J17 of AIC33EVM board); and
- the \( ^{2}\text{S} \) bus, four wires: BCLK, WCLK, SDIN and SDOUT (at J17 of AIC33EVM board).

Figure 1 shows the wires and connections between the AIC33 and SMDK2442 processor for the \( ^{2}\text{C} \) control interface.

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**Figure 1. TLV320AIC33 Connections to Samsung SC32440A Processor**

To implement the connection shown in Figure 1, ensure that these jumpers are correctly connected on the AIC33EVM board:

- Connect JMP10 between 2 and 3
- Connect JMP3 and JMP4 between 1 and 2
- Connect JMP9 between 1 and 2
- Connect JMP1 between 1 and 2
- Ensure that JMP11, JMP13, JMP14, and JMP15 are open
- Connect JMP12
This jumper configuration enables the internal MIC for recording and the HEADSET JACK for playing data from the codec.

The wiring diagram in Figure 2 describes the wiring details between the SMDK2442 interface and the AIC33.

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**Figure 2. TLV320AIC33EVM Connections to Samsung SMDK2440X Module**

See the TLV320AIC33EVM User's Guide (SBAU114, available for download at www.ti.com) for the schematic and other details of the EVM board. In Figure 2, the AIC33 is reset from two sources: RSTOUT and via a General Purpose Input/Output (GPIO) pin. Resetting from RSTOUT resets the AIC33 when the Samsung SMDK2442 processor powers on, putting the AIC33 into a known state. A reset via the GPIO Port B 2 pin is a response to a host processor instruction. Software can issue an active low pulse longer than 10ns in duration on this port pin to reset the AIC33. By setting JMP9 as directed, we are setting up the board to use the GPIO reset.
3 Device Driver

Figure 3 illustrates the locations of the AIC33 audio device driver files for both the SPI and I²C control interfaces. The files starting with Host... are the processor-dependent code or PDL, such as HostAudio.C or HostI2CComm.H.

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3.1 I²C Interface

The two AIC33 I²C bus pins, SCL and SDA, are connected to the GPIO Port E 14 and GPIO Port E 15 of the SMDK2442 processor, respectively. On the host side, the SMDK2442 GPIO, I²C, and clock management control registers are used to set up the I²C interface to communicate with the AIC33 via the I²C interface. The HWInitI2C() routine implements this set-up.

```c
BOOL HWInitI2C(BOOL InPowerHandle)
{
    UINT8 reg = 0x00;
    RETAILMSG(1, (TEXT("Setup Host GPIO & I2C for an I2C Interface...

// init I2C control register (disabled I2C unit)
// enable I2C unit clock (the clock should be enabled first)
g_pClockRegs->CLKCON |= S3C_CLKEN_I2C;
// set up GPE
g_pGPIORegs->GPEDN |= GPE_DN; //0xc000, Pull-up
disable

g_pGPIORegs->GPECON |= (GPE14_IIC_SCL | GPE15_IIC_SDA); //Making GPE15=>IICSDA
GPE14=>IICSCL
//Enable ACK, Prescaler IICCLK=PCLK/16, Enable interrupt, Transmit clock value Tx
clock=IICCLK/16
//e.g. If PCLK 50.7MHz, IICCLK = 3.17MHz, Tx Clock = 0.198MHz
reg = ICR_ACK | ICR_INTR;
reg &= ~(ICR_TXCLK);
reg |= ICR_TXCLKVAL;
g_pI2CRegs->IICCON = reg;
g_pI2CRegs->IICADD = 0x10; //2442 slave address
[7:1]
```
Two other important I²C interface routines are the `HWI2CWriteRegs()` and `HWI2CReadRegs()`. These routines allow the SMDFK2442 to write to or read from AIC33 control registers using the I²C bus. The I²C write and read protocols have been defined (see Figure 5 and Figure 6 of the TLV320AIC33 data sheet).

**HWI2CWriteRegs():**

```c
/////
// Function: HWI2CWriteRegs Routine
// Purpose: This routine allows the SMDFK2442 to write to AIC33
// control register(s) using I2C bus.
// Note: The first byte in bytesBuf is the starting address
// for writing; and the 2nd and on are bytes/contents
// writing to AIC33
/////
BOOL HWI2CWriteRegs(UINT8 *bytesBuf, int bytesCount, BOOL InPowerHandle)
{
  if (!InPowerHandle)
  {
    UINT8 reg;
    IicMod = WR_DATA;
    iicPtr = 0;
    iicDat[0] = *bytesBuf++; //Putting 1st byte i.e
    register address
    iicDat[1] = *bytesBuf; //Putting 2nd byte i.e.
    actual data
    iicDCount = bytesCount;
    g_pI2CRegs->IICDS = I2C_WRITE; //Putting AIC33 slave
    address (7bit address + 0 'write bit')
    reg = g_pI2CRegs->IICSTAT;
    reg = (ISR_MTX | ISR_START | ISR_ENOP); //Master transmit mode, START
    signal genration, Enable output
    g_pI2CRegs->IICSTAT = reg;
    /*Clearing the pending bit isn't needed because the pending bit has been
    cleared*/
    while(iicDCount != -1)
      Run_Iic_Poll();
    IicMod = POLL_ACK;
    while(1)
    {
      g_pI2CRegs->IICDS = I2C_WRITE;
      iicStat = 0x100;
      reg = g_pI2CRegs->IICSTAT;
      reg = (ISR_MTX | ISR_START | ISR_ENOP);
      //Master transmit mode, START signal genration, Enable output
      g_pI2CRegs->IICSTAT = reg;
      reg = g_pI2CRegs->IICCn;
      reg = ICR_ACK | ICR_INTR | ICR_TXCLKVAL; reg &= ~ICR_PENITR);
      //Resumes IIC operation.
      g_pI2CRegs->IICCn = reg;
      while(iicStat==0x100)
        Run_Iic_Poll();
      if(!iicStat & 0x1)
        break;
      //When ACK is received
  }
```
Device Driver

```c
DeviceDriver::HWI2CReadRegs():

    // Function: HWI2CReadRegs Routine
    // Purpose: This routine allows the SMDK2442 to read from AIC33
    // control register(s) using I2C bus.
    // Note: The first byte in bytesBuf is the starting address for
    // reading; and the 2nd and on are values reading from AIC33

    BOOL HWI2CReadRegs(UINT8 *bytesBuf, INT bytesCount, BOOL InPowerHandle)
    {
        if (!InPowerHandle)
        {
            UINT8 reg;
            iicMod = SETRD_ADDR;
            iicPtr = 0;
            iicDat[0] = *bytesBuf++;
            g_pI2CRegs->IICDS = I2C_WRITE;
            g_pI2CRegs->IICSTAT = ~(ISR_STOP);
            reg = g_pI2CRegs->IICCON;
            reg &= ~(ICR_PENITR);
            g_pI2CRegs->IICSTAT = reg;
            Delay(3);
            // Wait until stop condition is in effect.
            /*Write is completed.*/
            return(TRUE);
        }
        else
        {
            RETAILMSG(1, (TEXT("HW Tx Error...
                          
")));
            return(FALSE);
        }
    }
```
3.2 Audio Driver

From a hardware standpoint, the AIC33 audio driver must have both I²C and I²S buses (for audio control and audio data streaming, respectively). The I²C bus controls the audio codec operation by writing to the AIC33 audio control registers; the I²S bus transfers audio data between the host and the AIC33.

Additionally, the AIC33 MCLK pin should receive an external clock that provides the necessary timing for the AIC33 audio delta-sigma (ΔΣ) ADC and DAC to operate. MCLK to the AIC33 should be generated from the same source as the I²S clocks; that is, MCLK should also run from the host processor, which is the I²S master as described in this application report. The AIC33 audio driver was built on the standard audio driver, WaveDev, and is located in the directory AIC3xWaveDev.

On the host side, the SMDK2442 GPIO GPE0 to GPE4 pins were used as the I²S source, and connected to the AIC33 WCLK, BCLK, MCLK, SDIN and SDOUT pins respectively (see Figure 1). The GPIO pin GPE2 is programmed as the I²S SYSCLK and is connected to MCLK, which is programmed to generate a 16.9344MHz clock. The I²S setup was implemented at the routine, HWEnableI2S().

HWEnableI2S():

//
// Processor Related Routines Used at AudioPowerOn() and
// AudioPowerOff(),
// which include: PDD_AudioInitialize(),
// PDD_AudioDeinitialize()
// and PDD_AudioPowerHandler().
// -------------------------------------------------------------
//
// Function: HWEnableI2S()
//MMMM void HWEnableI2S(void)
//
// RETAILMSG(1, (TEXT("+++HWEnableI2S\n")));
// RETAILMSG(1, (TEXT("Setup Host GPIO & I2S Interface... \r\n")));
// /* Basic Outline: */
// /* Configure the GPIO registers and set to I2S mode */
// /* Set up I2S control registers at default condition */
// /* Enable the CPU clock to the IIS controller */
// v_pClockRegs->CLKCON |= IIS_INTERNAL_CLOCK_ENABLE;
// /* Set up GPIO to route I2S signals */
// //GPE4 - I2SSDO
// //GPE3 - I2SSDI
// //GPE2 - CCLK
// //GPE1 - I2SSCLK
// //GPE0 - I2SLRCK
// v_pGPIORegs->GPEDN |= 0x1f; //Disable
// v_pGPIORegs->GPECN |= 0x2aa; //Select I2S
// /* configure IIS registers */
// //IISCON : Tx DMA REQ Enbl
// //Rx DMA REQ Enbl
// Enable IIS Prescaler
// Disable IIS interface (stop)
// v_pI2SRegs->IISCON = RECEIVE_DMA_REQUEST_ENABLE
// TRANSMIT_DMA_REQUEST_ENABLE

The codec can be used according to given application environments. As an example, for this application report, the AIC33 was initially configured in this manner:

- **I²S interface:**
  1. The I²S interface is at 16 bits, standard I²S mode, with 44.1kHz ADC and DAC sample rates.
  2. The AIC33 is the slave because the host is the I²S master (the AIC33 can be I²S slave or master, but SMDK2442 can only be the master).

- **Audio input circuitry:**
  1. The left and right ADC input are from the stereo, single-ended LINE3 (MICIN3).
  2. ADC input gain is controlled by its PGA, with an initial gain setting of 0dB gain.

- **Audio output circuitry:**
  1. The left and right DAC outputs are routed to the stereo, single-ended headphone, HPL/R with HPLCOM and HPRCOM being shorted as the VCOM.
  2. Headphone output is in the CAPLESS mode.
  3. DAC gains and HPL/R output gains are all initialized to 0dB.

- **Other functions:**
  1. The input high-pass filter has not been enabled.
  2. The output digital boost, emphasis, and 3-D functions have not been enabled.
  3. PLL is disabled.
  4. The pop-reduction function is set to slowest rate and is enabled.
All AIC33 audio control registers (in Page0 of the AIC33 memory space) were set up or initialized, as previously stated, with the routine \texttt{InitAIC33Audio()} and called by the audio PDD routine, \texttt{PDD\_AudioInitialize()}. The audio initialization routine is given below.

\section*{Audio Initialization Routine:}

```c
// Audio Initialization
//--------------------------------------------------------------
// Initialize AIC33 Audio Register at Default
void InitAIC33Audio(BOOL bInPowerHandler)
{
  /*The register which are not used in AIC33 are commentet out*/
  RETAILMSG1(1, (TEXT("InitAIC33Audio.

  // init for digital functions
  AIC33WriteReg(AIC33\_RATE, RATE\_INIT\_VALUE, bInPowerHandler);
  AIC33WriteReg(AIC33\_PLLa, PLLa\_INIT\_VALUE, bInPowerHandler);
  AIC33WriteReg(AIC33\_PLLb, PLLb\_INIT\_VALUE, bInPowerHandler);
  AIC33WriteReg(AIC33\_PLLc, PLLc\_INIT\_VALUE, bInPowerHandler);
  AIC33WriteReg(AIC33\_PLLd, PLLd\_INIT\_VALUE, bInPowerHandler);
  AIC33WriteReg(AIC33\_DATAPATH, DATAPATH\_INIT\_VALUE, bInPowerHandler);
  AIC33WriteReg(AIC33\_INTERFa, INTERFa\_INIT\_VALUE, bInPowerHandler);
  AIC33WriteReg(AIC33\_INTERFb, INTERFb\_INIT\_VALUE, bInPowerHandler);
  AIC33WriteReg(AIC33\_INTERFc, INTERFc\_INIT\_VALUE, bInPowerHandler);
  AIC33WriteReg(AIC33\_DIGFILT, DIGFILT\_INIT\_VALUE, bInPowerHandler);
  AIC33WriteReg(AIC33\_HEDETb, HEDETb\_INIT\_VALUE, bInPowerHandler);
  // init for analog input functions
  AIC33WriteReg(AIC33\_ADC\_GAL, ADCGAL\_INIT\_VALUE, bInPowerHandler);
  AIC33WriteReg(AIC33\_ADC\_GAR, ADCGAR\_INIT\_VALUE, bInPowerHandler);
  AIC33WriteReg(AIC33\_MIC3\_ADCL, MIC3\_ADCL\_INIT\_VALUE, bInPowerHandler);
  AIC33WriteReg(AIC33\_MIC3\_ADCR, MIC3\_ADCR\_INIT\_VALUE, bInPowerHandler);
  AIC33WriteReg(AIC33\_MIC\_BIAS, MIC\_BIAS\_INIT\_VALUE, bInPowerHandler);
  // init for analog output functions
  AIC33WriteReg(AIC33\_OUTPWR, OUTPWR\_INIT\_VALUE, bInPowerHandler);
  AIC33WriteReg(AIC33\_OUT\_DRIVE, OUT\_DRIVE\_INIT\_VALUE, bInPowerHandler);
  AIC33WriteReg(AIC33\_OUTSTAGE, OUTSTAGE\_INIT\_VALUE, bInPowerHandler);
  AIC33WriteReg(AIC33\_OUT\_POP, OUT\_POP\_INIT\_VALUE, bInPowerHandler);
  AIC33WriteReg(AIC33\_DAC\_GAIN, DACGAIN\_INIT\_VALUE, bInPowerHandler);
  AIC33WriteReg(AIC33\_DAC\_R\_GAIN, DACR\_GAIN\_INIT\_VALUE, bInPowerHandler);
  AIC33WriteReg(AIC33\_DAC\_H\_PL, DAC\_H\_PL\_INIT\_VALUE, bInPowerHandler);
  AIC33WriteReg(AIC33\_H\_PL\_LEVEL, H\_PL\_LEVEL\_INIT\_VALUE, bInPowerHandler);
  AIC33WriteReg(AIC33\_DAC\_R\_H\_PR, DAC\_R\_H\_PR\_INIT\_VALUE, bInPowerHandler);
  AIC33WriteReg(AIC33\_H\_PR\_LEVEL, H\_PR\_LEVEL\_INIT\_VALUE, bInPowerHandler);
  AIC33WriteReg(AIC33\_PW\_STATUS, PW\_STATUS\_H\_PRO\_PW\_UP, bInPowerHandler);
  AIC33WriteReg(AIC33\_CLK\_GEN, CLK\_GEN\_INIT\_VALUE, bInPowerHandler);
  RETAILMSG1(1, (TEXT("Done InitAIC33Audio.

```
Installation

4 Installation

This section presents the installation steps for running the AIC33 WinCE 5.0 drivers on an SMDK2442 platform. The SC32442 Application Processor board support package (BSP) can be obtained from Samsung and installed on a PC. It is recommended to load the BSP after installing the Platform Builder 5.0 at (for example) C:\WinCE500\PLATFORM. To install the AIC33 Windows CE 5.0 audio driver into one of the SMDK2442 workspaces, perform the following steps.

Step 1. Copy:

a. Copy the file \AIC33WinCE5Driver\AIC33.cec to this location: C:\WINCE500\PUBLIC\COMMON\OAK\CATALOG\CEC\n
b. Copy all files inside \AIC33WinCE5Drivers\INC\ into:
C:\WINCE500\PLATFORM\SMDK2442\SRC\INC\n
c. Copy the file \AIC33WinCE5Driver\intr.c into:
C:\WINCE500\PLATFORM\SMDK2442\Src\Common\Intr\n
d. Copy the file \AIC33WinCE5Driver\s3c2440a_intr.h into:
C:\WINCE500\PLATFORM\SMDK2442\Src\Inc\n
e. Copy the directories AIC33LIB and AIC33WaveDev into:
C:\WINCE500\PLATFORM\SMDK2442\SRC\DRIVERS\n
Step 2. Set Up:

a. Run Platform Builder 5.0, and the Platform Builder IDE appears.
b. At the Platform Builder 5.0 IDE, open Manage Catalog Items from the menu File\Manage Catalog Items …\. When the Manage Catalog Items window appears, click the Import button on the right side of the window; navigate, find, and select AIC33.cec in the directory C:\WINCE500\PUBLIC\COMMON\OAK\CATALOG\CEC\ Then click on Open so that the item is ported in.
c. Click and drag to select all *.cec files in the Manage Catalog Items window. Then click on the Refresh button to make sure the new item is loaded.
d. Close the Manage Catalog Items window by clicking OK.

This step sets up the catalog to include the AIC33 device drivers.

Step 3. Open:

This step, in the Platform Builder 5.0 IDE, opens a new or existing SMDK2442 workspace according to the application instructions. This procedure is ignored here.

Step 4. Add:

a. In the Catalog window of the Platform Builder 5.0 IDE, find the TI AIC33 Audio CODEC Driver, right-click on it, and select Add to OS Design to add the audio driver to the OS.
b. The audio device driver should appear under the Device Drivers section at the OSDesignView window of the WorkSpace.

This step ports the AIC33 device drivers from the Catalog into the existing OS design.
5. Modify:

a. Open the dirs file in the directory:
   C:\WINCE500\PLATFORM\SMDK2442\SRC\DRIVERS\n
b. Add the AIC3xLIB and AIC3xWAVEDEV.
   For example, the dirs file could be:

   DIRS=\ceddk\keybd\PowerButton\pccard\serial\usb\nleddrvr\Battldrvr\Backlight\cs8900\Display\SDHC\touch\wavedev\AIC33LIB\AIC33WAVEDEV

   This step modifies the building device drivers in order to include TI AIC33 drivers.

Step 5. Update:

a. Open the existing platform.reg file from Hardware Specific section of the ParameterView window of the workspace.

b. Edit the platform.reg file; delete the old audio .dll and add in the AIC33 audio dll file:

   IF BSP_NOAUDIO !
     ; @CESYSGEN IF CE_MODULES_WAVEAPI
     [HKEY_LOCAL_MACHINE\Drivers\BuiltIn\Audio]
     "Prefix"="WAV"
     "Dll"="wavedev.dll"
     "Index"=dword:1
     "Order"=dword:0
     "Priority256"=dword:d2
     ; @CESYSGEN ENDIF CE_MODULES_WAVEAPI
   ENDIF BSP_NOAUDIO !
   c. Save and close the updated platform.reg file.

d. Edit the platform.bib file in the same manner:

   ;-------------------------------------------------------------------------------
   ; @CESYSGEN IF CE_MODULES_WAVEAPI
   IF BSP_NOAUDIO !
   wavedev.dll $(\_FLATRELEASEDIR)\wavedev.dll NK SH
   ENDIF BSP_NOAUDIO !
   ; @CESYSGEN ENDIF CE_MODULES_WAVEAPI
   ;-------------------------------------------------------------------------------
   e. Save and close the updated platform.bib file.

   This step updates the Hardware Specific Files, so that the operating system will use AIC33 device drivers.

5 WinCE 5.0 Driver Code

To obtain the driver code discussed in this application report, contact the TI Applications Support Group at: support@ti.com.
6 References

The following documents are available for download through the Texas Instruments web site (www.ti.com), except where noted.

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