Inverting circuit for high-to-low voltage level translation to drive ADC

Art Kay

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<tr>
<th>Input</th>
<th>ADC Input</th>
<th>Digital Output ADS8860</th>
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<tbody>
<tr>
<td>−10V</td>
<td>0.1V</td>
<td>0889, or 2185,</td>
</tr>
<tr>
<td>+10V</td>
<td>2.9V</td>
<td>F777, or 63351,</td>
</tr>
</tbody>
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<table>
<thead>
<tr>
<th>Power Supplies</th>
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<tbody>
<tr>
<td>Vref1</td>
</tr>
<tr>
<td>1V</td>
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</table>

**Design Description**

This circuit document describes how to translate a high-voltage signal (for example, ±10V) to low-voltage ADC inputs (for example, 0V to 3V). This circuit does not require any high-voltage supply to operate, but rather uses a voltage divider and level shift to translate the input signal. This circuit shows the OPA365 and ADS8860 devices, but the topology could be applied to many different ADCs. This design can be used a wide range of applications where a high-voltage input needs to be translated such as analog input modules for PLCs, instrumentation (lab, analytical, field and portable), and factory automation and control.
Specifications

<table>
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<th>Calculated</th>
<th>Simulated</th>
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<tr>
<td>Sampling rate</td>
<td>1MSPS (max sampling rate)</td>
<td></td>
<td>800kSPS</td>
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<tr>
<td>Bandwidth</td>
<td>&gt; 1MHz</td>
<td>Poles at 3.39MHz and 4.92MHz</td>
<td>2.44MHz</td>
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<tr>
<td>Noise</td>
<td>&lt; 1/2 LSB = 38.1µV</td>
<td>29.52µV</td>
<td>31.55µV</td>
</tr>
<tr>
<td>Transient settling error</td>
<td>&lt; 1/2 LSB = 38.1µV</td>
<td></td>
<td>–2.2µV</td>
</tr>
</tbody>
</table>

Design Notes

1. The common mode of this circuit is kept at a constant value (Vref1 = 1V in this example). Because the common mode is constant, the amplifier does not need to have a rail-to-rail input or zero crossover distortion. See the TI Precision Labs *Determining a SAR ADC’s Linear Range when using Operational Amplifiers* video for more details.
2. Select a C0G type capacitor for Cfilt to minimize distortion.
3. Use 0.1% 20ppm / °C film resistors, or better, to minimize gain error and drift.
4. The input impedance of this circuit is Rin = Ri (71.5Ω, in this example). For a high-impedance input, use a high-voltage amplifier buffer (for example, Vcc = +15V, and Vee = –15V). Alternatively, the input impedance could be increased by multiplying Rn, Rx, and Rf by the same factor. However, increasing the resistance on all the resistors will impact system noise.
5. The TI Precision Labs - ADCs video series covers methods for selecting the charge bucket circuit, Cfilt and Rfilt. See the Introduction to SAR ADC Front-End Component Selection video for details on this subject. In this example, the sampling rate was reduced from 1MSPS to 800kSPS, to improve settling.
Component Selection

1. First select the amplifier input and output range. In this example, the input range is –10V to +10V. The amplifier output range is set according to the ADC input and the amplifier linear output range. The ADC input range in this example is set by the reference voltage and is 3V. The amplifier supply is set to 3V to match the ADC input range. The output of the amplifier cannot swing to the power supply rails because of output swing limitations (that is, the linear range for the OPA365 device is 0.1V < \( V_{OUT} < 2.9V \)). The output range can be adjusted further to provide design margin. For example, 0.2V < \( V_{OUT} < 2.8V \), provides margin for issues like power-supply variation.

2. The Analog Engineer’s Calculator can be used in the next step to select component values. Enter the input and output voltages and reference voltage (–10V < \( V_{IN} < +10V \), and 0.1V < \( V_{OUT} < 2.9V \)). The range of acceptable reference voltages is given at the bottom of the tool (0.12V to 1.22V in this example). In this example, the reference is selected to be 1V. The tool outputs the 0.1% resistors required to map the voltages (\( R_i = 71.5k\Omega \), \( R_x = 27.7k\Omega \), \( R_f = 10k\Omega \)).

3. The following equations show the transfer function for the inverting level-shift topology. It is possible to use these equations to solve for the different component values rather than the calculator. To do this, choose a reference value and fix the value of \( R_f \) to 10k\( \Omega \). Once done, solve for \( R_i \) and \( R_x \) for two different values of output signal. The algebra for this problem is a little complex, so using the calculator is the suggested method. Use the following equations to verify the transfer function:

\[
V_O = \frac{R_f}{R_i} \cdot V_{IN} + \left(1 + \frac{R_f}{R_i \parallel R_x}\right) \cdot V_{ref}
\]

where

\[
R_i \parallel R_x = \frac{R_i \cdot R_x}{R_i + R_x}
\]

Using the values from the calculator:

\( R_i = 71.5k\Omega \), \( R_x = 27.7k\Omega \), \( R_f = 10k\Omega \), \( V_{ref} = 1.0V \)

\( V_O(-10V) = 0.13999V \cdot V_{IN} + 1.5009V \)

\( V_O(+10V) = 2.8995V \)

\( V_f(+10V) = 0.0123V \)

4. Find \( R_{filt} \) and \( C_{filt} \) to allow for settling at 1MSPS. The Refine the \( R_{filt} \) and \( C_{filt} \) Values video shows the algorithm for selecting \( R_{filt} \) and \( C_{filt} \). The final value of 24.9\( \Omega \) and 1.1\( \mu \)F proved to settle to well below \( \frac{1}{2} \) of a least significant bit (LSB).
**DC Transfer Characteristics**

The following graph shows the linear output response for a –10-V to 10-V input. In this case, the amplifier output is approximately 2.9V for a –10-V input and 0.1V for a +10-V input. This design was scaled so that the output range avoids the nonlinear power supply rails by 0.1V. See the *Determining a SAR ADC's Linear Range when using Operational Amplifiers* video for detailed theory on this subject.

Vin = -10.0V
Vout = 2.89943V
Vin = 10.0V
Vout = 0.10223V

**AC Transfer Characteristics**

The bandwidth is limited by the Cf • Rf filter ($f_{c1} = 3.39$MHz) and the output filter ($f_{c2} = 4.92$MHz). These two poles combine to form a second-order filter with a simulated cutoff frequency at 2.44MHz. See the *Op Amps Bandwidth* video series for more details on this subject.

\[
\begin{align*}
    f_{c1} &= \frac{1}{2\pi \cdot (10k\Omega) \cdot (4.7pF)} = 3.39$MHz from the filter in the feedback network \\
    f_{c2} &= \frac{1}{2\pi \cdot (2 \cdot 29.4\Omega) \cdot (1.1nF)} = 4.92$MHz from the output filter
\end{align*}
\]
Transient ADC Input Settling Simulation

The following simulation shows settling to a −10-V DC input signal. This type of simulation shows that the sample and hold kickback filter is properly selected. See the Final SAR ADC Drive Simulations video for detailed theory on this subject. Note: in this example the amplifier had settling issues, so the sampling rate was decreased from 1MSPS to 800kSPS. Reducing the sampling rate increases the acquisition period to improve settling (t_{acq} = 1 / f_{samp} − t_{conv} = (1/800kSPS) − 710ns = 540ns).

Noise Simulation

The following noise calculation takes into account the thermal noise of the resistor network, the amplifier noise, and the bandwidth limit from the filters. The calculated total noise is 29.52μV and the simulated total noise is 31.55μV. See the Op Amp Noise Calculation video for detailed theory on amplifier noise calculations, and the Calculating the Total Noise for ADC Systems video for data converter noise.

Noise equivalent input resistor network:

\[ R_{eq} = \frac{1}{R_i + \frac{1}{R_x} + \frac{1}{R_f}} = \frac{1}{71.5 \, \text{kΩ} + \frac{1}{27.7 \, \text{kΩ}} + \frac{1}{10 \, \text{kΩ}}} = 6.67 \, \text{kΩ} \]

Resistor network noise:

\[ e_{nReq} = \sqrt{4kTR} = \sqrt{4 \cdot (1.381 \cdot 10^{-23}) \cdot (273 + 25) \cdot 6.67 \, \text{kΩ}} = 10.48 \, \text{nV/√Hz} \]

OPS365 noise density:

\[ e_{nOPA365} = 4.5 \, \text{nV/√Hz} \]

Noise gain:

\[ G_n = \frac{R_f}{R_i || R_x} + 1 = \frac{10 \, \text{kΩ}}{(71.5 \, \text{kΩ}) || (27.7 \, \text{kΩ})} + 1 = 1.501 \]

Total noise:

\[ e_{nTOT} = G_n \cdot \sqrt{e_{nOPA365}^2 + e_{nReq}^2} \cdot \sqrt{K_n \cdot f_c} \]

\[ e_{nTOT} = (1.501) \sqrt{(4.5 \, \text{nV/√Hz})^2 + (10.48 \, \text{nV/√Hz})^2} \cdot \sqrt{1.22 \cdot 2.44 \, \text{MHz}} = 29.52 \, \text{μV} \]
Design Featured Devices and Alternative Parts

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<th>Key Features</th>
<th>Link</th>
<th>Other Possible Devices</th>
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Link to Key Files


References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.
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