Burr-Brown Products from Texas Instruments
APPLICATION BULLETIN

Ultrasound Processor Supplementary Material

By Mike Koen

Ultrasound diagnostic equipment is being utilized for medical analysis at an ever increasing rate. Ultrasound equipment is taking it's place along side other established technologies such as X-Ray, CAT Scan, and MRI for medical diagnosis. Relative to these other means of analysis, it is safer and less expensive. Additionally, it is the technology of choice in areas such as obstetrics and cardiology. An ultrasound system employs a multichannel phased array of acoustic elements to form an image. An ultrasound probe with as many as 512 pizeo-electric elements is excited by a high-voltage impulse. The high-voltage impulse is typically a shaped burst of 3 to 50 cycles at a frequency from 3MHz to 20MHz with an amplitude of ±200V. The pizeo-electric crystal converts the electric energy of the impulse to acoustic energy that is applied to the patient through the probe. The acoustic energy enters the body and is then reflected from an object within the body, such as a fetus or a blood vessel. The reflected acoustic energy is then converted back to an electric signal by the same pizeo-electric crystal that was initially energized by the impulse. The dynamic range of the return signal is very large—approaching 120dB. Solid objects just below the skin, such as bones, reflect very large signals, while objects located near the back of the body are reflected with a large amount of attenuation. It then becomes necessary to amplify the return signal by varying amounts to keep within the dynamic capability of the analog-to-digital converter. The reflected acoustic signal experiences a $1/r^2$ attenuation response. To properly process the signal, it becomes necessary to alter the gain inversely to the way that the return signal is attenuated. Initially, the gain is set low and is then swept to increase the gain with a characteristic that is linear in dB with the control voltage. The output of this variable gain amplifier is then applied to filters and data converters for further processing by DSP techniques. The development described herein advances the state of the art, due to the use of CMOS technology, to achieve the necessary performance. Previous implementation of this function has used bipolar technology [1]. 0.5µ CMOS technology has the advantage of lowering the cost and increasing functionality compared to using bipolar technology.

There are many demanding requirements for this variable gain amplifier and among them are:

1. To achieve adequate spatial resolution, many channels are required. Due to this factor, it is necessary to achieve low cost. 0.5µ CMOS was used, as this technology can achieve high performance at moderate cost.
2. Low power is an important consideration due to the number of channels and the need for simple packaging and board layout. Excessive power dissipation also complicates the installation of the final system.
3. Programming flexibility for differing system specifications require different gain and gain ranges.
4. To achieve optimum signal-to-noise ratio and proper frequency response, it is necessary to terminate the probes in a simple, but low-noise fashion.
5. Due to the large dynamic-range requirements, it is necessary to have excellent overload-recovery capability to prevent large signals from suppressing nearby small signals.

Table I summarizes the performance of the voltage controlled amplifier.

Bandwidth	50MHz
Maximum Overall Gain	71dB
Minimum Overall Gain	6dB
Maximum Gain Control Range	0dB to 45dB
Minimum Gain Control Range	0dB to 24dB
LNA Gain Adjust Range	6dB to 26dB
Noise	$0.7nV/\sqrt{Hz}$
Supply Voltage	5V
Power Dissipation	450mW

TABLE I. Performance of the Voltage Control Amplifier.

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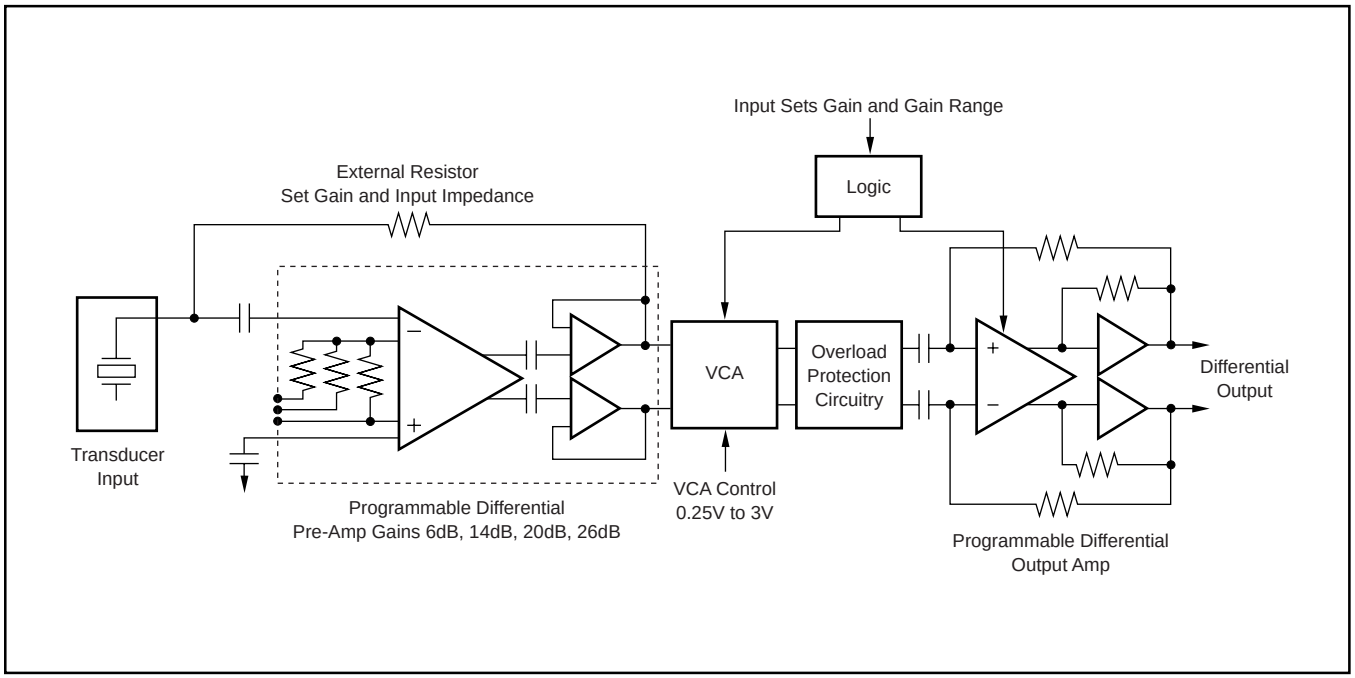


FIGURE 1. Block Diagram of Ultrasound Processor.

Figure 1 shows a block diagram of the ultra-sound processor. The ultra-sound signal is first amplified by a low-noise amplifier that employ's feedback to achieve a low-noise signal termination. The low-noise amplifier converts the single-ended input signal to a differential signal. A differential signal has the advantage of reducing second-harmonic distortion and converting substrate and power-supply effects to common-mode noise. The low-noise preamplifier has low-impedance buffered outputs for driving the succeeding voltage-controlled attenuator. The low-noise preamplifier employs very-low resistance local feedback to achieve stable, low-distortion, low-noise gain.

The voltage-controlled attenuator takes the differential output from the low-noise amplifier where the attenuation is programmed by an external control voltage. For flexibility, the maximum attenuation is programmable. The attenuator reduces the signal by continuously adjusting the value of a shunt FET, operated as a variable resistor, with a control voltage. The value of maximum attenuation can be further adjusted by controlling the size of the shunt FET. An array of FETs is grouped together and programmed so that an effective FET of varying sizes can be created under logic control.

The differential output from the attenuator is amplified by a programmable post amplifier. The post amplifier is programmable by the same logic that programs the voltage-controlled attenuator. The combination of the amplifier and attenuator yields a swept amplified characteristic where the gain varies from 0dB to X gain where the peak gain X is programmable. Figure 2 which shows a diagram of this characteristic.

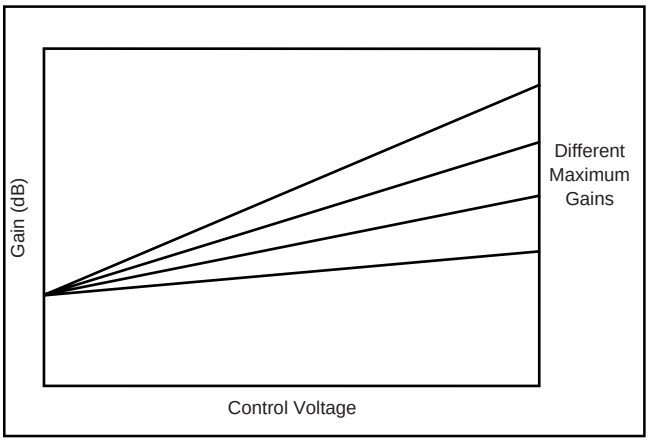


FIGURE 2.

In between the attenuator and the post amplifier is circuitry that enables the amplifier output to provide a clean output when the input is exceedingly large and could severely overload the post amplifier. The attenuator is initially set to maximum attenuation as the signal input is maximum at the beginning of a sweep. As time progresses the effective gain of the signal chain increases and there are times when the gain is high enough so that the signal return would cause overload effects that would prevent the detection of weak nearby signals. A comparator senses a signal level that would cause the post amplifier to overload and inserts a DC level at the input that prevents undesirable overload effects with the post amplifier. See Figure 3 for a die photograph of the dual ultrasound processor.

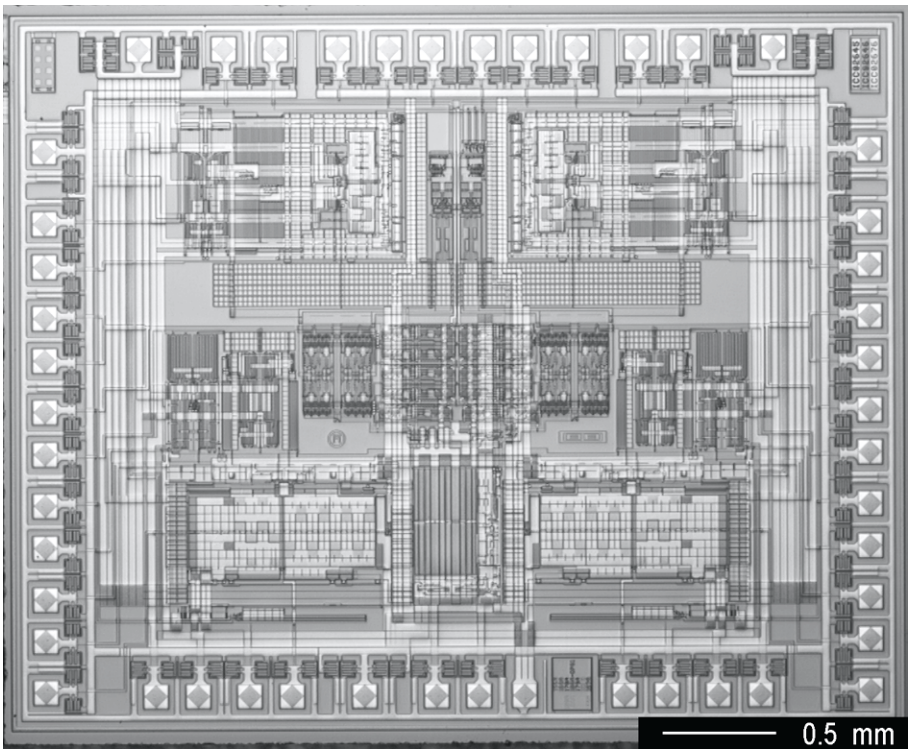


Figure 3. Die Photograph of Dual Ultra-Sound Processor.

LOW NOISE PREAMPLIFIER

One of the requirements of the low-noise preamplifier is to achieve a low-noise figure along with being able to terminate the input in a low-noise manner. The amplifier should be flexible and be easily programmed to handle a variety of probe impedances and gain requirements. The chosen amplifier architecture uses feedback to achieve a lower-noise means of terminating a cable as compared to the conventional termination method. Appendix I shows an analysis of the noise figure improvement.

One of the most straight-forward ways to design a low-noise amplifier is to use a source coupled pair. This architecture achieves low noise by virtue of the fact that the sources are directly coupled together. The draw back of this circuit is with both the signal-handling capability and the gain stability. Both are limited due to the open-loop nature of the input stage. A common way to correct the problem of the variability of gm is to insert a resistor between the two sources. This solution improves the linearity of the stage, but it does so at the expense of noise performance. If the resistor is made large to improve the linearity, it will generate excessive noise. Another method that can be employed to improve linearity is to use feedback instead of just allowing the source resistor to become larger. Figure 4 shows a block diagram of this circuit.

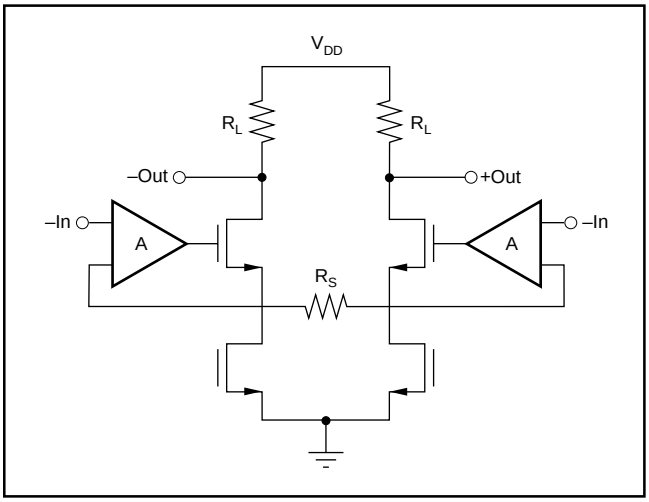


FIGURE 4.

The differential gain of this amplifier is given by the expression:

$$\text{Gain} = \frac{A gm\, R_S}{1 + gm\, R_S + A gm\, R_S} \frac{R_L}{R_S} \qquad (1)$$

Since A>>1, the gain is then given by the expression:

$$\text{Gain} = \frac{R_L}{R_S} \qquad (2)$$

Figure 5 shows a schematic of the low-noise preamplifier. The preamplifier has differential input and output capability. This circuit employs low-resistance local feedback to achieve stable low-noise, low-distortion performance with a very high input impedance. High current in the input stage is required for low-noise operation and to achieve low distortion in both the input and output stages. Conventional circuits have separate input and output stages. The difference between the signal on the gate and source of Q_4 is amplified by Q_2 and Q_4. Q_1, Q_2, Q_4, and Q_5 form amplifier A (see Figure 3). Devices Q_6 through Q_{10} play the same role for signals present on –IN. The power dissipation of this circuit is minimized as the same bias current flows through both the input device, Q_4 and the output device, Q_3. The gain is user programmable by selecting the value of R_S.

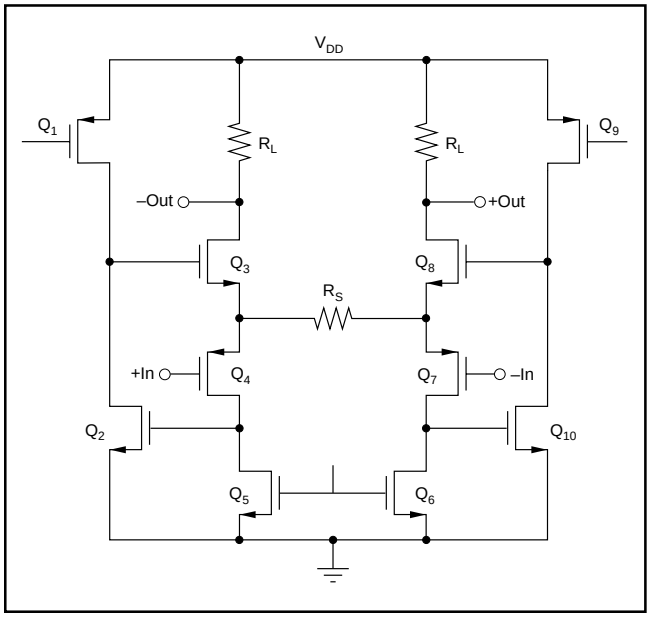


FIGURE 5.

BUFFER

The differential output of the preamplifier is buffered by a wide-band class A-B voltage follower that has the capability of driving low-impedance loads. It was necessary to add this buffer circuit as the preamplifier drives a differential voltage controlled attenuator that has a variable input impedance. If the buffer was not included, the gain of the preamplifier would vary with control voltage and then, when feedback was applied, the input impedance of the preamplifier would vary. The schematic of the buffer is shown in Figure 6. Class A-B operation is achieved by essentially placing two simple operational amplifiers in parallel. One of the operational amplifiers has an n-channel input stage, Q_2 and Q_4, with a p-channel output stage, Q_6. The other operational amplifier has the reverse, a p-channel input stage, Q_9 and Q_{11}, and an n-channel output stage, Q_7. Under zero signal conditions the same current flows through both the Q_6 and Q_7 that are connected together in the output. When the output devices must either source or sink a current that is considerably larger than the bias current, a drive voltage is created at the gates of either Q_6 or Q_7 to provide this current. This architecture was chosen to minimize that power dissipation. The bandwidth of this voltage follower is about 250MHz and is wide enough not to cause stability problems when the loop is closed.

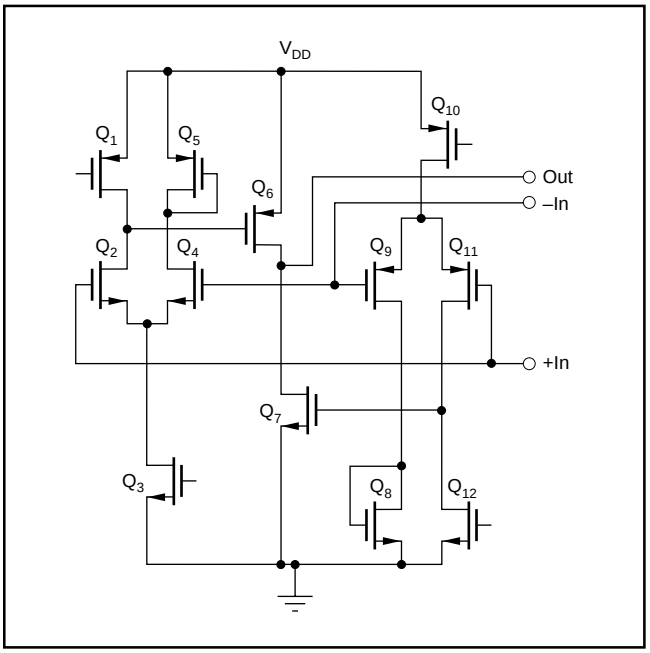


FIGURE 6.

VOLTAGE CONTROLLED ATTENUATOR

The voltage-controlled attenuator was designed to have a control characteristic where the loss in dB is a linear function of the control voltage. Figure 7 shows a block diagram of the attenuator and various waveforms associated with the attenuator. The desired control characteristic is a piece wise approximation to the desired control waveform. When many FETs are in cascade and the stages are turned on sequentially, an approximation to the desired control characteristic is achieved. The desired control of the attenuator is generated by a separate clipping amplifier that drives each gate. Each clipping amplifier is offset in a linear sequential fashion so that each section of the attenuator begins to conduct when the preceding FET achieves maximum attenuation. The output of the clipping amplifier varies between (V_{CM}-V_T) and ground, and is chosen so that the FET is at the edge of conduction. V_{CM} is a common-mode voltage chosen for maximum dynamic range, and V_T is the FET threshold voltage. Biasing circuitry has been designed so the voltage (V_{CM}-V_T) will track voltage and process variations and the attenuator will be relatively free of these effects.

The voltage variable attenuator that has been used in this design is an improvement over the one described in reference [2], [3] and [4]. The newly described attenuator achieves lower noise compared to previous CMOS designs due to the fact that the effective series resistance is lower. The attenuator is comprised of two sections with five parallel elements in each section. A series resistor placed at the input to each section converts a signal current to a signal voltage. All elements of the attenuator are p-channel FETs that are

biased in the triode region and act as resistors. When the attenuation is to be changed, the voltage on the gates of the parallel FETs is changed.

The circuit shown in Figure 7 is used to create the function:

$$A = R\,\frac{V}{V_N} \qquad (3)$$

where A is the gain, R is the radix of the exponential function, V is the control voltage and Vn is a constant.

Taking the logarithm of equation (3) and multiplying both sides by 20 yields:

$$20\log_{10}(A) = 20\log_{10}(R)\,\frac{V}{V_N} \qquad (4)$$

Examining equation (4), it is seen that the left-hand side is the gain expressed in dB and 20log10(R) is a constant C_1. Therefore, by combining terms and simplifying, equation (4) becomes:

$$A_{DB} = CV \qquad (5)$$

For the attenuator shown in Figure 7, there is only a single series resistor for each section, so it becomes necessary for the shunt FETs to vary in size to create the linear in dB gain control characteristic. As an example, assume the control voltage on pin A1 is at its lowest value to create the maximum attenuation from Q_1. The attenuation would be formed from the series resistance and the resistance of the

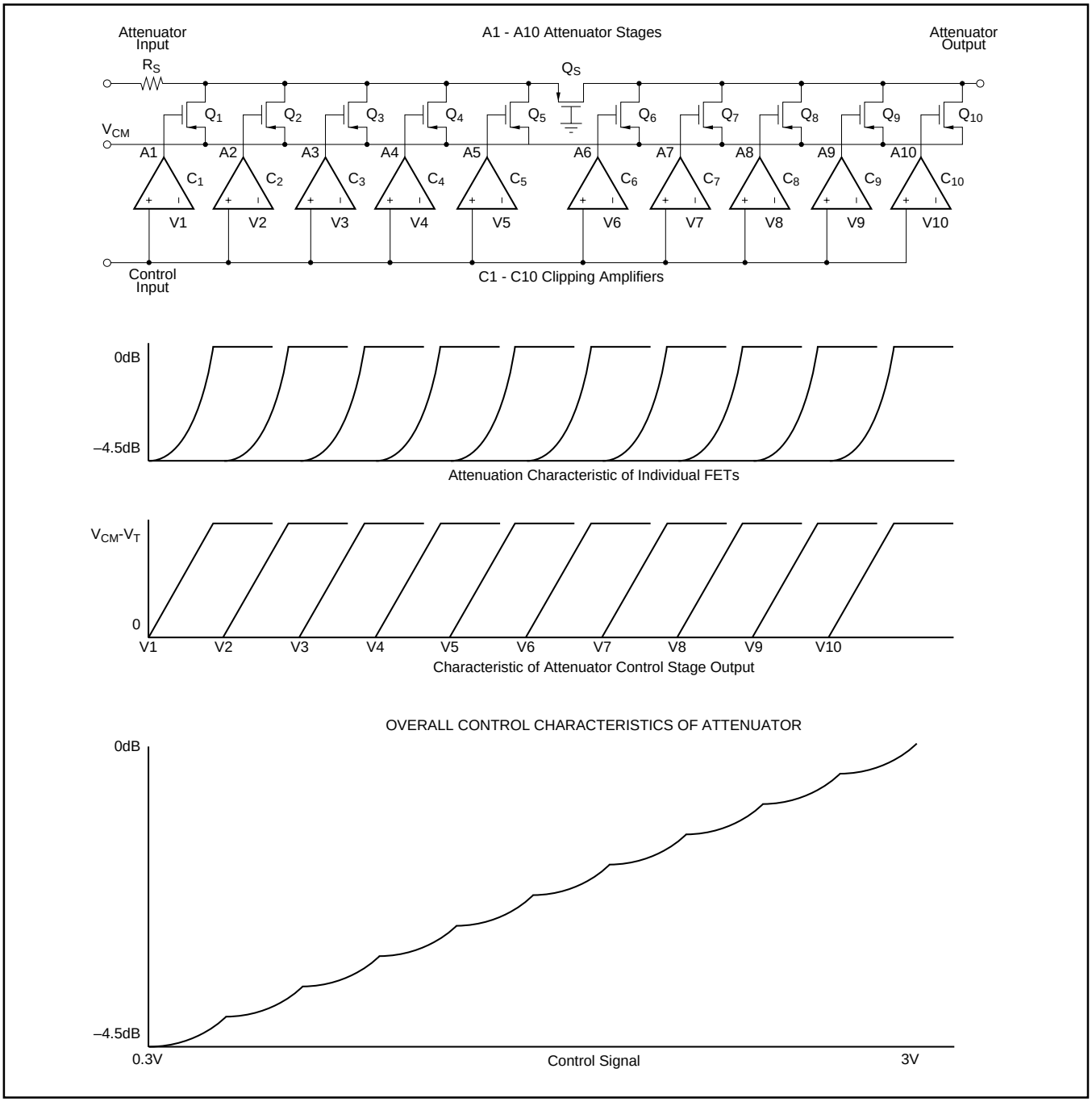


FIGURE 7.

shunt FET Q_1. When the value of the voltage on pin A2 is at the lowest, Q_2 will then create an additional amount of attenuation that is the same as that created by Q_1. The parallel combination of the resistance of Q_1 and Q_2 create a resistance that is less then Q_1 alone. Therefore, when Q2 is applied it is necessary for Q_2 to then have a lower resistance than Q_1 to create a similar amount of attenuation. That is why the shunt FETs shown in Figure 7 are progressively larger, going from Q_1 to Q_5. The second section is the same as the first with Q_S acting like a series resistor. Q_S is a FET rather than a resistor, to achieve better matching over process and temperature. The input resistor Rs was chosen for superior signal-handling capability.

The attenuator can also be programmed for different amounts of maximum attenuation. Figure 8 shows a simplified diagram of a single attenuator section with this feature. When the switch control lines, B1 and B2, are placed in a position so that shunt FETs Q_{1A} through Q_{5A} are selected, a certain attenuation range will be established. When Q_{1B} through Q_{5B} are selected, another combination of shunt FETs is selected, and a different attenuation range can be established. Figure 7 shows the cascading of two attenuator sections. In principal the attenuation range can be extended by adding more FETs to an individual attenuator section. The limit is set by the high-frequency bandwidth; when larger FETs are added, the capacitance associated with the larger FET forms a high-frequency time constant with the series resistor, to limit the bandwidth. There are two considerations at play when deciding upon the number of FETs that should be included in a single section. Bandwidth is one consideration, and another consideration is the accuracy of the gain control voltage curve. The attenuation characteristic is a piece-wise approximation to a linear curve. Over any particular section of the control characteristic, a single-shunt FET controls the attenuation as it makes the transition from being off to its lowest value. This transition is not linear in dB. However, if the transition region is small, the deviation from ideal linearity is not great. The greater the attenuation of a single section, the greater the transition region will be and the greater the deviation from ideal linearity. Therefore, if it is necessary to have a more precise approximation to an ideal linear in dB versus control voltage curve, it would be necessary to have more stages. Each stage would not contribute as much attenuation and the overall attenuation would be achieved with more stages.

When a FET is used as a resistor, the resistance is given by the formula:

$$R_{ON} = \frac{1}{2\mu Cox \frac{W}{L}\left(V_{SG} - V_T\right)} \tag{6}$$

where R_{ON} is the value of the resistance, μ and Cox are constants associated with the process, W and L are the width and length of the transistor, V_{SG} is the source to gate voltage and V_T is the threshold voltage.

The attenuation of each element of the attenuator is given by the formula:

$$A = \frac{R_P}{R_P + R_S} \tag{7}$$

where R_P is the parallel resistor and R_S is the series resistor.

Substituting equation 6 into equation 7 and rearranging terms yields:

$$A = \frac{1}{1 + \frac{W_P}{W_S}\frac{V_{SGP} - V_T}{V_{SGS} - V_T}} \tag{8}$$

where V_{SGP} and V_{SGS} are the gate to source voltage of the parallel resistor and series resistor respectively, and W_P and W_S are the transistor widths. The attenuation of each section is then varied in accordance with the value of V_{SGP}. Equation 8 shows that the attenuation is an inverse function of V_{SGP}.

When the shunt FETs are turned on sequentially an approximation to the exponential function shown in equation 3 can be achieved. Referring to Equation 8, if V_{SGP} varied between two values, the attenuation would also vary between two values. If each FET changed at periodic intervals, the attenuation A would be minimum in each state when V_{SGP} was equal to V_T and maximum in the other state when V_{SGP} was greater than V_T. Now when:

$$A = \frac{1}{1 + \frac{W_P}{W_S}\frac{V_{SGP} - V_T}{V_{SGS} - V_T}} = r^N \tag{9}$$

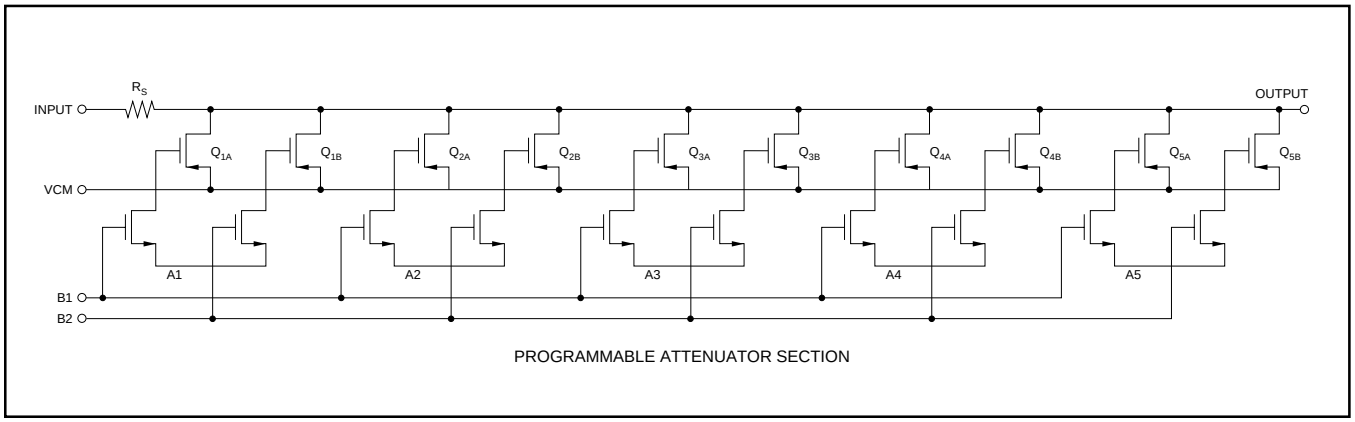


FIGURE 8.

the attenuation function can be represented by a base with an exponent. When the attenuation was one, V_{GSP} would equal V_T, and N would equal 0 and in the other state:

$$N = \log_R \frac{1}{1 + \frac{W_P}{W_S}\frac{V_{SGP} - V_T}{V_{SGS} - V_T}} \qquad (10)$$

When all the stages are in cascade the control characteristic would appear as:

$$A = r^{N1} \bullet r^{N2} \bullet r^{N3} \quad \bullet\bullet\bullet\bullet \quad r^{Nn} = r^{N1+N2+N3++++Nn} \qquad (11)$$

The exponent shown in the last part of Equation 11 is the sampled version of the linear exponent shown in Equation 3. This would give rise to an attenuation control function that is similar in shape to the stepped characteristic of a digital-to-analog converter. A closer approximation to the true exponential characteristic would be a function of the number of steps or approximations in a given interval. The voltage on the gate of each FET varies linearly with the input signal, rather than like a step, and this will have the effect of smoothing the attenuation control characteristic as shown in Figure 8.

OVERLOAD PROTECTION CIRCUITRY

For the ultrasound imaging system to be able to discriminate between objects of widely different sizes, it is necessary that the amplifying system have excellent overload-recovery capability. Overload protection is achieved by sensing the amplitude of the signal that comes from the voltage-controlled attenuator with a comparator. When the signal exceeds the threshold level of the comparator, the output of the attenuator is switched to a fixed DC level whose amplitude is within the range of the post amplifier, thereby preventing serious recovery problems. It is necessary to sense both the upper and lower part of the waveform, as the signal is bipolar. A block diagram of this circuitry is shown in Figure 9. The gain of the post amplifier is programmable, so that it is necessary to also program the DC level that is inserted in place of the signal to prevent overload.

POST AMPLIFIER

Figure 10 shows a simplified circuit diagram of the post amplifier. The gain of the post amplifier is programmed in an inverse manner compared to the voltage-controlled attenuator. When the attenuator is programmed for maximum attenuation, the post amplifier will have maximum gain. The overall characteristic of the attenuator-amplifier combination will then have a gain that varies from a minimum of 0dB to a maximum determined by the maximum gain of the post amplifier. The maximum gain of the post amplifier can be programmed in 3dB steps from 24dB to 45dB. Corre-

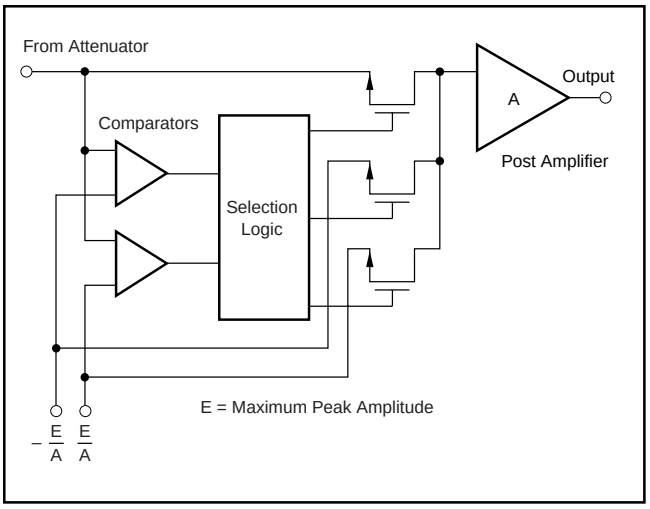


FIGURE 9.

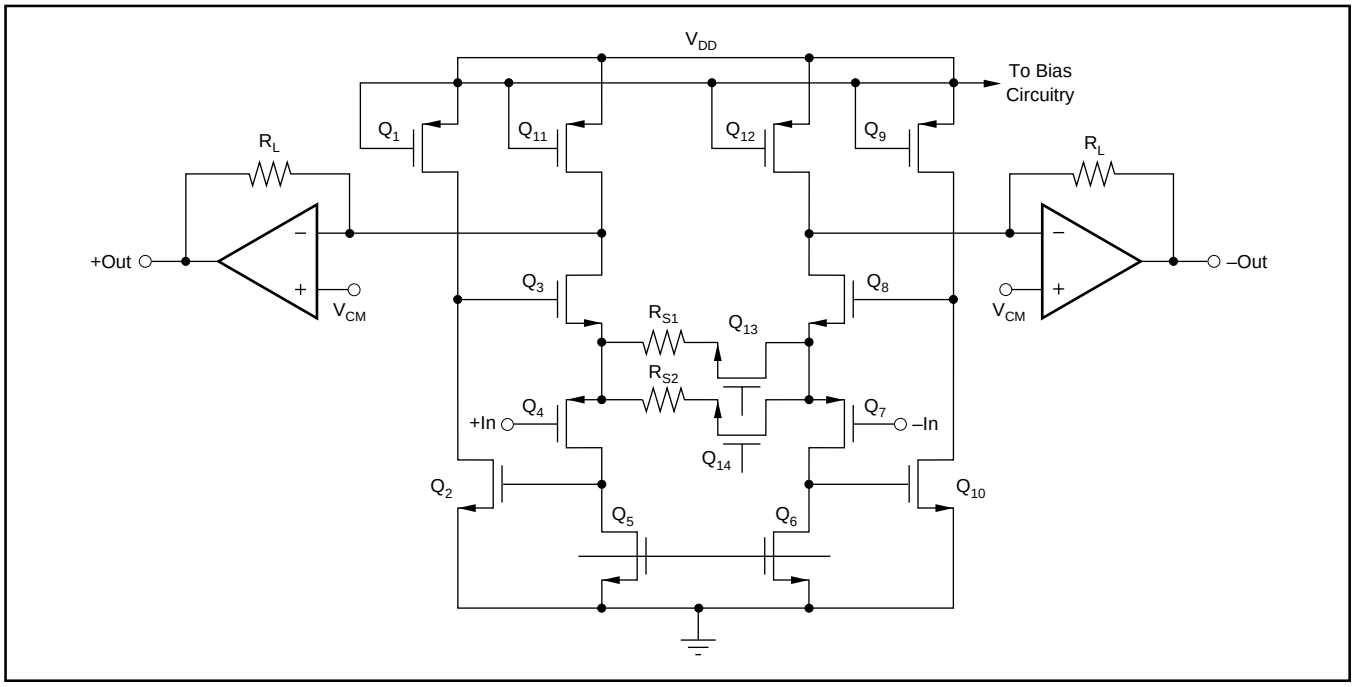


FIGURE 10.

spondingly the maximum attenuation of the attenuator can also be programmed for a 24dB to 45dB loss. The net effect of this combination is a combined gain characteristic that will vary from a minimum of 0dB to a maximum ranging from 24dB to 45dB.

The architecture of the post amplifier consists of a differential programmable voltage-to-current converter stage followed by two transconductance amplifiers to form a differential output. The circuitry associated with the voltage-to-current converter is similar to that previously described of the low-noise amplifier. Low noise is also required for the postamplifier, due to the large amount of attenuation that can be inserted between the low-noise preamplifier and this output amplifier. At minimum attenuation, the noise of the preamplifier would dominate, which is not true at maximum attenuation. The FET switches that are in series with the resistors that are placed between the sources of the input p-channel FETs, are sized to have much lower resistance to avoid creating linearity problems. A transconductance amplifier is used to buffer the output of the programmable voltage-to-current converter. The low-noise pre-amplifier used a voltage follower as a buffer, as the value of the feedback resistor would have been too small to drive, since the buffer was also required to drive the input of the 150Ω attenuator. A very small resistor was necessary to achieve exceptionally low noise. The disadvantage of this approach is that there is a large voltage swing at the output of the amplifying stage which raises the distortion level. The post amplifier does not require as low noise, so it was desirable to use a transconductance stage with a 2.4kΩ feedback resistor This has the effect of reducing the swing at the output drains Q_3, Q_8, Q_{11} and Q_{12}.

APPENDIX I

NOISE FIGURE OF CONVENTIONAL AND ACTIVE TERMINATION

One of the key features of the low-noise amplifier architecture that has been described is the use of feedback to achieve superior noise performance as compared to a conventional means for terminating a cable. Ultrasound probes are typically connected to the low-noise amplifier through 3 meters of cable. Therefore, it is necessary to terminate the cable to achieve maximum power transfer and to avoid pulse distortion effects such as false echoes. The following derivation will demonstrate this point. Figure 11 shows a simplified block diagram of a signal E_S with a source impedance R_S that is transmitted through a cable and terminated at the input to the low-noise amplifier with an impedance R_T. The amplifier has a fixed gain A with an associated noise density of E_N. Equation 7 is the noise figure of an amplifier whose input is terminated conventionally.

Figure 12 shows a block diagram of the low-noise amplifier that employs feedback to terminate the cable. Usually, the gain of an operational amplifier is very large and under these circumstances the input impedance becomes quite small. In general the input impedance of an inverting feedback amplifier is given by the expression shown in Figure 8 where R_F is the feedback resistor and A is the amplifier gain. The closed-loop gain of this circuit is given by Equation 9 under the assumption that $R_F = R_S (1+A)$. Equation 13 is the noise figure of an amplifier using active termination. Figure 13 shows the improvement in noise figure using active termination.

References

[1] *"Dual, Ultralow Noise Variable Gain Amplifier"*, Analog Devices AD604.

[2] *"An Analog-to-Digital Processor For Camcorders And Digital Still Cameras"*, IEEE Transactions on Consumer Electronics, Vol 44, No. 3, August 1998, pages 570-580.

[3] *"Variable-Gain Amplifier Controlled by an Analog Signal and Having a Large Dynamic Range"*, Patent Number 5,077,541.

[4] *"Logarithmic Attenuator and Method"*, Patent Number 5,880,618.

1) $\frac{E_O}{E_S} = \frac{A}{2}$

2) Input Noise = $\sqrt{4kTBR_S}$

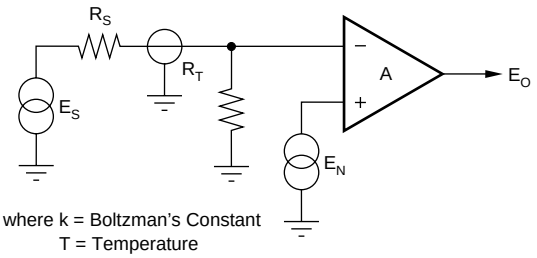
3) Input SNR = $\frac{E_S}{\sqrt{4kTBR_S}}$

4) Output Signal = $\frac{E_S}{2} A$

5) Output Noise = $\sqrt{E_N^2 + 2kTBR_S}$ A

6) Output SNR = $\frac{\frac{E_S}{2} A}{\sqrt{E_N^2 + 2kTBR_S} A} = \frac{\frac{E_S}{2}}{\sqrt{E_N^2 + 2kTBR_S}}$

7) Noise Figure = $\frac{\text{Input SNR}}{\text{Output SNR}} = \frac{\frac{E_S}{\sqrt{4kTBR_S}}}{\frac{\frac{E_S}{2}}{\sqrt{E_N^2 + 2kTBR_S}}} = \sqrt{2 + \frac{E_N 2}{kTBR_S}}$



where k = Boltzman's Constant
T = Temperature
B = Bandwidth

FIGURE 11.

8) $R_{IN} = \frac{R_F}{1+A}$

9) $\frac{E_O}{E_S} = \frac{A}{2}$

10) Output Signal = $\frac{E_S}{2} A$

11) Output Noise = $\frac{A(A+2))}{2(A+1)} \sqrt{E_N{}^2 + 4kTBR_S \frac{(A+1)}{(A+2)}}$

12) Output Signal / NoiseRatio = $\frac{\frac{E_S}{2} A}{\frac{A(A+2)}{2(A+1)} \sqrt{E_N{}^2 + 4kTBR_S} \frac{(A+1)}{(A+2)}}$

13) Noise Figure = $\frac{\text{Input Signal / Noise Ratio}}{\text{Output Signal / Noise Ratio}} = \frac{\frac{E_S}{\sqrt{4kTBR_S}}}{\frac{(A+2)}{(A+1)} \sqrt{E_N{}^2 + 4kTBR_S \frac{(A+1)}{(A+2)}}}$

$= \sqrt{\frac{(A+2)}{(A+1)}} \sqrt{1 + \frac{E_N{}^2 (A+2)}{4kTBR_S (A+1)}}$

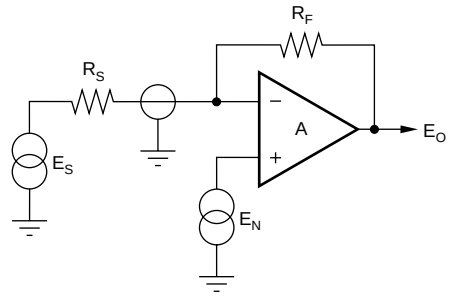


FIGURE 12.

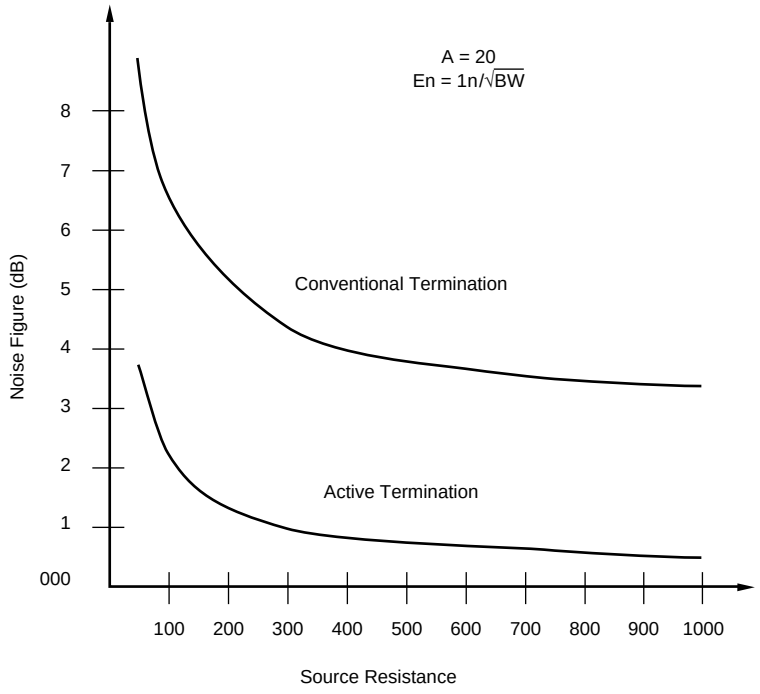


FIGURE 13.

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