Texas Instruments QML Lot Documents

Texas Instruments is certified and listed by the Defense Logistics Agency Land And Maritime (DLA) as a manufacturer of QML Class Q and Class V microcircuits (integrated circuits) in accordance with MIL-PRF-38535 (General Specification For Manufacturing Integrated Circuits). The Quality System utilized by Texas Instruments in the manufacture of these microcircuits is fully compliant to the requirements of MIL-PRF-38535 and ISO9001.

The following documents summarizing screening and Quality Conformance Inspection are provided with each Texas Instruments QML lot.

<table>
<thead>
<tr>
<th>Document</th>
<th>Class Q</th>
<th>Class V</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Certificate of Conformance per MIL-PRF-38535</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>2. Processing Conformance Report (PCR) summarizing</td>
<td></td>
<td></td>
</tr>
<tr>
<td>a. Assembly Lot Traceability</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>b. Wafer Lot Traceability</td>
<td></td>
<td></td>
</tr>
<tr>
<td>c. 100% Screens Performed</td>
<td></td>
<td></td>
</tr>
<tr>
<td>d. QCI** Group A Testing</td>
<td></td>
<td></td>
</tr>
<tr>
<td>e. QCI Group B Testing</td>
<td></td>
<td></td>
</tr>
<tr>
<td>f. QCI Group C Testing</td>
<td></td>
<td></td>
</tr>
<tr>
<td>g. QCI Group E Testing (Class V RHA only)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>h. QCI WLA Testing (Class V only)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3. QCI Group B Summary Report</td>
<td>Optional*</td>
<td>Yes</td>
</tr>
<tr>
<td>4. QCI Group C Summary Report</td>
<td>Optional*</td>
<td>Yes</td>
</tr>
<tr>
<td>5. QCI Group D Summary Report</td>
<td>Optional*</td>
<td>Yes</td>
</tr>
<tr>
<td>6. QCI Group E Summary Report</td>
<td>N/A</td>
<td>RHA Only</td>
</tr>
<tr>
<td>7. QCI Wafer Lot Acceptance Summary Report</td>
<td>N/A</td>
<td>Yes</td>
</tr>
</tbody>
</table>

* A copy of this report may be ordered or downloaded (see below)

Instructions for downloading a copy of a lot specific PCR and QCI documents are shown in Appendix I. Examples of each document are shown in Appendix II.

For additional information please contact your Texas Instruments representative or post a question in the TI High Reliability E2E Community Forum [http://e2e.ti.com/support/applications/hirel/](http://e2e.ti.com/support/applications/hirel/)
Appendix I – Instructions for Downloading Lot Documents

To access the system for downloading QML lot documents a MYTI user account with an additional two-factor authorization is required. For difficulties in logging on please contact qci_2fa@list.ti.com.

1. To begin obtain the specific lot number for the reports desired. It can be obtained from the following documents provided with the lot:
   a. The Certificate of Conformance (listed as QA Lot Number)
   b. The Processing Conformance Report (listed as Q.C. Reference Number)
   c. For this example we will use the TPS50601-SP part type 5962R1022101VSC and PCR Lot Number 5005609.
   d. Please note that a PCR Lot Number is also known as a QA Lot Number or QC Reference Number and that a Wafer Lot Number is also known to as a Diffusion Lot Number.

2. Log on to https://qci.ext.ti.com/ using a MYTI account

3. For a QCI Summary Report (Group B, C, D, E, or WLA)
   a. Under the “Reports” tab highlight “Lot Test Summary” the click the report desired, for example “Group E Lot Test Summary”
   b. Enter the “PCR Lot Number” in the last box and click “Show Report”.
   c. From the displayed page the report can be copied to the clip board, printed to a local printer, transferred to Excel, or forwarded via email.

   a. On the lower section of the screen under “File Attachment” a list of the associated RHA reports for the wafer lot associate with the PCR Lot Number in question. Right-click on the filename that that is associated with the wafer number and testing desired and download to a local directory.

5. At any time click the “Help” link in the upper-right corner of the page for assistance.
Appendix II – Example Lot Documents
Texas Instruments Incorporated
Military Products Department
Military High Reliability Integrated Circuits
Processing Conformance Report

Device Type: 5962R1022101VS
SMD: 5962R1022101VS
Device Description:

PCR Lot Number: 500560
Lot Window:

Assembly Location: MM
Wafer Lot #: 210856
Assembly Data Code Year: 2015
Wafer Lot Date Code Year: 2013

Week: 32
Lot: 5
Die Run: 5
W/F Code: 5

Integrated Circuits referenced above have received the following processing per recorded lot history:

SCREEN
- INTERNAL VISUAL PRECAP 2010 CONDITION A (100X)
- INTERNAL VISUAL PRECAP 2010 CONDITION A (40X)
- TEMPERATURE CYCLING 2014 CONDITION C
- CENTRIFUGE 2001 CONDITION E (Y1 PLANE)
- PIND TEST 2020 CONDITION A
- RADIOGRAPHY 2012 MONITOR OR (100%) INTERNAL ELECTRICAL TEST
- TEMPERATURE CYCLING 1010 CONDITION C
- CENTRIFUGE 2001 CONDITION E, Y1 PLANE
- PIND TEST 2020 CONDITION A
- RADIOGRAPHY 2012
- 100%
- INTERIM ELECTRICAL TEST

FINAL ELECTRICAL TEST TEMP: 25°C
- 125°C
- 5°C
- N/A
- N/A

TEST PROGRAM (s)
- EF3527/07
- EF3527/07
- EF4994/00

- HERMETICITY
- FINE LEAD GROVE LEAK
- EXTERNAL VISUAL
- EXTERNAL VISUAL

QUALITY CONFORMANCE ATTRIBUTE DATA GROUP "A" "SUMMARY" + "DETAIL"

SUBGROUP TEST & TEMP SAMPLE SIZE
- A-1/4/7 DC ELECTRICAL - AMBIENT 116 OR 100%
- A-2/5/8 DC ELECTRICAL - MAXIMUM 116 OR 100%
- A-3/6/8 DC ELECTRICAL - MINIMUM 116 OR 100%
- A-9 AC ELECTRICAL - AMBIENT 116 OR 100%
- A-10 AC ELECTRICAL - MAXIMUM 116 OR 100%
- A-11 AC ELECTRICAL - MINIMUM 116 OR 100%

Device Lead Finish complies with MIL-PRF-38535 A.3.5.6.3 Microcircuit finishes: "Finishes of all external leads or terminals and all external package elements shall conform to either A.3.5.6.3.2 or A.3.5.6.3.3 as applicable. The use of pure tin, as an underplate or final finish, is prohibited both internally and externally. The tin content of solder shall not exceed 97 percent. Tin shall be alloyed with a minimum of 3 percent lead by weight.

SOLDER PROCESSING DATE (IF APPLICABLE): N/A
NOTE: The following documents MUST be pulled and sent with each lot:
1) PROCESS CONFORMANCE REPORT
2) GENERIC GROUP B QCI SUMMARY REPORT
3) GENERIC GROUP D QCI SUMMARY REPORT
4) WATER LOT ACCEPTANCE REPORT FOR THE WATER LOT USED IN THIS ASSEMBLY LOT

Product has passed Group E RHA QCI in accordance with MIL-PRF-38515.

Prepared By: Kat Kangawamme
Date: 09/09/2015

QCI Group B - Lot #: 200566
Date Code: 1502
Pkg Type: 20M3H
Lead Finish: A
Wafer Lot Data Code: 1A

QCI Group C - Lot #: 107466
Pkg Type: 20M3H
Lead Finish: A

QCI Group E - Lot #: 210856
Wafer Lot #: 210856

Wafer Lot Accept - Lot #: 3017466

Group B Summary Report

Lot Number: 5005609
Device Name: TPS50601-RHA
Date Code: 2015-32-A
Assembly Site: MMT
Test Start: 09/09/2015
Test Complete: 09/09/2015
Pin: 20
Package: HKH
Lead Finish: A
Package Family: GROUP 9

<table>
<thead>
<tr>
<th>66666 Sub-Group</th>
<th>Test</th>
<th>Method</th>
<th>Sample Size</th>
<th>Rejects / Data</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>B2</td>
<td>RESISTANCE TO SOLVENTS</td>
<td>TM2015</td>
<td>3</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>B3</td>
<td>SOLDERABILITY</td>
<td>TM2003</td>
<td>3</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>B5</td>
<td>BOND STRENGTH</td>
<td>2011</td>
<td>4</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>B5</td>
<td>DIE ATTACH STRENGTH</td>
<td>2019 OR 2027</td>
<td>4</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

Notes:
1. Resistance to solvents testing required only on devices using inks or paints as a marking medium.
2. 22 leads / 3 packages minimum. Not required for solder columns
3. 15 wires / 4 units minimum

Comments:

Prepared By: Vut Kangkamanee
Prepared By Email: x0194988@ti.com
Prepare Date: 09/09/2015
Group C Summary Report

Lot Number: 3017448  
Lot Date Code: 2014-02-A  
Wafer Lot Date Code: 2013-1Q-C-R  
Wafer Lot Number: 2108506

Device Name: TPS50601-RHA  
Die Attach: QMI  
Package: HKH

Assembly Site: MMT  
Window: 1Q 2013 to 1Q 2014  
MCG: 88

Parent Die: RTPS50601VRHC0  
Pin: 20

Test Start: 02/03/2014  
Test Complete: 03/24/2014

<table>
<thead>
<tr>
<th>Sub-Group</th>
<th>Test</th>
<th>Method</th>
<th>Sample Size</th>
<th>Rejects / Data</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>Steady-state life test</td>
<td>1005</td>
<td></td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>C1</td>
<td>Endpoint Electrical Test</td>
<td>45</td>
<td></td>
<td>0</td>
<td>2</td>
</tr>
</tbody>
</table>

Notes:
1. 1,000 hours/125C or equivalent. (If greater than 1,000 hours/125C enter actual conditions into comments below)
2. Endpoint electrical testing in accordance with device test specification.

Comments:

50/0 TESTED

Prepared By: Vut Kangkamanee  
Prepared By Email: x0194988@ti.com  
Prepare Date: 03/24/2014
Group D Summary Report

<table>
<thead>
<tr>
<th>6666 Sub-Group</th>
<th>Test</th>
<th>Method</th>
<th>Sample Size</th>
<th>Rejects / Data</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>D1</td>
<td>Physical Dimensions</td>
<td>2016</td>
<td>15</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>D2</td>
<td>Lead Integrity</td>
<td>2004 and 2028</td>
<td>45</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>D2</td>
<td>Seal (Fine and Gross)</td>
<td>1014</td>
<td></td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>D3</td>
<td>Thermal Shock</td>
<td>1011</td>
<td>15</td>
<td>0</td>
<td>2</td>
</tr>
<tr>
<td>D3</td>
<td>Temperature Cycle</td>
<td>1010</td>
<td></td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>D3</td>
<td>Moisture Resistance</td>
<td>1004</td>
<td></td>
<td>0</td>
<td></td>
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<tr>
<td>D3</td>
<td>Visual Examination</td>
<td>1004 and 1010</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>D3</td>
<td>Seal (Fine and Gross)</td>
<td>1014</td>
<td></td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>D3</td>
<td>End-point electrical test</td>
<td></td>
<td>0</td>
<td>4</td>
<td></td>
</tr>
<tr>
<td>D4</td>
<td>Mechanical Shock</td>
<td>2002</td>
<td>15</td>
<td>0</td>
<td>5</td>
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<tr>
<td>D4</td>
<td>Vibration, Variable Freq</td>
<td>2007</td>
<td></td>
<td>0</td>
<td>6</td>
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<tr>
<td>D4</td>
<td>Constant acceleration</td>
<td>2001</td>
<td></td>
<td>0</td>
<td>7</td>
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<tr>
<td>D4</td>
<td>Seal (Fine and Gross)</td>
<td>1014</td>
<td></td>
<td>0</td>
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<tr>
<td>D4</td>
<td>Visual Examination</td>
<td>1010 and 1011</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>D4</td>
<td>End-point electrical test</td>
<td></td>
<td>0</td>
<td>4</td>
<td></td>
</tr>
<tr>
<td>D5</td>
<td>Salt Atmosphere</td>
<td>1009</td>
<td>15</td>
<td>0</td>
<td>10</td>
</tr>
<tr>
<td>D5</td>
<td>Visual Inspection</td>
<td>1009</td>
<td></td>
<td>0</td>
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<tr>
<td>D5</td>
<td>Seal (Fine and Gross)</td>
<td>1014</td>
<td></td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>D6</td>
<td>Internal water vapor</td>
<td>1018</td>
<td>3 (5)</td>
<td>0 (1)</td>
<td>8</td>
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<tr>
<td>D7</td>
<td>Adhesion of lead finish</td>
<td>2025</td>
<td>15</td>
<td>0</td>
<td>9</td>
</tr>
<tr>
<td>D8</td>
<td>Lid Torque</td>
<td>2024</td>
<td>5</td>
<td>0</td>
<td>11</td>
</tr>
</tbody>
</table>

Notes:
1. Condition B2, 3 devices, 45 leads total. For PGA and rigid leads use Condition B1 or Method 2028. For LCCC packages only, use condition D and SS of 15 based on the number of pads tested from 3 devices minimum.
2. Condition B, 15 cycles.
3. Condition C, 100 cycles.
4. Endpoint electrical testing in accordance with device test specification.
5. Condition B.
6. Condition A.
7. Condition E (20KG) Y1 axis only.
8. Endpoint electrical testing in accordance with device test specification.
9. 5000 PPM and 100C. Sample size is 3/0 or 5/1.
10. Endpoint electrical testing in accordance with device test specification.
11. Glass Frit Seal Only - N/A for MMT Assembly.

Comments:

File Attachment

<table>
<thead>
<tr>
<th>Filename</th>
<th>No Files Uploaded</th>
</tr>
</thead>
</table>

Prepared By: Vut Kangkamanee  Prepared By Email: x0194988@ti.com  Prepare Date: 09/03/2015
Group E Summary Report

Lot Number: 2108506  
Device Name: TPS50601-RHA

Wafer Lot Code: 2013-1Q-C-R  
Wafer #: 14  
Parent Die: RTP50601VRHC0

Test Start: 08/05/2013  
Test Complete: 09/11/2013  
Wafer Lot Number: 2108506

Pin: 20  
Package: HKH  
MCG: 88

<table>
<thead>
<tr>
<th>Sub-Group</th>
<th>Test</th>
<th>Method</th>
<th>Sample Size</th>
<th>Rejects / Data</th>
<th>Notes</th>
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</thead>
<tbody>
<tr>
<td>E2</td>
<td>RHA LOT ACCEPTANCE REPORT</td>
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<tr>
<td>E2</td>
<td>Total Ionizing Dose</td>
<td>1019</td>
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<td>1</td>
</tr>
<tr>
<td>E2</td>
<td>Dose Rate mrad(Si)/sec</td>
<td></td>
<td></td>
<td>N/A</td>
<td></td>
</tr>
<tr>
<td>E2</td>
<td>-or-</td>
<td></td>
<td></td>
<td>---</td>
<td></td>
</tr>
<tr>
<td>E2</td>
<td>Dose Rate rad(Si)/sec</td>
<td></td>
<td>100</td>
<td></td>
<td></td>
</tr>
<tr>
<td>E2</td>
<td>Total Dose krad (Si)</td>
<td></td>
<td>100</td>
<td></td>
<td></td>
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<tr>
<td>E2</td>
<td>Electrical Test</td>
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<td>2</td>
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</tr>
<tr>
<td>E2</td>
<td>Total Grp E Sample Size</td>
<td></td>
<td>22</td>
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<tr>
<td>E2</td>
<td>Rejects</td>
<td></td>
<td></td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

Notes: Registered my.ti.com users may download the RHA acceptance report from https://qci.ext.ti.com/qci/
1. Dose Rate and Total Dose per TI RHA QM Plan
2. 25C: Maximum supply voltage
3. Endpoint electrical testing in accordance with device test specification.
4. Registered my.ti.com users may download the RHA acceptance report from https://qci.ext.ti.com/qci/ (In case of difficulty contact qci_2fa@list.ti.com)

Comments:
1/ The manufacturer supplying device type 01 has performed characterization testing in accordance with MIL-STD-883 method 1019 paragraph 3.13.1.1 and the parts exhibited no enhanced low dose rate sensitivity (ELDRS) at a dose level of 100 krad(Si). The radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A and condition D to a maximum total dose of 100K rads(Si). 2/ Device type 01 is irradiated at dose rate = 50 - 300 rads(Si)/s in accordance with MIL-STD-883, method 1019, condition A, and is guaranteed to a maximum total dose specified. The effective dose rate after extended room temperature anneal = 0.1 rad (Si)/s per MIL-STD-883, method 1019, condition A, section 3.11.2. The total dose specification for these devices only applies to the specified effective dose rate, or lower environment.

File Attachment

<table>
<thead>
<tr>
<th>Filename</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS50601-SP_RHA_DLA_Packet.pdf</td>
</tr>
</tbody>
</table>

Prepared By: a0461373  
Prepared By Email:  
Prepare Date: 03/31/2014
**WLA Summary Report**

**Lot Number:** 3017448  
**Device Name:** TPS50601-RHA  
**Wafer Lot Date Code:** 2013-1Q-C-R  
**Wafer Lot Number:** 2108506  
**Parent Die:** RTPS50601VRHC0  
**Lead Finish:** A  
**MCG:** 88  
**Test Start:** 02/03/2014  
**Test Complete:** 03/24/2014

<table>
<thead>
<tr>
<th>Sub-Group</th>
<th>Test</th>
<th>Method</th>
<th>Sample Size</th>
<th>Rejects / Data</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>WLA-1</td>
<td>Wafer Thickness</td>
<td>5007</td>
<td>2 wafers/lot</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>WLA-2</td>
<td>Metallization Thickness</td>
<td>5007</td>
<td>1 wafer/lot</td>
<td>0</td>
<td>2</td>
</tr>
<tr>
<td>WLA-3</td>
<td>Thermal Stability</td>
<td>5007</td>
<td>1 wafer/lot</td>
<td>0</td>
<td>2,3</td>
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<tr>
<td>WLA-4</td>
<td>SEM Inspection Lot Acceptance</td>
<td>2018</td>
<td>2 wafers/lot</td>
<td>0</td>
<td>2</td>
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<tr>
<td>WLA-4</td>
<td>Lab Performing Analysis:</td>
<td></td>
<td></td>
<td></td>
<td>TI</td>
</tr>
<tr>
<td>WLA-5</td>
<td>Glassivation Thickness</td>
<td>5007</td>
<td>1 wafer/lot</td>
<td>0</td>
<td>2</td>
</tr>
<tr>
<td>WLA-6</td>
<td>Gold Backing Thickness</td>
<td>5007</td>
<td>1 wafer/lot</td>
<td>0</td>
<td>2,4</td>
</tr>
<tr>
<td>WLA-7</td>
<td>Steady-state life test</td>
<td>1005</td>
<td></td>
<td>0</td>
<td>5</td>
</tr>
<tr>
<td>WLA-7</td>
<td>Endpoint Electrical Test</td>
<td>1005</td>
<td>45</td>
<td>0</td>
<td>6</td>
</tr>
</tbody>
</table>

**Notes:**
1. This test is not required when the finished wafer design thickness is greater than 10 mils before backgrind.
2. In-line monitor data for this wafer lot may be used.
3. Applicable to all linear, all MOS, all bipolar digital operating at 10V or more (VFB/VT/C-V)
4. Gold backed wafers only.
5. 1,000 hours/125C or equivalent
6. Endpoint electrical testing in accordance with device test specification

**Comments:**

**Prepared By:** a0461373  
**Prepared By Email:**  
**Prepare Date:** 03/26/2014
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