Texas Instruments
Military and HiRel Products

Nomenclature and Process Flows
**Typical Analog Product**

**Example:**  **TLE2022AMJGBEP**

**Prefix—** **TLE**
- SNJ = TI Interface, MILPRF-38535 (QML)
- SN = Commercial Processing
- TL = TI Linear Control Circuit
- TLC = TI LinCMOST™
- TLE = TI Excalibur
- TLV = TI Linear Low Voltage
- TPIC = TI Intelligent Power
- AD = Analog Devices™ *
- AM = Advanced Micro Devices™ *
- LM = National Semiconductor™ *
- LT = Linear Technology™ *
- OP = PMI™ *
- SE = Signetics™ *
- µA = Fairchild™ *
- THS = TI High Power
- TPS = TI Power Supply

**Package Type / Pin Count—** **JG**
- DA = Plastic Small Outline Package / 28, 30, 32 or 38
- FK = Ceramic Leadless Chip Carrier / 20 or 28
- GA = Ceramic Pin Grid Array / 84
- HFG = Ceramic Flatpack / 84 or 164
- J = Ceramic DIP / 8, 14, 16, 20 or 28
- JG = Ceramic DIP / 8
- U = Ceramic Flatpack / 10
- W = Ceramic Flatpack / 14 or 16
- WD = Ceramic Flatpack / 56
- L = Ceramic Leadless Chip Carrier / 20 or 28
- PHP = Plastic Quad Flatpack PowerPad / 48
- PCE = Plastic Quad Flatpack / 144 or 160
- PWP = Plastic Power TSSOP / 14, 16, 20, 24 or 28
- DW = Plastic Widebody (30 mil) SOIC / 16, 20, 24 or 28
- TCP = Tape Carrier Package / Custom
- PFB = Plastic Quad Flatpack / 48

**Unique Device Designator—** **2022A**
- A or B in last position = Upgrade

**Temperature Range—** **M**
- M = -55°C to 125°C (applicable to all TI prefixes except SNJ)
- Q = -40°C to 125°C
- I = -40°C to 85°C
- T = -40°C to 105°C

**Process Level—** **B**
- Blank = Standard Suffix, Commercial Processing
- B = MIL-PRF-38535 (QML)

**Enhanced Plastic—** **EP**

* = Second Source
TI-Unitrode Power Management Products

Example: **UC1825BJ883BEP**

**Prefix—TLE**
- UC = Linear Integrated Circuits
- UCC = BiCMOS

**Part Number—1825**
- First Digit “1” = Military Temperature Range*
- First Digit “2” = Industrial Temperature Range*
- First Digit “3” = Commercial Temperature Range*

**Optional Grades—B**
- A or B = Improved Version

**Process Level—883B**
- J, JE = Ceramic DIP (300 mil and 600 mil)
- L, L20 = Ceramic Leadless Chip Carrier (CLCC)

**Enhanced Plastic—EP**

* = Consult individual data sheets for specific temperature ranges on each part.
** = The “883B” designator was retained to be consistent with the original Unitrode naming convention.
# Digital Signal Processors (DSPs)

**Example:** SMJ320C40GBM40EP

<table>
<thead>
<tr>
<th>Prefix—<strong>SMJ</strong></th>
<th>Package Type / Pin Count—<strong>GB</strong></th>
<th>Speed Designator—<strong>GB</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>SM</td>
<td>JD = CDIP</td>
<td>12 = 120 MHz</td>
</tr>
<tr>
<td>SMJ</td>
<td>FD/FJ = LCCC</td>
<td>16 = 160 MIPS (VC5416)</td>
</tr>
<tr>
<td>SMQ</td>
<td>GB/GF = CPGA</td>
<td>20 = 200 MIPS (VC5421)</td>
</tr>
<tr>
<td>(Order by SMD)</td>
<td>GFA = CFGP</td>
<td>33 = 33 MHz</td>
</tr>
<tr>
<td>SMP</td>
<td>GLG/GLP = FC/CSP</td>
<td>40 = 40 MHz</td>
</tr>
<tr>
<td>SMX</td>
<td>HFH/HFG = CFP</td>
<td>50 = 500 MHz (C64xx)</td>
</tr>
<tr>
<td>TMS</td>
<td>HFP = CFP</td>
<td>60 = 60 MHz (600 MHz C6415)</td>
</tr>
<tr>
<td>TMP</td>
<td>KGD = KGD</td>
<td>66 = 66 MHz</td>
</tr>
<tr>
<td>SMV</td>
<td>PCM/PQ = QFP</td>
<td>10 = 100 MIPS (C54x)</td>
</tr>
<tr>
<td>(Order by SMD)</td>
<td>GNM = FBEA</td>
<td>14 = 140 MHz</td>
</tr>
<tr>
<td></td>
<td>GAD = FCµEBA</td>
<td>15 = 150 MHz</td>
</tr>
<tr>
<td></td>
<td>GJC = FC/CSP</td>
<td>16 = 167 MHz</td>
</tr>
<tr>
<td></td>
<td>GJL = FC/CSP</td>
<td>17 = 175 MHz</td>
</tr>
<tr>
<td></td>
<td>GLZ = FCBGA</td>
<td>20 = 200 MHz</td>
</tr>
<tr>
<td></td>
<td>GDP = LQFP</td>
<td>120 = 120 MFLOPS (VC33)</td>
</tr>
<tr>
<td></td>
<td>PGE = Plastic LQFP</td>
<td>150 = 150 MFLOPS (VC33)</td>
</tr>
<tr>
<td></td>
<td>GGU = BGA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>GGW = BGA Microstar</td>
<td></td>
</tr>
<tr>
<td></td>
<td>PGF = LQFP</td>
<td></td>
</tr>
<tr>
<td></td>
<td>GHH = PBGA</td>
<td></td>
</tr>
</tbody>
</table>

**320 DSP Family Designator—**320 or 32

**320 DSP Product Designator—**C40

<table>
<thead>
<tr>
<th>Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>BC</td>
<td>CMOS Boot</td>
</tr>
<tr>
<td>C</td>
<td>CMOS</td>
</tr>
<tr>
<td>E</td>
<td>CMOS EPROM</td>
</tr>
<tr>
<td>F</td>
<td>CMOS FLASH</td>
</tr>
<tr>
<td>LC</td>
<td>CMOS 3.3 V</td>
</tr>
<tr>
<td>VC</td>
<td>CMOS 1.5 V / 3.3 V</td>
</tr>
<tr>
<td></td>
<td>14 = E14</td>
</tr>
<tr>
<td></td>
<td>25 = C25</td>
</tr>
<tr>
<td></td>
<td>26 = C26</td>
</tr>
<tr>
<td></td>
<td>30 = C30</td>
</tr>
<tr>
<td></td>
<td>31 = C31</td>
</tr>
<tr>
<td></td>
<td>32 = C32</td>
</tr>
<tr>
<td></td>
<td>33 = VC33</td>
</tr>
<tr>
<td></td>
<td>40 = C40</td>
</tr>
</tbody>
</table>

**Temperature Range—**M

<table>
<thead>
<tr>
<th>Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>M</td>
<td>-55°C to 125°C</td>
</tr>
<tr>
<td>A</td>
<td>-40°C to 105°C (C6000)</td>
</tr>
<tr>
<td>L</td>
<td>0°C to 70°C</td>
</tr>
<tr>
<td>W</td>
<td>-55°C to 115°C</td>
</tr>
<tr>
<td>S</td>
<td>Special Per datasheet</td>
</tr>
<tr>
<td>Blank</td>
<td>25°C</td>
</tr>
</tbody>
</table>

* = Not all speed, package, process, temperature combinations are available.
First-In, First-Out Products (FIFOs)

Example: **SN54ABT36148HFPEP**

Prefix—**SN**
SN = Commercial Processing
SNJ = MIL-PRF-38535 (QML) (Class Q)

Military Temperature—**54**
54 = -55°C to 125°C
74 = 0°C to 70°C

Technology—**ABT**
ABT = Advanced BiMOS
ACT = Advanced CMOS
LS = Low-Power Schottky
HC = High Speed CMOS (CMOS Input Levels)
HCT = High Speed CMOS (TTL Input Levels)

Circuit Designator—**3614**
J, JE = Ceramic DIP (300 mil and 600 mil)
L, L20 = Ceramic Leadless Chip Carrier (CLCC)

Package Type—**3614**
J = CDIP
HFP = CFP
KGD = KGD
PCB/PN = QFP
FK = LCCC
GB = BGA Microstar

Enhanced Plastic—**EP**
TI Acquired Harris Logic

Example: **CD4XXXXXXX**

**Prefix—**CD

**Device Function (up to 5 digits)—**4XXXX

**Supply Voltage—**XX
A = 2 V Max
B = 18 V Max
UB = 18 V Max Unbuffered

**Package Designation—**X
F = Ceramic Dual In-Line Package (CDIP)
K = Ceramic Flatpack
D = Metal Seal CDIP

**Process Levels—**X
3 = Mil Temp Commercial Processing
3A = MILPRF-38535 (QML)
B = MIL-M-38510 Electrical (QPL)
**Logic**

**Example:** SNJ54ABTH162245WDEP

<table>
<thead>
<tr>
<th><strong>Prefix—SNJ</strong></th>
<th><strong>Special Features—H</strong></th>
<th><strong>Enhanced Plastic—EP</strong></th>
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</thead>
<tbody>
<tr>
<td>SNJ</td>
<td>D = Level Shifting Diode (CBTD)</td>
<td></td>
</tr>
<tr>
<td>SN</td>
<td>H = Bus Hold (LVTH)</td>
<td></td>
</tr>
</tbody>
</table>

**Type—54**

**Technology—ABT**

<table>
<thead>
<tr>
<th>Designation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ALS/AS</td>
<td>Advanced Low-Power Schottky Advanced Schottky</td>
</tr>
<tr>
<td>AHC/AHCT</td>
<td>Advanced High Speed CMOS</td>
</tr>
<tr>
<td>HC/HCT</td>
<td>High Speed CMOS</td>
</tr>
<tr>
<td>BCT</td>
<td>BiCMOS</td>
</tr>
<tr>
<td>ACT</td>
<td>Advanced CMOS</td>
</tr>
<tr>
<td>ABT</td>
<td>Advanced BiCMOS</td>
</tr>
<tr>
<td>LVC</td>
<td>Low Voltage CMOS</td>
</tr>
<tr>
<td>LVTH</td>
<td>Low Voltage Advanced CMOS w/ Bus Hold</td>
</tr>
<tr>
<td>CDC</td>
<td>Clock Distribution Circuit</td>
</tr>
<tr>
<td>CBT</td>
<td>Crossbar Bus Switch</td>
</tr>
<tr>
<td>GTL</td>
<td>Gunning Transceiver Logic</td>
</tr>
<tr>
<td>FCT</td>
<td>Fast CMOS Technology</td>
</tr>
<tr>
<td>F</td>
<td>FAST</td>
</tr>
</tbody>
</table>

**Bus/Scan Options—16**

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>SCOPE/JTAG</td>
</tr>
<tr>
<td>16</td>
<td>Widebus</td>
</tr>
<tr>
<td>18</td>
<td>SCOPE/JTAG Widebus</td>
</tr>
<tr>
<td>32</td>
<td>Widebus+</td>
</tr>
</tbody>
</table>

**Options—2**

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>Series-Damping Resistors on Outputs</td>
</tr>
</tbody>
</table>

**Device Function—245**

**Package Type—WD**

<table>
<thead>
<tr>
<th>Designation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PZ</td>
<td>LQFP</td>
</tr>
<tr>
<td>PW</td>
<td>TSSOP</td>
</tr>
<tr>
<td>DW</td>
<td>SOIC</td>
</tr>
<tr>
<td>DL</td>
<td>SSOP</td>
</tr>
<tr>
<td>D</td>
<td>SOIC</td>
</tr>
<tr>
<td>DB</td>
<td>TSSOP</td>
</tr>
<tr>
<td>DGG</td>
<td>TSSOP</td>
</tr>
<tr>
<td>DCK</td>
<td>SOP</td>
</tr>
<tr>
<td>QGL</td>
<td>BGA Microstar Junior</td>
</tr>
<tr>
<td>ZQL</td>
<td>BGA Microstar Junior</td>
</tr>
<tr>
<td>J, JT</td>
<td>CDIP</td>
</tr>
<tr>
<td>W/WD</td>
<td>Ceramic Flatpack</td>
</tr>
<tr>
<td>FK</td>
<td>Leadless Ceramic Chip Carrier</td>
</tr>
<tr>
<td>HV, HT, HFP</td>
<td>Ceramic Quad Flatpack</td>
</tr>
<tr>
<td>GB</td>
<td>Pin Grid Array (PGA)</td>
</tr>
</tbody>
</table>
Programmable Logic

Example: TIBPAL16L8-10MJB

Prefix—TIB
TIB = IMPACT™

Product Family Designator—PAL

Number of Array Inputs—16

Output Configuration Designator—L
L = Active Low
R = Registered
V = Variable (programmable)

Number of Outputs in Designated Configuration—8

Performance Designator—10
-7 = 7 ns propagation delay
-10 = 10 ns propagation delay
-12 = 12 ns propagation delay
-15 = 15 ns propagation delay
-20 = 20 ns propagation delay
-25 = 25 ns propagation delay
-30 = 30 ns propagation delay
A = Standard power
A-2 = Half power

Temperature Range—M
M = -55°C to 125°C
C = 0°C to 70°C

Package Type—J
J, JT = Ceramic Dual In-Line Package (CDIP)
FK = Leadless Ceramic Chip Carrier (LCCC)
W = Ceramic Flatpack

Processing—B
Blank = Commercial processing
B = MIL-PRF-38535 (QML)
(Class Q)
DSCC Standard Microcircuit Drawing (SMD)

Example: **5962-85155 or 8200501MFA***

**Drawing Number—5962-85155 or 82005**

**Device—01**

**Device Structure—M**
- M = Vendor self-certification to the requirements for MIL-STD-883 compliant
- Q = Certification and qualification to the MIL-PRF-38535 (Class Q)
- V = Certification and qualification to the MIL-PRF-38535 (Class V)

**Package—F**
- A = 14-pin Flatpack (1/4" x 1/4")
- B = 14-pin Flatpack (3/16" x 1/4")
- C = 14-pin DIP
- D = 14-pin Flatpack
- E = 16-pin DIP
- F = 10-pin Flatpack
- G = 8-pin Can
- H = 10-pin Flatpack
- I = 10-pin Flatpack
- J = 24-pin DIP
- K = 24-pin Flatpack
- L = 24-pin DIP (300 mil)
- M = 12-pin Can
- N = 24-pin DIP
- P = 8-pin DIP
- Q = 40-pin DIP
- R = 20-pin DIP
- S = 20-pin Flatpack
- T = 20-pad LCC
- U = 28-pad LCC
- V = 18-pin DIP
- W = 22-pin DIP
- X = Other packages
- Y = Other packages

**Lead Finish—A***
- A* = Solder Dip
- C = Gold Plate
- D = Paladium
Example: JM38510/00104BCA*

Process Level—JM38510/
Device/Slash Sheet—00104

Device Class—B

Package Type—C
A = 14-pin Flatpack (1/4" x 1/4")  I = 10-pin Flatpack  S = 20-pin Flatpack
B = 14-pin Flatpack (3/16" x 1/4")  J = 24-pin DIP  V = 18-pin DIP
C = 14-pin DIP  K = 24-pin Flatpack  W = 22-pin DIP
D = 14-pin Flatpack  L = 24-pin DIP (300 mil)  2 = 20-pad LCC
E = 16-pin DIP  M = 12-pin Can  3 = 28-pad LCC
F = 16-pin Flatpack  P = 8-pin DIP  X = Other packages
G = 8-pin Can  Q = 40-pin DIP  Y = Other packages
H = 10-pin Flatpack  R = 20-pin DIP

* Solder dip lead finish normally supplied by TI. Lead finish options must be specified by ordering the DSCC SMD number.

Lead Finish—A*
A* = Solder Dip
C = Gold Plate
D = Palladium
Process Flows

Things to Consider
Several process flows are available for TI Military Products. The flows are typical and may vary depending on changes to applicable military standards, such as MIL-PRF-38535.

QML products, processed to MIL-PRF-38535 level Q, are offered in three different types:

JM38510
Processed under MIL-PRF-38535 and electrically tested to the JAN slash sheet.

DSCC/SMD
Processed under MIL-PRF-38535 and electrically tested to the DSCC standard microcircuit drawing.
- SMQ - Processed under MIL-PRF-38535 Class N (Order by SMD)
- SMV - Processed under MIL-PRF-38535 Class V (Order by SMD)

SNJ/SMJ
Processed under MIL-PRF-38535 (Class Q) and electrically tested to the TI data sheet. All QML products are symbolized with the Q quality designator on the top side.

Enhanced Plastic
Testing and screening of EP products is performed in accordance with the TI data sheet for that device. Configuration control is performed by Texas Instruments. TI processes EP products per “best commercial practices” to the TI internal baseline flow. Processing and screening is documented in the TI Quality System Manual and is in compliance with ISO9001.

<table>
<thead>
<tr>
<th>Process Flows (See Note A)</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DSCC/SMD</td>
<td>Standard Microcircuit Drawing products processed to a MIL-PRF-38535 flow. Electricals controlled by SMD/DSCC.</td>
</tr>
<tr>
<td>SNJ/SMJ</td>
<td>Products processed to MIL-PRF-38535 Level B for military applications. Electricals controlled by current TI data sheet.</td>
</tr>
<tr>
<td>SMX/SMX*</td>
<td>Commercial level ceramic processing. Test flow defined in this section. Electricals defined by current TI data sheet but may not be production tested.</td>
</tr>
<tr>
<td>SMP*/SNF*</td>
<td>Experimental products assembled and tested by Military Products prior to qualification. No minimum screening or testing required. Electricals controlled by current TI data sheet.</td>
</tr>
<tr>
<td>JAN</td>
<td>Processed per QML MIL-PRF-38535 flow. Electricals controlled by JAN slash sheet.</td>
</tr>
</tbody>
</table>

* These devices have not met or completed TI Military Semiconductors internal qualification requirements. These devices are for prototyping purposes only and standard TI warranties do not apply. Supply of these devices does not constitute a commitment by TI to release them to production.

NOTE A: While TI offers SCDs, it is not the standard or preferred method of procurement.
QML Processing Flow Covering DS CC, SMD, SNJ, SMJ and JAN (See Note A)

- Wafer Fab Certification DS CC/TRB
- Certified Manufacturing Lines DS CC/TRB
- Wafer Fabrication & Device Assembly
- Traceability to Diffusion Lot
- Internal Visual, Method 2010, Condition B
- Bond Full & Die Shear (Sampled), Method 2011, Method 2019, Condition D
- Sealing
- Topside Symbol

- Temperature Cycle, Method 1010, Condition C
- Constant Acceleration
- Optional Pre-Burn-In, Electrical Parameters
- Burn-In Test, Method 1015, Condition A or D (See Note C)
- Post Burn-In Electrical Parameters
- Percent Defective Allowable (POA) Calculation

- Final Electrical Test (See Note B)
- Quality Conformance Inspection, Group A (Method 5005), Sample Size = 116/0
- Fine/Gross Leak Detection, Method 1014, Condition A/B and C (See Note D)
- External Visual, Method 2009
- Group B, Method 5005
- Group C, Method 5005
- Group D, Method 5005
**Process Flows**

**SN/SM Processing Flow**

1. Assembly
2. Topside Symbol
3. Burn-in (Optional)
4. Final Electrical Test (See Note F)
5. Fine/Gross Leak Detection, Method 1014, Condition A/B and C (See Note G)

**NOTE A:** Per MIL-PRF-38535, if sufficient quality and reliability data is available, the manufacturer, through the QML program and the Technical Review Board may modify, substitute or delete tests.

**NOTE B:** According to device type, electrical parameters are defined by the slash sheet, DSCC/SMD, or TI data sheet and Method 5084.

**NOTE C:** Condition A or D at manufacturer's option

**NOTE D:** Ceramic packages only

**NOTE E:** Lead finish options must be specified by ordering the DSCC SMD number

**NOTE F:** Contact the Product Information Center (PIC) for detailed test information.

**NOTE G:** Ceramic packages only.

**NOTE H:** Lead finish may vary. For example, ceramic PGA and ceramic QIP packages may be gold finish. Contact the PIC for detailed information.

---

**ESD Markings (Optional)**

<table>
<thead>
<tr>
<th>MIL-PRF-38535 ESD Class Designation</th>
<th>Marking</th>
<th>ESD Voltage Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1 Triangle</td>
<td>0 - 1999 V</td>
</tr>
<tr>
<td>2</td>
<td>2 Triangles</td>
<td>2000 - 3999 V</td>
</tr>
<tr>
<td>3</td>
<td>No Triangles</td>
<td>4000 V</td>
</tr>
</tbody>
</table>

*As referred to above, ESD marking is optional.*
Process Flows

Offshore Class V Process Flow (Texas Instruments/Unitrode)

- Wafer Fab Acceptance
- SPC Bond Process Monitor
- 100%/100X Internal Visual, Method 2010, Condition A
- Temperature Cycling Cond C, 50 Cycles, Centrifuge Condition E
- PIND, 100, 0 rejects or 5 cycles
- Serialization (Symbol) 100%
- X-ray Monitor, Real-time Video Inspection
- Pre Burn-in Electrical Test (as required)
- Burn-in 240 Hr
- Post Burn-in 240 Hr
- Post Burn-in Electricals, PDA = 3%
- 100% High/Low Electricals
- Quality Conformance Inspection (QCI), Group A (Method 5005) SS + 116/0
- Fine/Gross Leak Detection (Ceramic Only), Method 1014, Condition B and C
- External Visual, Method 2009
- QCI Group B and D, Group C by Wafer Lot
- Fine/Gross Leak Detection, Method 1014, Condition A/B and C (See Note D)

NOTE: Per MIL-PRF-38535, if sufficient quality and reliability data is available, the manufacturer, through the QML program and the TRB, may modify, substitute or delete tests.
## Process Flows

### Symbolization

<table>
<thead>
<tr>
<th>Example</th>
<th>Symbolization</th>
</tr>
</thead>
<tbody>
<tr>
<td>JANB 54LS161A</td>
<td>YCBF† YYWLLZ§ USA JM38510/30003BCA</td>
</tr>
<tr>
<td>SN 54LS161A</td>
<td>SN54LS161AJ 00XXY THAILAND§</td>
</tr>
<tr>
<td>SNJ 54LS161A</td>
<td>YCBF† YYWLLZ§ USA JM38510/30003BCA</td>
</tr>
<tr>
<td>SNJ With No SMD</td>
<td>SNJ54LS381J 00XXY THAILAND§</td>
</tr>
<tr>
<td>SMJ 320C30GBM40</td>
<td>SMJ320C30GBM40 or 5962-9052604MXA</td>
</tr>
<tr>
<td>UCC 1806JQMLV</td>
<td>UCC1806JQMLV 5962-9457501VEA YYWLLZ§ THAILAND§</td>
</tr>
</tbody>
</table>

- † Tobu is optional
- § ESD marking is optional
- Y = diffusion date, B = die revision
- F = wafer fab code (optional)
- S = YYWW = seal data
- L = lot number
- Z = B/I split lot
- * OSM marking denotes OML-compliant product
- # Where this is an approved source
- ○ Country of origin may be located on package underside.
For more information

www.ti.com/hirel
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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
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