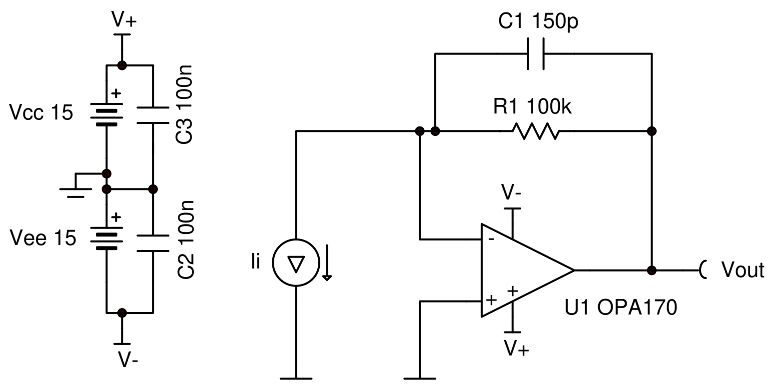
Analog Engineer's Circuit
Transimpedance Amplifier Circuit

Design Goals

Input		Output		BW	Supply	
I_{iMin}	I_{iMax}	V_{oMin}	V_{oMax}	f_p	V_{cc}	V_{ee}
0 A	50 µA	0 V	5 V	10 kHz	15 V	–15 V

Design Description

The transimpedance op amp circuit configuration converts an input current source into an output voltage. The current to voltage gain is based on the feedback resistance. The circuit is able to maintain a constant voltage bias across the input source as the input current changes which benefits many sensors.



Design Notes

1. Use a JFET or CMOS input op amp with low bias current to reduce DC errors.
2. A bias voltage can be added to the non-inverting input to set the output voltage for 0 A input currents.
3. Operate within the linear output voltage swing (see A_{ol} specification) to minimize non-linearity errors.

Design Steps

1. Select the gain resistor.

$$R_1 = \frac{V_{oMax} - V_{oMin}}{I_{iMax}} = \frac{5V - 0V}{50\mu A} = 100k\Omega$$

2. Select the feedback capacitor to meet the circuit bandwidth.

$$C_1 \le \frac{1}{2 \times \pi \times R_1 \times f_p}$$

$$C_1 \le \frac{1}{2 \times \pi \times 100k\Omega \times 10kHz} \le 159pF \approx 150pF \text{ (Standard Value)}$$

3. Calculate the necessary op amp gain bandwidth (GBW) for the circuit to be stable.

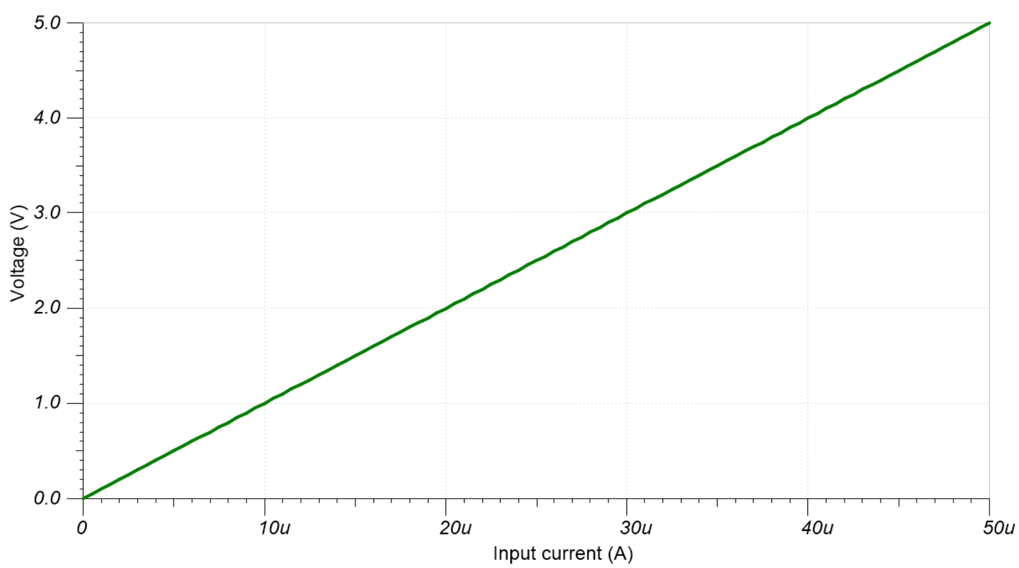
$$GBW > \frac{C_i + C_1}{2 \times \pi \times R_1 \times {C_1}^2} > \frac{6pF + 150pF}{2 \times \pi \times 100k\Omega \times (150pF)^2} > 11.03kHz$$

$$\text{where } C_i = C_s + C_d + C_{cm} = 0pF + 3pF + 3pF = 6pF \text{ given}$$

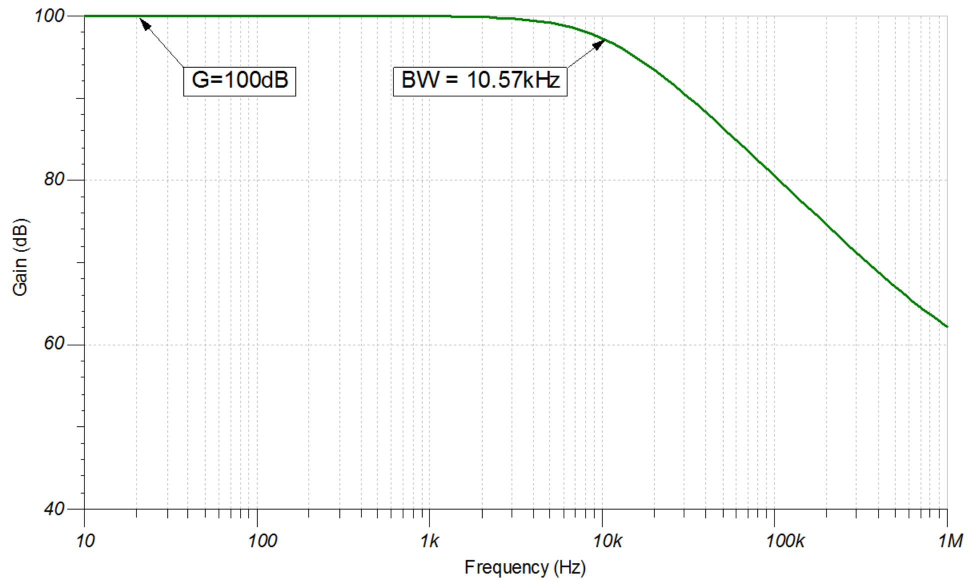
- C_s: Input source capacitance
- C_d: Differential input capacitance of the amplifier
- C_{cm}: Common-mode input capacitance of the inverting input

Design Simulations

DC Simulation Results



AC Simulation Results



Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See circuit SPICE simulation file SBOC501.

See TIPD176.

Design Featured Op Amp

OPA170	
V_{cc}	2.7 V to 36 V
V_{inCM}	(V_{ee}–0.1 V) to (V_{cc} –2 V)
V_{out}	Rail–to–rail
V_{os}	0.25 mV
I_q	0.11 mA
I_b	8 pA
UGBW	1.2 MHz
SR	0.4 V/µs
#Channels	1, 2, and 4
OPA170	

Design Alternate Op Amp

OPA1671	
V_{cc}	1.7 V to 5.5 V
V_{inCM}	Rail–to–rail
V_{out}	(V_{ee}+10 mV) to (V_{cc}-10 mV) at 275 µA
V_{os}	250 µV
I_q	940 µA
I_b	1 pA
UGBW	12 MHz
SR	5 V/µs
#Channels	1
OPA1671	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from February 1, 2018 to February 1, 2019	Page
• Downscale the title and changed title role to 'Amplifiers'. Updated *Design Alternate Op Amp* table with OPA1671. Added link to circuit cookbook landing page.	1

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