1 Overview

This document contains information for INA180-Q1 (SOT-23-5 package) and INA181-Q1 (SOT-23-6 package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1 and Figure 2 show the device functional block diagrams for reference.

**Figure 1. INA180-Q1 Functional Block Diagram**

**Figure 2. INA181-Q1 Functional Block Diagram**

INA180-Q1, INA181-Q1 were developed using a quality-managed development process, but were not developed in accordance with the IEC 61508 or ISO 26262 standards.
2 Functional Safety Failure In Time (FIT) Rates

2.1 INA180-Q1, SOT-23-5 Package

This section provides Functional Safety Failure In Time (FIT) rates for the SOT-23-5 package of INA180-Q1 based on two different industry-wide used reliability standards:

- **Table 1** provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- **Table 2** provides FIT rates based on the Siemens Norm SN 29500-2

### Table 1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

<table>
<thead>
<tr>
<th>Category</th>
<th>FIT IEC TR 62380 / ISO 26262</th>
<th>FIT (Failures Per 10^9 Hours)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total Component FIT Rate</td>
<td>4</td>
<td></td>
</tr>
<tr>
<td>Die FIT Rate</td>
<td></td>
<td>2</td>
</tr>
<tr>
<td>Package FIT Rate</td>
<td></td>
<td>2</td>
</tr>
</tbody>
</table>

The failure rate and mission profile information in **Table 1** comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Automotive Control
- Power dissipation: 10 mW
- Climate type: World-wide Table 8
- Package factor: Lambda 3 Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

### Table 2. Component Failure Rates per Siemens Norm SN 29500-2

<table>
<thead>
<tr>
<th>Table</th>
<th>Category</th>
<th>Reference FIT Rate</th>
<th>Reference Virtual T&lt;sub&gt;j&lt;/sub&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>CMOS, Op amp, comparators, voltage monitors</td>
<td>8 FIT</td>
<td>45°C</td>
</tr>
</tbody>
</table>

The Reference FIT Rate and Reference Virtual T<sub>j</sub> (junction temperature) in **Table 2** come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.
2.2 **INA181-Q1, SOT-23-6 Package**

This section provides Functional Safety Failure In Time (FIT) rates for the SOT-23-6 package of INA181-Q1 based on two different industry-wide used reliability standards:

- **Table 3** provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- **Table 4** provides FIT rates based on the Siemens Norm SN 29500-2

### Table 3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

<table>
<thead>
<tr>
<th>FIT IEC TR 62380 / ISO 26262</th>
<th>FIT (Failures Per 10^9 Hours)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total Component FIT Rate</td>
<td>4</td>
</tr>
<tr>
<td>Die FIT Rate</td>
<td>2</td>
</tr>
<tr>
<td>Package FIT Rate</td>
<td>2</td>
</tr>
</tbody>
</table>

The failure rate and mission profile information in **Table 3** comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Automotive Control
- Power dissipation: 10 mW
- Climate type: World-wide Table 8
- Package factor: Lambda 3 Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

### Table 4. Component Failure Rates per Siemens Norm SN 29500-2

<table>
<thead>
<tr>
<th>Table</th>
<th>Category</th>
<th>Reference FIT Rate</th>
<th>Reference Virtual T&lt;sub&gt;j&lt;/sub&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>CMOS Op amp, comparators, voltage monitors</td>
<td>8 FIT</td>
<td>45°C</td>
</tr>
</tbody>
</table>

The Reference FIT Rate and Reference Virtual T<sub>j</sub> (junction temperature) in **Table 4** come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.
3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for INA180-Q1, INA181-Q1 in Table 5 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 5. Die Failure Modes and Distribution

<table>
<thead>
<tr>
<th>Die Failure Modes</th>
<th>Failure Mode Distribution (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>OUT open (Hi-Z)</td>
<td>10%</td>
</tr>
<tr>
<td>OUT to GND</td>
<td>20%</td>
</tr>
<tr>
<td>OUT to VS</td>
<td>15%</td>
</tr>
<tr>
<td>OUT functional, not in specification</td>
<td>50%</td>
</tr>
<tr>
<td>Pin to pin short, any two pins</td>
<td>5%</td>
</tr>
</tbody>
</table>
4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the INA180-Q1 (SOT-23-5 package) and INA181-Q1 (SOT-23-6 package). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 7, Table 11 and Table 15)
- Pin open-circuited (see Table 8, Table 12 and Table 16)
- Pin short-circuited to an adjacent pin (see Table 9, Table 13 and Table 17)
- Pin short-circuited to VS (see Table 10, Table 14 and Table 18)

Table 7 through Table 14 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 6.

Table 6. TI Classification of Failure Effects

<table>
<thead>
<tr>
<th>Class</th>
<th>Failure Effects</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>Potential device damage that affects functionality</td>
</tr>
<tr>
<td>B</td>
<td>No device damage, but loss of functionality</td>
</tr>
<tr>
<td>C</td>
<td>No device damage, but performance degradation</td>
</tr>
<tr>
<td>D</td>
<td>No device damage, no impact to functionality or performance</td>
</tr>
</tbody>
</table>

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- T_A = -40°C to +125°C
- V_S = 2.7 V to 5.5 V
- V_IN+ = 12 V
- V_REF = V_S / 2 (INA181-Q1 only)

4.1 INA180-Q1, SOT-23-5 Package (Pinout A)

Figure 3 shows the INA180-Q1 pin diagram for the SOT-23-5 package (pinout A). For a detailed description of the device pins please refer to the ‘Pin Configuration and Functions’ section in the INA180-Q1 datasheet.

Figure 3. INA180-Q1 Pin Diagram (SOT-23-5 Package, Pinout A)
### Table 7. Pin FMA for Device Pins Short-Circuited to Ground

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin No.</th>
<th>Description of Potential Failure Effect(s)</th>
<th>Failure Effect Class</th>
</tr>
</thead>
<tbody>
<tr>
<td>OUT</td>
<td>1</td>
<td>Output will be pulled down to GND and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.</td>
<td>B</td>
</tr>
<tr>
<td>GND</td>
<td>2</td>
<td>Normal operation.</td>
<td>D</td>
</tr>
<tr>
<td>IN+</td>
<td>3</td>
<td>In high-side configuration, a short from the bus supply to GND will occur.</td>
<td>B</td>
</tr>
<tr>
<td>IN-</td>
<td>4</td>
<td>In high-side configuration, a short from the bus supply to GND will occur (through $R_{SHUNT}$). High current will flow from bus supply to GND. The shunt may be damaged. In low-side configuration, normal operation.</td>
<td>B for high-side; D for low-side</td>
</tr>
<tr>
<td>VS</td>
<td>5</td>
<td>Power supply shorted to GND.</td>
<td>B</td>
</tr>
</tbody>
</table>

### Table 8. Pin FMA for Device Pins Open-Circuited

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin No.</th>
<th>Description of Potential Failure Effect(s)</th>
<th>Failure Effect Class</th>
</tr>
</thead>
<tbody>
<tr>
<td>OUT</td>
<td>1</td>
<td>Output can be left open. There is no effect on the IC, but the output will not be measured.</td>
<td>C</td>
</tr>
<tr>
<td>GND</td>
<td>2</td>
<td>When GND is floating, output will be incorrect as it is no longer referenced to GND.</td>
<td>B</td>
</tr>
<tr>
<td>IN+</td>
<td>3</td>
<td>Shunt resistor is not connected to amplifier. IN+ pin may float to an unknown value. Output will go to an unknown value not to exceed VS or GND.</td>
<td>B</td>
</tr>
<tr>
<td>IN-</td>
<td>4</td>
<td>Shunt resistor is not connected to amplifier. IN- pin may float to an unknown value. Output will go to an unknown value not to exceed VS or GND.</td>
<td>B</td>
</tr>
<tr>
<td>VS</td>
<td>5</td>
<td>No power to device. Device may be biased through inputs. Output will be incorrect and close to GND.</td>
<td>B</td>
</tr>
</tbody>
</table>
Table 9. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin No.</th>
<th>Shorted to</th>
<th>Description of Potential Failure Effect(s)</th>
<th>Failure Effect Class</th>
</tr>
</thead>
<tbody>
<tr>
<td>OUT</td>
<td>1</td>
<td>2 - GND</td>
<td>Output will be pulled down to GND and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating, could cause die junction temperature to exceed 150°C.</td>
<td>B</td>
</tr>
<tr>
<td>GND</td>
<td>2</td>
<td>3 - IN+</td>
<td>In high-side configuration, a short from the bus supply to GND will occur.</td>
<td>B</td>
</tr>
<tr>
<td>IN+</td>
<td>3</td>
<td>4 - IN-</td>
<td>Inputs shorted together, so no sense voltage applied. Output will stay close to GND.</td>
<td>B</td>
</tr>
<tr>
<td>IN-</td>
<td>4</td>
<td>5 - VS</td>
<td>In high-side configuration, device power supply shorted to bus supply (through R&lt;sub&gt;SHUNT&lt;/sub&gt;). In low-side configuration, device power supply shorted to GND.</td>
<td>A for high-side; B for low-side</td>
</tr>
<tr>
<td>VS</td>
<td>5</td>
<td>1 - OUT</td>
<td>When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.</td>
<td>B</td>
</tr>
</tbody>
</table>

Table 10. Pin FMA for Device Pins Short-Circuited to VS

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin No.</th>
<th>Description of Potential Failure Effect(s)</th>
<th>Failure Effect Class</th>
</tr>
</thead>
<tbody>
<tr>
<td>OUT</td>
<td>1</td>
<td>Output will be pulled to VS and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.</td>
<td>B</td>
</tr>
<tr>
<td>GND</td>
<td>2</td>
<td>Power supply shorted to GND.</td>
<td>B</td>
</tr>
<tr>
<td>IN+</td>
<td>3</td>
<td>In high-side configuration, device power supply shorted to bus supply. In low-side configuration, device power supply shorted to GND (through R&lt;sub&gt;SHUNT&lt;/sub&gt;).</td>
<td>A for high-side; B for low-side</td>
</tr>
<tr>
<td>IN-</td>
<td>4</td>
<td>In high-side configuration, device power supply shorted to bus supply (through R&lt;sub&gt;SHUNT&lt;/sub&gt;). In low-side configuration, device power supply shorted to GND.</td>
<td>A for high-side; B for low-side</td>
</tr>
<tr>
<td>VS</td>
<td>5</td>
<td>Normal operation.</td>
<td>D</td>
</tr>
</tbody>
</table>
4.2 INA180-Q1, SOT-23-5 Package (Pinout B)

Figure 4 shows the INA180-Q1 pin diagram for the SOT-23-5 package (pinout B). For a detailed description of the device pins please refer to the ‘Pin Configuration and Functions’ section in the INA180-Q1 datasheet.

![INA180-Q1 Pin Diagram](image)

Figure 4. INA180-Q1 Pin Diagram (SOT-23-5 Package, Pinout B)

Table 11. Pin FMA for Device Pins Short-Circuited to Ground

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin No.</th>
<th>Description of Potential Failure Effect(s)</th>
<th>Failure Effect Class</th>
</tr>
</thead>
<tbody>
<tr>
<td>IN+</td>
<td>1</td>
<td>In high-side configuration, a short from the bus supply to GND will occur.</td>
<td>B</td>
</tr>
<tr>
<td>GND</td>
<td>2</td>
<td>Normal operation.</td>
<td>D</td>
</tr>
<tr>
<td>IN-</td>
<td>3</td>
<td>In high-side configuration, a short from the bus supply to GND will occur (through $R_{\text{SHUNT}}$). High current will flow from bus supply to GND. The shunt may be damaged. In low-side configuration, normal operation.</td>
<td>B for high-side; D for low-side</td>
</tr>
<tr>
<td>OUT</td>
<td>4</td>
<td>Output will be pulled down to GND and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.</td>
<td>B</td>
</tr>
<tr>
<td>VS</td>
<td>5</td>
<td>Power supply shorted to GND.</td>
<td>B</td>
</tr>
</tbody>
</table>
### Table 12. Pin FMA for Device Pins Open-Circuited

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin No.</th>
<th>Description of Potential Failure Effect(s)</th>
<th>Failure Effect Class</th>
</tr>
</thead>
<tbody>
<tr>
<td>IN+</td>
<td>1</td>
<td>Shunt resistor is not connected to amplifier. IN+ pin may float to an unknown value. Output will go to an unknown value not to exceed VS or GND.</td>
<td>B</td>
</tr>
<tr>
<td>GND</td>
<td>2</td>
<td>When GND is floating, output will be incorrect as it is no longer referenced to GND.</td>
<td>B</td>
</tr>
<tr>
<td>IN-</td>
<td>3</td>
<td>Shunt resistor is not connected to amplifier. IN- pin may float to an unknown value. Output will go to an unknown value not to exceed VS or GND.</td>
<td>B</td>
</tr>
<tr>
<td>OUT</td>
<td>4</td>
<td>Output can be left open. There is no effect on the IC, but the output will not be measured.</td>
<td>C</td>
</tr>
<tr>
<td>VS</td>
<td>5</td>
<td>No power to device. Device may be biased through inputs. Output will be incorrect and close to GND.</td>
<td>B</td>
</tr>
</tbody>
</table>

### Table 13. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin No.</th>
<th>Shorted to</th>
<th>Description of Potential Failure Effect(s)</th>
<th>Failure Effect Class</th>
</tr>
</thead>
<tbody>
<tr>
<td>IN+</td>
<td>1</td>
<td>2 - GND</td>
<td>In high-side configuration, a short from the bus supply to GND will occur.</td>
<td>B</td>
</tr>
<tr>
<td>GND</td>
<td>2</td>
<td>3 - IN-</td>
<td>In high-side configuration, a short from the bus supply to GND will occur (through R\text{SHUNT}). High current will flow from bus supply to GND. The shunt may be damaged. In low-side configuration, normal operation.</td>
<td>B for high-side; D for low-side</td>
</tr>
<tr>
<td>IN-</td>
<td>3</td>
<td>4 - OUT</td>
<td>In high-side configuration, OUT pin shorted to bus supply. In low side configuration, output is shorted to GND.</td>
<td>A for high-side; B for low-side</td>
</tr>
<tr>
<td>OUT</td>
<td>4</td>
<td>5 - VS</td>
<td>Output will be pulled to VS and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.</td>
<td>B</td>
</tr>
<tr>
<td>VS</td>
<td>5</td>
<td>1 - IN+</td>
<td>In high-side configuration, device power supply shorted to bus supply. In low-side configuration, device power supply shorted to GND (through R\text{SHUNT}).</td>
<td>A for high-side; B for low-side</td>
</tr>
<tr>
<td>Pin Name</td>
<td>Pin No.</td>
<td>Description of Potential Failure Effect(s)</td>
<td>Failure Effect Class</td>
<td></td>
</tr>
<tr>
<td>---------</td>
<td>--------</td>
<td>-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------</td>
<td>----------------------</td>
<td></td>
</tr>
<tr>
<td>IN⁺</td>
<td>1</td>
<td>In high-side configuration, device power supply shorted to bus supply. In low-side configuration, device power supply shorted to GND (through R_{SHUNT}).</td>
<td>A for high-side; B for low-side</td>
<td></td>
</tr>
<tr>
<td>GND</td>
<td>2</td>
<td>Power supply shorted to GND.</td>
<td>B</td>
<td></td>
</tr>
<tr>
<td>IN⁻</td>
<td>3</td>
<td>In high-side configuration, device power supply shorted to bus supply (through R_{SHUNT}). In low-side configuration, device power supply shorted to GND.</td>
<td>A for high-side; B for low-side</td>
<td></td>
</tr>
<tr>
<td>OUT</td>
<td>4</td>
<td>Output will be pulled to VS and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.</td>
<td>B</td>
<td></td>
</tr>
<tr>
<td>VS</td>
<td>5</td>
<td>Normal operation.</td>
<td>D</td>
<td></td>
</tr>
</tbody>
</table>
4.3 **INA181-Q1, SOT-23-6 Package**

Figure 5 shows the INA181-Q1 pin diagram for the SOT-23-6 package. For a detailed description of the device pins please refer to the 'Pin Configuration and Functions' section in the INA181-Q1 datasheet.

![INA181-Q1 Pin Diagram (SOT-23-6 Package)](image)

**Figure 5. INA181-Q1 Pin Diagram (SOT-23-6 Package)**

**Table 15. Pin FMA for Device Pins Short-Circuited to Ground**

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin No.</th>
<th>Description of Potential Failure Effect(s)</th>
<th>Failure Effect Class</th>
</tr>
</thead>
<tbody>
<tr>
<td>OUT</td>
<td>1</td>
<td>Output will be pulled down to GND and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.</td>
<td>B</td>
</tr>
<tr>
<td>GND</td>
<td>2</td>
<td>Normal operation.</td>
<td>D</td>
</tr>
<tr>
<td>IN+</td>
<td>3</td>
<td>In high-side configuration, a short from the bus supply to GND will occur.</td>
<td>B</td>
</tr>
<tr>
<td>IN-</td>
<td>4</td>
<td>In high-side configuration, a short from the bus supply to GND will occur (through $R_{SHUNT}$). High current will flow from bus supply to GND. The shunt may be damaged. In low-side configuration, normal operation.</td>
<td>B for high-side; D for low-side</td>
</tr>
<tr>
<td>REF</td>
<td>5</td>
<td>Normal operation if REF pin is at GND potential by design; otherwise the system measurement will be incorrect.</td>
<td>D if REF=GND by design; C otherwise</td>
</tr>
<tr>
<td>VS</td>
<td>6</td>
<td>Power supply shorted to GND.</td>
<td>B</td>
</tr>
</tbody>
</table>
### Table 16. Pin FMA for Device Pins Open-Circuited

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin No.</th>
<th>Description of Potential Failure Effect(s)</th>
<th>Failure Effect Class</th>
</tr>
</thead>
<tbody>
<tr>
<td>OUT</td>
<td>1</td>
<td>Output can be left open. There is no effect on the IC, but the output will not be measured.</td>
<td>C</td>
</tr>
<tr>
<td>GND</td>
<td>2</td>
<td>When GND is floating, output will be incorrect as it is no longer referenced to GND.</td>
<td>B</td>
</tr>
<tr>
<td>IN+</td>
<td>3</td>
<td>Shunt resistor is not connected to amplifier. IN+ pin may float to an unknown value. Output will go to an unknown value not to exceed VS or GND.</td>
<td>B</td>
</tr>
<tr>
<td>IN-</td>
<td>4</td>
<td>Shunt resistor is not connected to amplifier. IN- pin may float to an unknown value. Output will go to an unknown value not to exceed VS or GND.</td>
<td>B</td>
</tr>
<tr>
<td>REF</td>
<td>5</td>
<td>Output common-mode voltage is not defined. Output will not maintain a linear relationship with differential input voltage.</td>
<td>B</td>
</tr>
<tr>
<td>VS</td>
<td>6</td>
<td>No power to device. Device may be biased through inputs. Output will be incorrect and close to GND.</td>
<td>B</td>
</tr>
</tbody>
</table>

### Table 17. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin No.</th>
<th>Shorted to</th>
<th>Description of Potential Failure Effect(s)</th>
<th>Failure Effect Class</th>
</tr>
</thead>
<tbody>
<tr>
<td>OUT</td>
<td>1</td>
<td>2 - GND</td>
<td>Output will be pulled down to GND and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.</td>
<td>B</td>
</tr>
<tr>
<td>GND</td>
<td>2</td>
<td>3 - IN+</td>
<td>In high-side configuration, a short from the bus supply to GND will occur.</td>
<td>B</td>
</tr>
<tr>
<td>IN+</td>
<td>3</td>
<td>4 - IN-</td>
<td>Inputs shorted together, so no sense voltage applied. Output will stay close to REF potential.</td>
<td>B</td>
</tr>
<tr>
<td>IN-</td>
<td>4</td>
<td>5 - REF</td>
<td>In high-side configuration, REF shorted to bus supply. In low-side configuration, REF shorted to GND (normal operation if REF is at GND potential by design).</td>
<td>A for high-side; C for low-side (D if REF=GND by design)</td>
</tr>
<tr>
<td>REF</td>
<td>5</td>
<td>6 - VS</td>
<td>Normal operation if REF pin is at VS potential by design; otherwise the system measurement will be incorrect.</td>
<td>D if REF=VS by design; C otherwise</td>
</tr>
<tr>
<td>VS</td>
<td>6</td>
<td>1 - OUT</td>
<td>Output will be pulled to VS and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.</td>
<td>B</td>
</tr>
</tbody>
</table>
Table 18. Pin FMA for Device Pins Short-Circuited to VS

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin No.</th>
<th>Description of Potential Failure Effect(s)</th>
<th>Failure Effect Class</th>
</tr>
</thead>
<tbody>
<tr>
<td>OUT</td>
<td>1</td>
<td>Output will be pulled to VS and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.</td>
<td>B</td>
</tr>
<tr>
<td>GND</td>
<td>2</td>
<td>Power supply shorted to GND.</td>
<td>B</td>
</tr>
<tr>
<td>IN+</td>
<td>3</td>
<td>In high-side configuration, device power supply shorted to bus supply. In low-side configuration, device power supply shorted to GND (through $R_{SHUNT}$).</td>
<td>A for high-side; B for low-side</td>
</tr>
<tr>
<td>IN-</td>
<td>4</td>
<td>In high-side configuration, device power supply shorted to bus supply (through $R_{SHUNT}$). In low-side configuration, device power supply shorted to GND.</td>
<td>A for high-side; B for low-side</td>
</tr>
<tr>
<td>REF</td>
<td>5</td>
<td>Normal operation if REF pin is at VS potential by design; otherwise the system measurement will be incorrect.</td>
<td>D if REF=VS by design; C otherwise</td>
</tr>
<tr>
<td>VS</td>
<td>6</td>
<td>Normal operation.</td>
<td>D</td>
</tr>
</tbody>
</table>
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