Application Note
SCAA045 - November 2000

Design and Layout Guidelines for the CDCVF2505 Clock Driver

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ABSTRACT

This application note describes tuning techniques, line termination methods, and filter circuit for the CDCVF2505, and it provides PCB layout guidelines.

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1 Introduction

The CDCVF2505 is a high-performance, low-skew, low-jitter, phase-lock loop (PLL) clock driver (refer to [1] for details). It uses a PLL to phase- and frequency-align the input (CLKIN) and output (1Y[0:3], CLKOUT) clock signals precisely, and it provides integrated series-damping resistors that make it ideal for driving point-to-point loads. Unlike many products containing PLLs, the CDCVF2505 does not require an external RC network; instead, the *loop* filter for the PLL is included on-chip, minimizing component count, space, and cost. As can be seen from Table 1, the CDCVF2505 has performance superior to the Cypress CY2305.

Table 1. Functional Comparison Between CDCVF2505 and CY2305

FEATURE	CDCVF2505	CY2305
Number of inputs	5	5
Package	8-pin SOIC and 8-pin TSSOP	8-pin SOIC
Frequency range	24–200 MHz	1–100/133 MHz
Cycle-to-cycle jitter at 66 MHz	< 150 ps	< 200 ps
SSC compatible	Yes	No
On-chip series damping resistors	25 Ω	No
Input-to-output propagation delay	< ±150 ps	< 350 ps
Output duty cycle	45–55%	40–60%
PLL lock time	100 µs	1 ms
Rise/fall time at 0.4–2.0 V	2.5/2.5 ns	2.5/2.5 ns
Operating temperature range	–40°C–85°C	0°C–70°C
Output skew	150 ps max.	< 250 ps
Power-down feature	Yes	No

When a PLL is used in an application, data errors can be introduced as a result of (a) signal degradation from line noise and, (b) reflections caused by improper line termination when the signal transit time through the transmission line exceeds the rise or fall time of the signal. This note provides guidelines and suggestions for avoiding noise and line termination problems. It also details tuning for zero and specified nonzero delays.

2 Tuning for Zero Delay

As shown in Figure 1, the CLKOUT pin (8) completes the feedback loop of the PLL. This connection is made inside the chip and external feedback is not required. However,CLKOUT can be loaded with a capacitor to adjust the input-to-output propagation delay. Depending on the application and the delay requirements, the designer can choose two capacitor values between 5 pF and 25 pF on CLKOUT to determine the exact propagation delay between CLKIN and Yn. Native propagation delay as a function of delta load (the difference between the CKLOUT and Yn loads) is shown in Figure 2.

When a lead-lag relationship is sought instead of a zero delay, it can be obtained by loading the feedback pin, CLKOUT. To get a positive phase error (i.e. CLKIN leads the Y outputs), the CLKOUT pin should be loaded more lightly than the Y outputs. Alternatively, for a more negative phase error (Y outputs leading the reference input CLKIN), the CLOCKOUT pin should be loaded more heavily than the Y outputs. As a rule of thumb, the adjustment is about 50 ps/pF of loading difference; thus, 1 pF will induce delay of 35–50 ps. A 1-inch trace of 50-Ω transmission line in FR-4 material has about a 3-pF parasitic capacitance, or approximately a 100-ps delay.

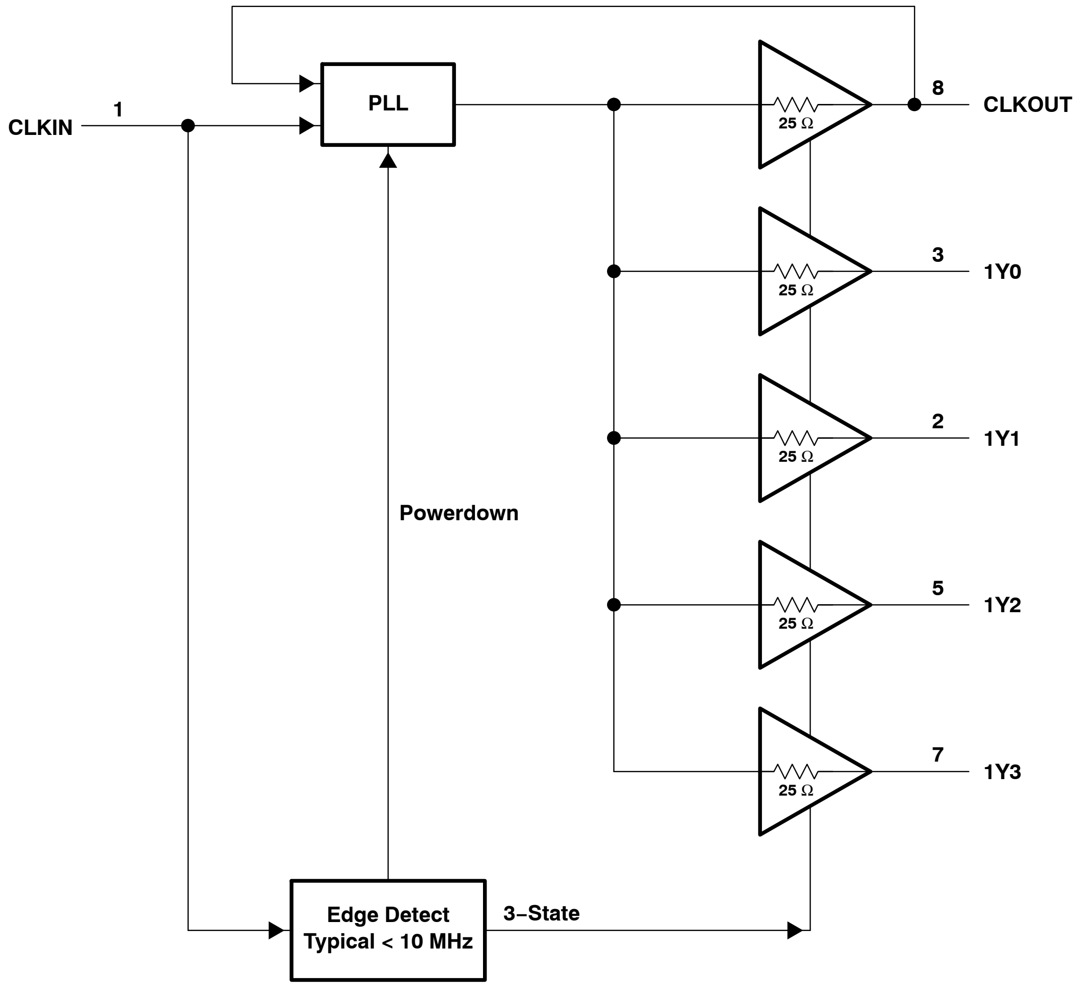


Figure 1. Functional Block Diagram of CDCVF2505

Note that adjusting the trace length of the feedback loop coarse-tunes the phase error. Adjusting the capacitive loading on the feedback is the best way to fine tune the phase error, with this loading being placed as close to the CLKOUT pin as physically possible. For example, for a phase lead (CLKIN lead Yn), the trace length of the Y outputs is increased. Conversely, increasing the trace length of the feedback path decreases the phase error and, in this case, the Yn outputs are advanced relative to the reference clock input (CLKIN).

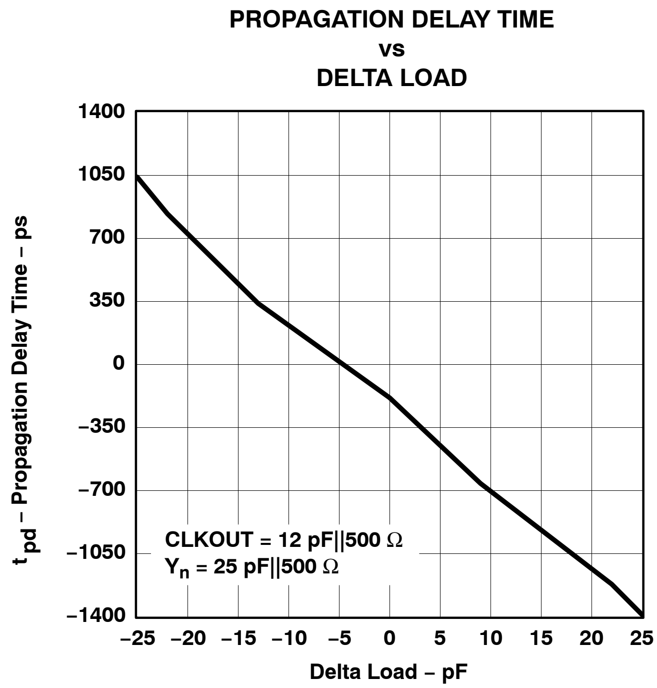


Figure 2. Delay vs Delta Load

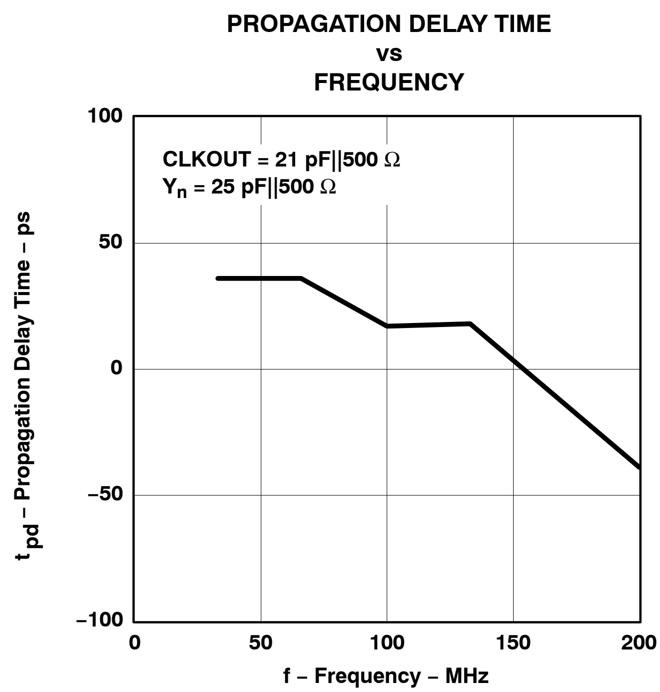


Figure 3. Tuning for Minimum Delay

3 Common Termination Techniques

As a general rule, transmission line (trace) termination is necessary when the round trip propagation time of the signal is equal to or greater than the transition (rise or fall) time of the driver; otherwise, there will be data errors caused by signal degradation, line noise, and, reflections.

Most termination methods rely on impedance matching of the line with either the source or the load. There are several termination techniques that can be used to terminate transmission lines. These are series (source), parallel, Thévenin, and ac termination. Each has its advantages and disadvantages, although ac termination has the widest general endorsement.

Excluding the series damping resistor, the typical output characteristic of the CDCVF2505 driver shown in Figure 4 is a PMOS impedance of 12 Ω and an NMOS impedance of 15 Ω. Therefore, the total output impedence of the driver when the output is high is approximately 37 Ω (12 + 25) and 40 Ω (15 + 25) when the driver is low.

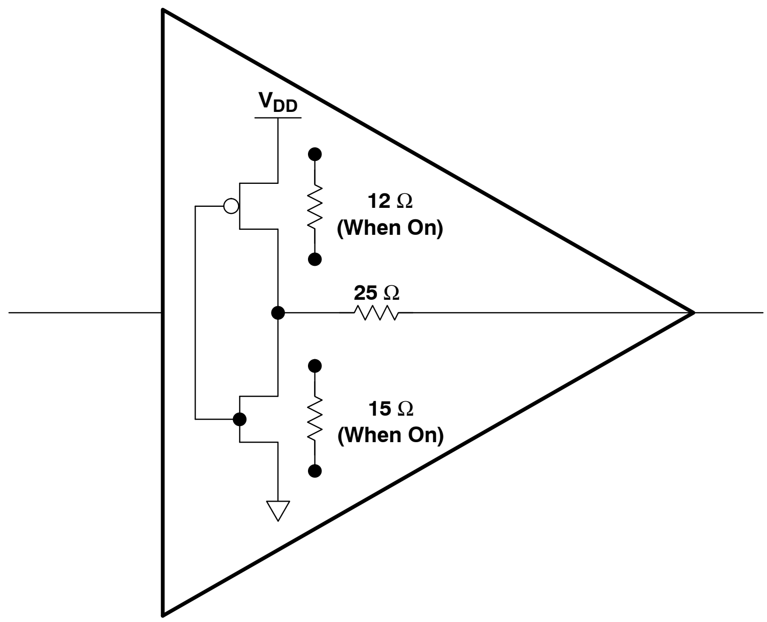


Figure 4. Driver Output Impedance

3.1 Series Termination

In series termination, a resistor is added to the outputs of the driver, thereby increasing the impedance at the line source and preventing signal reflection off the driver end. The resistor value is chosen to match the source and trace impedances. This is shown schematically in Figures 5(a) and 5(b) for single and dual transmission lines, respectively.

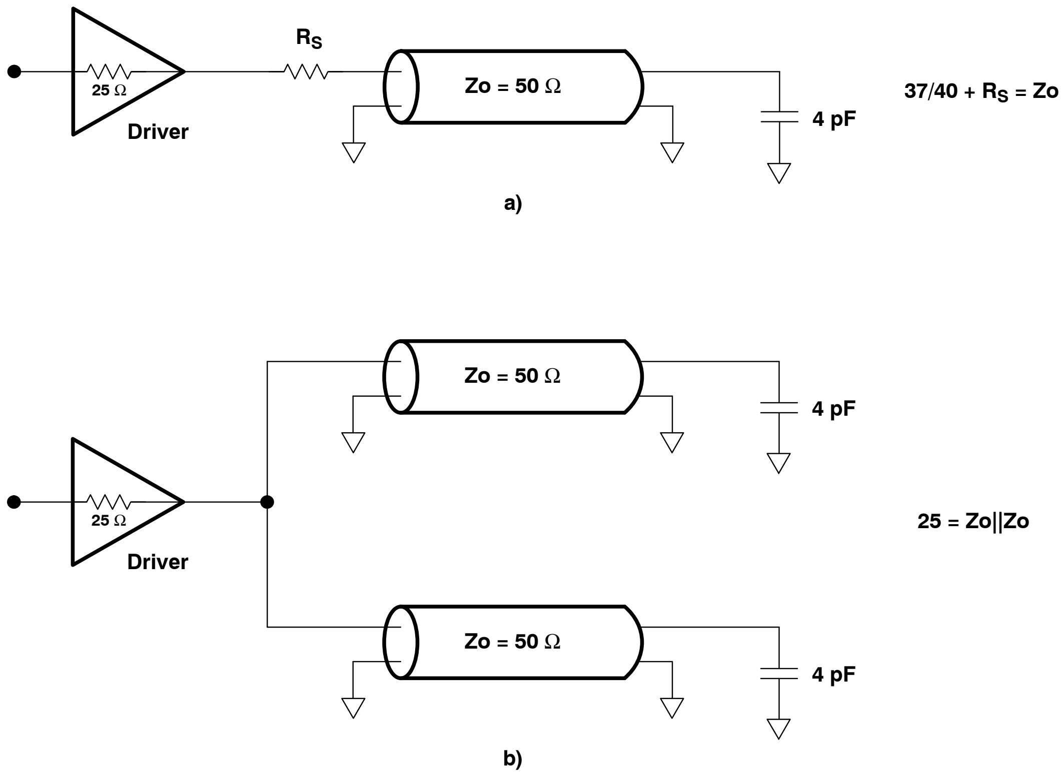


Figure 5. Series Termination

Series termination is effective in reducing the driver's edge rate, and it consumes low power. It is recommended for single receiver, point-to-point and star topologies. Series termination provides good signal quality by damping overshoot and undershoot, and effectively reducing line noise and EMI. Its drawbacks are that it slows the signal's rise and fall time, and that it should not be used with distributed loads. The CDCVF2505 can be used to drive one or two 50-Ω transmission lines each. In the dual-transmission-line case, there is no need to add any external series resistor to the outputs because the CDCVF2505 has an integrated 25-Ω resistor included on chip. Conversely, in the single-transmission-line case, an additional 25-Ω resistor should be added as close as possible to the outputs of the CDCVF2505. In both cases the CDCVF2505 provides optimal performance with minimal overshoot and undershoot, as can be seen from Figure 6. This figure shows simulated signal integrity of the output buffer at 133 MHz and a 4-pF load driving single and dual transmission lines. The plot does not reflect the actual duty cycle of the PLL; rather, the similation was done for the output buffer only. The CDCVF2505 corrects the output duty cycle of the PLL to 50%, independent of the input duty cycle.

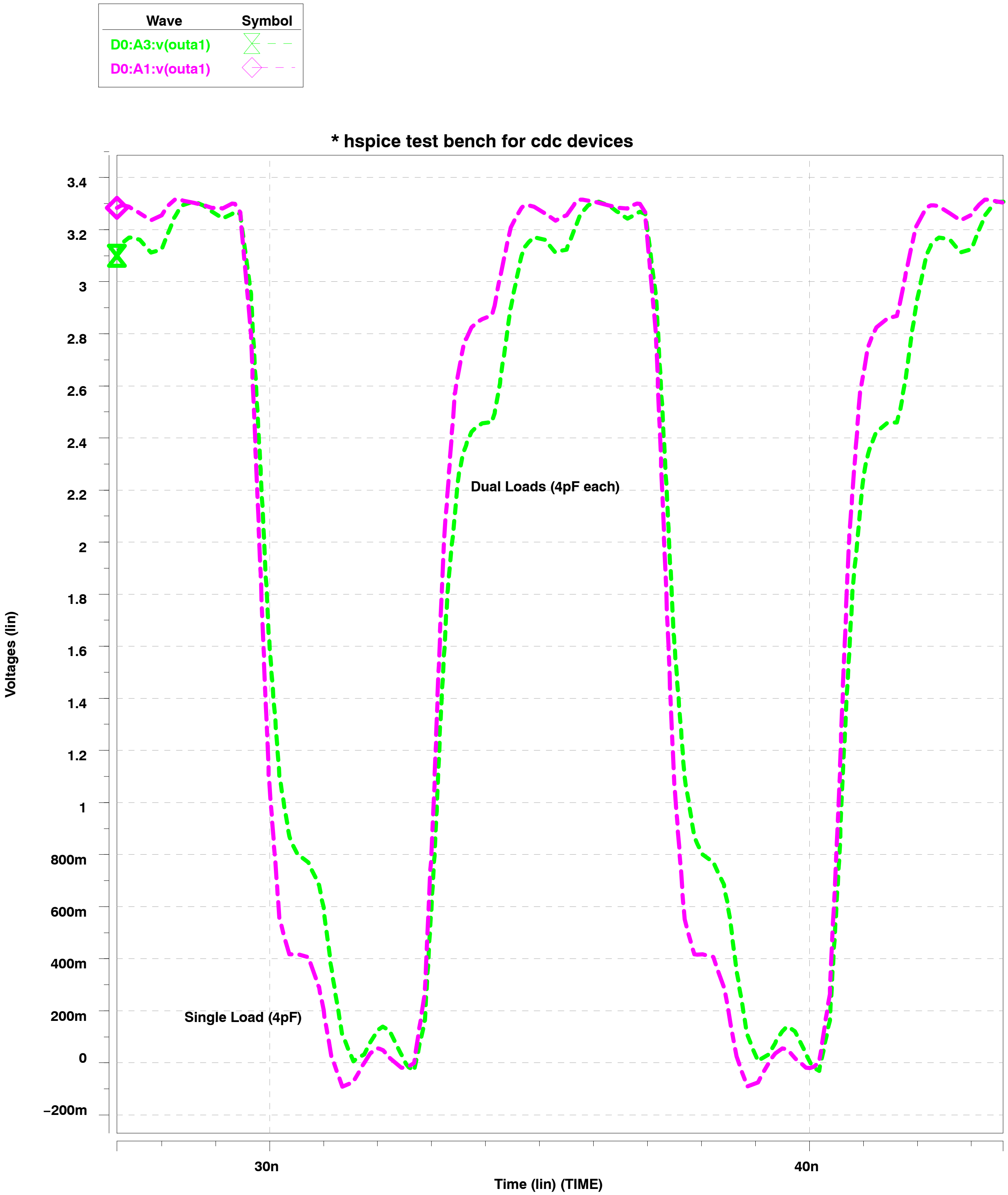


Figure 6. CDCVF2505 Output Waveforms Driving Single and Dual Loads

3.2 Parallel Termination

Parallel termination is simple to implement. It uses a single resistor at the load end of the trace, as shown in Figure 7 and, like the Thévenin and ac methods, it acts by preventing signal reflection from the load end. The value of the termination resistor should be such that the load and line impedances match. In essence, the termination resistor absorbs and dissipates energy that would otherwise reflect.

There are a few disadvantages to this method: It consumes a large amount of power, it produces unbalanced rise and fall times which result in duty cycle distortion, and it degrades the high output level of the signal.

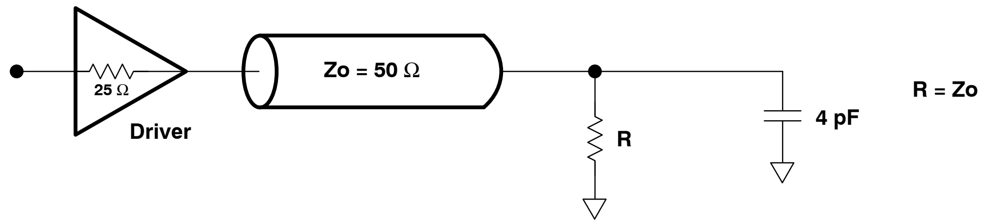


Figure 7. Parallel Termination

3.3 Thévenin Termination

Thévenin termination uses two load-end resistors whose parallel combination must result in matching between the load and trace impedances. This is shown schematically in Figure 8.

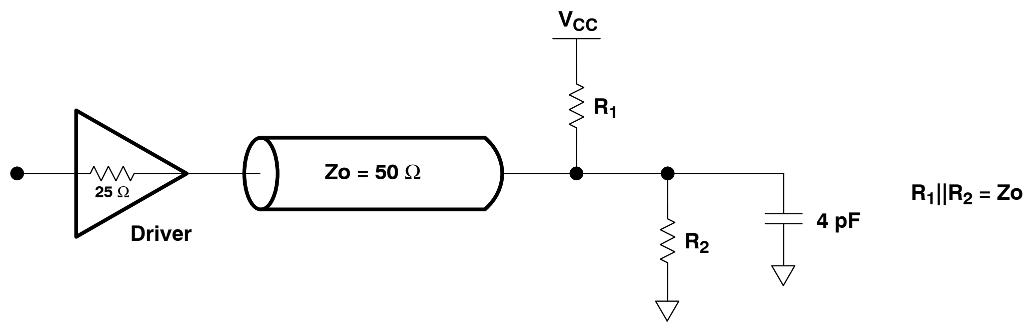


Figure 8. Thévenin Termination

The termination resistors are a pullup and pulldown pair that help balance the driver's high- and low-logic levels. This method enhances the fan-out capability of the driver, and it reduces power consumption caused by duty cycle distortion. A disadvantage is the constant dc-current leakage from V_{CC} to GND regardless of the driver's logic state.

3.4 AC Termination

Here, an RC high-pass filter is used to terminate the load end of the trace (see Figure 9). AC termination is recommended for backplanes, cables, distributed loads, and clocks drivers. It generates no power dissipation and permits loads to be added anywhere along the transmission line. To avoid overshoot and undershoot, the RC time constant should be greater than the transmission line's round-trip propagation time. The capacitor serves to block low-frequency noise and considerably reduces quiescent power dissipation while minimizing overshoot and undershoot.

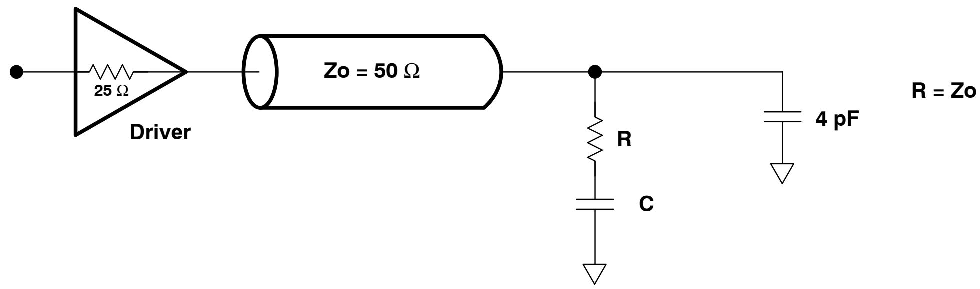


Figure 9. AC Termination

4 Layout Guidelines

The following suggestions are offered to aid PCB layout:

- Isolate the power pin of the clock driver from the power plane of the board by a ferrite bead. The ferrite prevents high-frequency noise from reaching the main power supply.
- Minimize EMI by avoiding the use of vias to route clock signals. Vias add unwanted inductance to the trace and in general reduce the effectiveness of bypass capacitors.
- To minimize reflections and ringing, keep traces short and impedance balanced
- If possible, place clock signals far away from data busses.
- Load all outputs equally.
- Avoid routing traces near the edge of the PCB board.
- Clock traces should not cross each other. They should also be of equal length to minimize clock skew.
- Route clock traces point-to-point and terminate them individually.
- Keep power and ground planes close together. This reduces power-supply noise.
- Place power-supply decoupling capacitors and filter components as close to VCC as possible. For decoupling, it is recommended to use low-inductance, low-ESR (equivalent series resistance) capacitors because they provide best performance.

5 Filtering and Noise Reduction Techniques

The following provides general guidelines for reducing radiated emissions and improving signal quality of PLL clock generators. Also discussed are power-supply and ground-noise reduction techniques through decoupling, and the use of both bypass capacitors and ferrite beads.

5.1 Bypass and Filter Capacitors

Filter capacitors are used to eliminate low-frequency power-supply noise. A popular filter capacitor is a surface mount 22-µF ceramic device connected as close to the power supply as physically possible.

Bypass capacitors, on the other hand, are used to provide a very-low-impedance path for current surges between V_{CC} and GND at high frequency. Also, they guard the power system against induced fluctuations. It is recommended to use mica or monolithic, ceramic-type capacitors because they are small, inexpensive and, most importantly, they have very low equivalent series inductance (ESL) and series equivalent resistance (ESR). The precise value for a bypass capacitor can be determined as follows (see also Johnson and Graham, 1993).

- Assuming all gates are switching simultaneously, find the maximum expected step change in current and the maximum power-supply noise. Dividing the power-supply noise by the current change gives the *maximum* common-path impedance: $Z_{max} = \Delta V/\Delta I$.
- Find the inductance, L, of the power-supply wiring, then calculate the 3-dB or knee frequency using the equation $f = Z_{max}/(2\pi L)$.
- Calculate the capacitance, C, of the bypass capacitor according to $C = 1/(2\pi f Z_{max})$.

This kind of calculation is exemplified by the following: Assume (i) there is a 40-gate board with each gate switching a 20-pF load in 2.5 ns, (ii) the power supply has a wiring inductance, L, of 100 nH, and (iii) a voltage noise margin, V_n, of 110 mV. Then

$$\Delta I = n\,C\,\frac{\Delta V}{\Delta t} = \frac{(40)\left(20 \times 10^{-12}\right)(3.3)}{2.5 \times 10^{-9}} = 1.056 \text{ A}$$

The maximum impedance is

$$Z_{max} = \frac{V_n}{\Delta I} = \frac{0.110}{1.056} = 0.104\ \Omega$$

Then, the frequency above which the power supply wiring requires a bypass capacitor to take over is

$$f_{PSW} = \frac{Z_{\max}}{(2\pi\,L)} = \frac{0.104}{2\pi \times 100 \times 10^{-9}} = 166 \text{ kHz}$$

Next, the value of the bypass capacitor is calculated:

$$C_{bypass} = \frac{1}{(2\pi\,f_{PSW}\,Z_{max})} = \frac{1}{2\pi \times 166 \times 10^{3} \times 0.104} = 9.22\ \mu\text{F}$$

This is an uncommon value, so a 10-µF capacitor is used instead. The calculation says that a 10-µF capacitor is effective at frequencies above 166 kHz. Assuming now that the 10-µF capacitor has an ESL of 1 nH, the *maximum* frequency at which this bypass capacitor is effective is

$$f_{bypass} = \frac{Z_{max}}{(2\pi\,ESL)} = \frac{0.104}{\left(2\pi \times 1 \times 10^{-9}\right)} = 16.55 \text{ MHz}$$

The 10-µF capacitor is effective over the hundredfold range from 166 kHz to 16.6 MHz.

It is good practice to use an array of small capacitors in parallel because they provide lower series inductance at high frequency than a single large capacitor. The most common values for bypass capacitors are: 22 µF, 4.7 µF, 0.1 µF, and 0.001 µF. The 22-µF and 4.7-µF capacitors work well at relatively low frequency (low frequency bypass). The 0.1-µF capacitor targets the midrange frequencies, while 0.001-µF and smaller capacitors handle high frequencies (high frequency bypass). Choosing three or more capacitors with different values effectively filters noise from a wider bandwidth.

As opposed to ideal capacitors, real capacitors contain additional parasitic, inductive and resistive elements. The most important parameters are the ESL and ESR, because they act respectively as an inductance and a resistance in series with the capacitance. They tend to defeat the effectiveness of a bypass capacitor.

The equation for the impedance of a capacitor as a function of frequency, including ESR, is:

$$X(f) = \sqrt{ESR^2 + \left(2\pi fL - \frac{1}{2\pi fC}\right)^2}$$

There are several ESR meters commercially available that can measure very low resistance (below 1 Ω), and some ESR meters are 1-Ω full-scale with 10-mΩ resolution. There are other methods for measuring ESR without using an ESR meter—further information on ESR measurements can be found at: http://fribble.cie.rpi.edu/~repairfaq/sam/captest.htm

5.2 Ferrite Beads

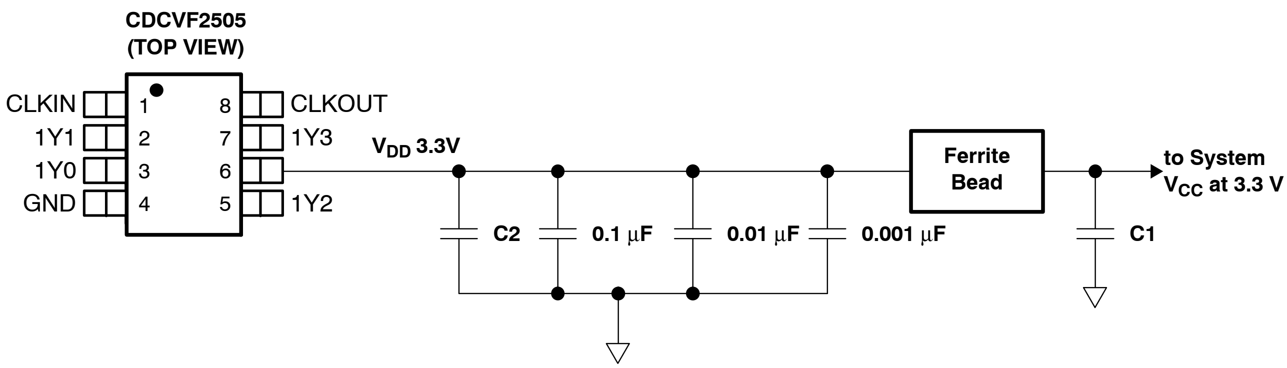
By nature, PLL-based clock drivers and generators are noise-sensitive. Inserting a ferrite bead to isolate the high-frequency noise created by the clock generator and to prevent it from reaching the main power supply suppresses noise and reduces its spread around the PCB.

Ferrite beads neither enhance nor degrade the performance of a clock generator; they merely provide noise isolation (power supply decoupling). It is preferable to use low-dc-impedance ferrite, between 0 Ω and 5 Ω. However, at clock frequencies the impedance of the bead should be at least 50 Ω under load conditions. This relatively large impedance prevents noise generated by clock harmonics from spreading across the PCB. The impedance of a ferrite bead is a function of frequency, size, material, and the number of turns. Because ferrite beads are composed of ferromagnetic material that is contained within the bead, they are not susceptible to externally-radiated magnetic fields, nor can such fields detune them. Only when temperature rises above the Curie point will the ferrite loose its magnetic properties and become useless as a noise-attenuating element.

The Curie temperature is material dependant and can range between 120°C and 500°C. Although other vendors have similar products, Fair-Rite Corporation's beads #43/44, #61, #73 are popular and meet these requirements. The #43/44 material is best-suited for noise attenuation over the range 20–300 MHz; the #73 material is recommended for suppression over the range 1–25 MHz; for frequencies above 200 MHz, #61 is the best choice.

5.3 Filter Circuit

Putting these components together provides good filtering for many clock generators and especially for PLL-based clock drivers. Although the CDCVF2505 has only one V_{CC}, it has an integrated internal filter circuit separating the analog and digital power supplies, it works even better with an additional external filter circuit. Figure 10 contains an example of such a circuit.



NOTES: 1. C2 can be 47, 39, 10, or 4.7 μF
2. C1 is system dependent and can be found as in the example

Figure 10. Filter Circuit for the CDCVF2505

The exact value of a bypass capacitor is not as critical as having three or more different capacitor ranges, one each for low frequency, midrange, and high frequency. For example, if the maximum wiring impedance, Z_{max}, is 0.1 Ω, the value, C, of the bypass capacitor can be calculated from the equation $C = 1 / (2\pi f Z_{max})$. Values for some capacitors that can be used to filter certain noise frequencies are listed in Table 2.

Table 2. Capacitor Values for Filtering Certain Frequencies

f_{3dB} (MHz)	C (μF)
0.033	47
0.072	22
0.159	10
0.339	4.7
3.2	0.5
7.2	0.22
16	0.1
32	0.05
80	0.02
100	0.016
160	0.01
200	0.008
318	0.005
400	0.004
1600	0.001

5.4 Typical Output Driver Characteristics

Figures 11 and 12 show the output buffer characteristic impedance of the CDCVF2505 clock driver when the driver is in high and low states, respectively. These curves provide typical output behavior when driving both single and multiple loads. The strength of the driver is measured by the current sourcing or sinking capabilities.

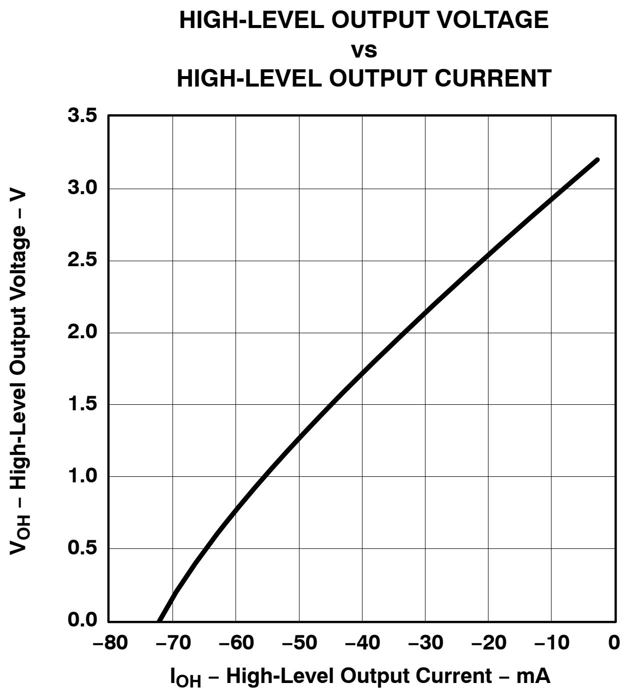


Figure 11. High-Level Output Voltage vs Current

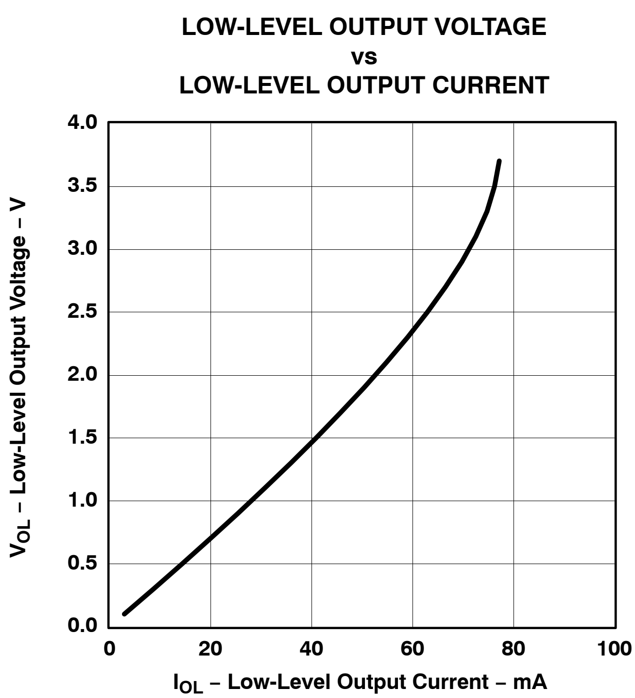


Figure 12. Low-Level Output Voltage vs Current

6 Bibliography

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