

Defining Skew, Propagation-Delay, Phase Offset (Phase Error)

Kal Mustafa
High Performance Analog/CDC

ABSTRACT

This application note discusses various types of skew, propagation delays, and phase error/phase offset in general. Special attention is given to important parameters that are used in TI clock distribution circuits (CDC) devices. This application note will not address measurement methods of these parameters; however, another report will address these measurements.

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1 Skew

Skew is the time delta between the actual and expected arrival time of a clock signal. Skew can be either extrinsic or intrinsic. The latter is internal to the driver (generator circuitry) and defined as the difference in propagation delays between the device outputs. On the other hand, extrinsic skew is the time difference due to unbalanced trace lengths and/or output loading.

1.1 Output Skew

Output skew ($t_{sk(o)}$) is also referred to as pin-to-pin skew, output skew is the difference between propagation delays of any two outputs of the same device at identical transitions (i.e., compares $t_{pd(LH)}$ versus $t_{pd(LH)}$ or $t_{pd(HL)}$ versus $t_{pd(HL)}$ for any two outputs). For example, if the propagation delay of the fastest output ($t_{pd(LHn)}$) is 2 ns and that of the slowest output ($t_{pd(LH1)}$) is 2.165 ns, then the output skew is: $t_{sk(o)} = t_{pd(LHn)} - t_{pd(LH1)} = -165$ ps

JEDEC defines output skew as: the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

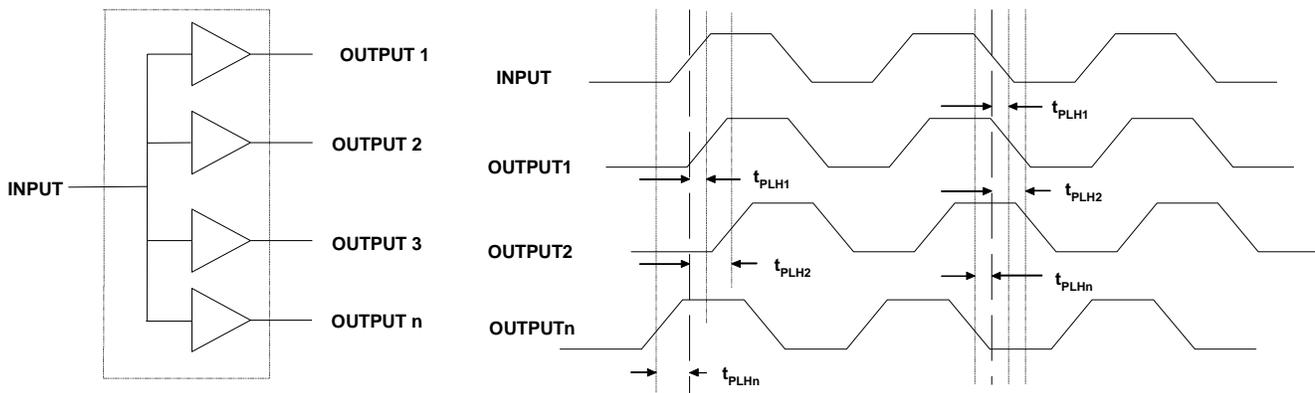


Figure 1. Output Skew (Pin-to-Pin Skew)

1.2 Part-to-Part Skew

Part-to-part skew ($t_{sk(pp)}$) is also known as package skew and device-to-device skew. Part-to-part skew is similar to output skew, except that it applies to two or more identical devices. Part-to-part skew is defined as the magnitude of the difference in propagation delays between any specified outputs of two separate devices operating at identical conditions. The devices must have the same input signal, supply voltage, ambient temperature, package, load, environment, etc.

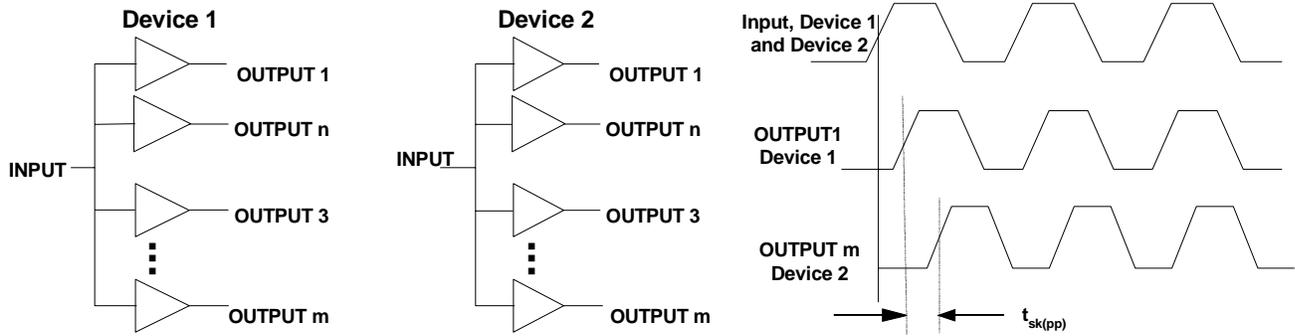


Figure 2. Part-to-Part Skew (Device-to-Device and Package Skew)

1.3 Pulse Skew

Pulse skew ($t_{sk(p)}$) is the magnitude of the time difference between the high-to-low (t_{PHL}) and the low-to-high (t_{PLH}) propagation delays when a single switching input causes one or more outputs to switch, $t_{sk(p)} = |t_{PHL} - t_{PLH}|$.

Pulse skew is sometimes referred to as pulse width distortion or duty cycle skew.

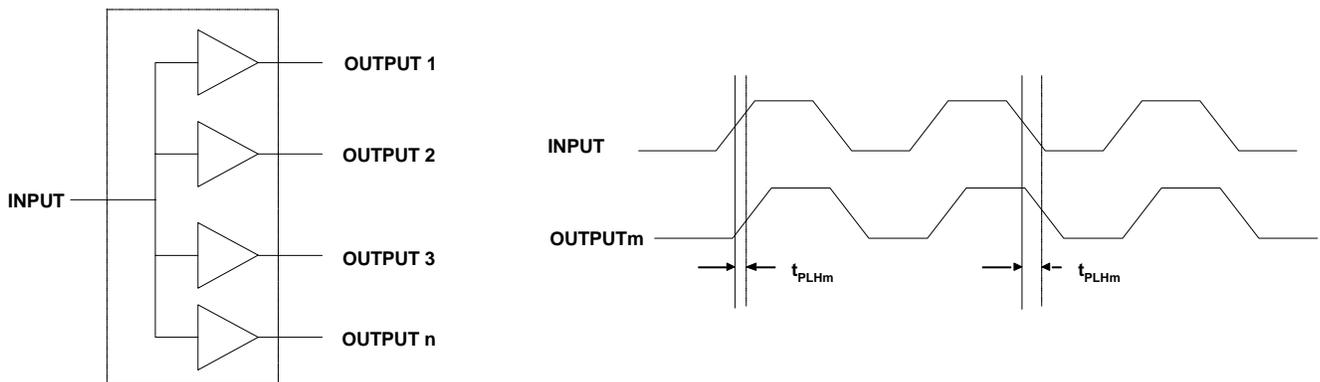


Figure 3. Pulse Skew

1.4 Process Skew

Process skew ($t_{sk(pr)}$) is the difference in propagation delay times between corresponding outputs on any two like devices when both devices operate under identical conditions. Process skew quantifies skew due to process variation in the manufacturing process (skew caused by lot-to-lot variation). It excludes variations in supply voltage, operating temperature, output loading, input edge rate, input frequency, etc. Conceptually, process skew is output skew over several devices.

Process skew is generally specified and production tested under fixed conditions (e.g., $V_{CC} = 3.3 \text{ V}$, $T_A = 25^\circ\text{C}$, $C_L = 25 \text{ pF}$, all inputs switching simultaneously).

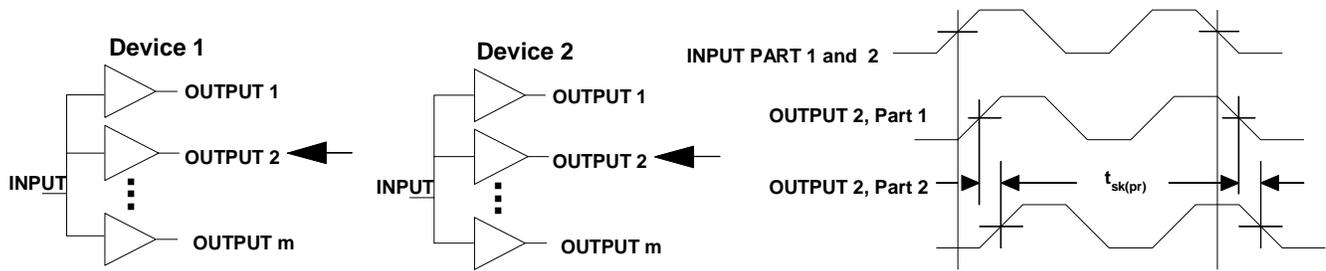


Figure 4. Process Skew

1.5 Bank Skew

Bank skew ($t_{sk(b)}$) is the output skew between outputs (at same bank), of a single device with a single driving input terminal. The main difference between bank skew and output skew is that the latter is the worst-case delta between outputs in any output bank.

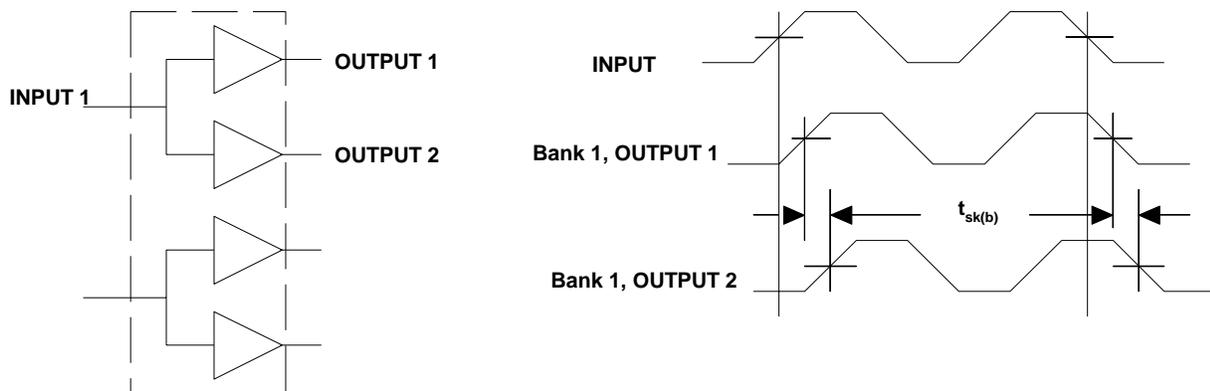


Figure 5. Bank Skew

1.6 Inverting Skew

Inverting skew ($t_{sk(inv)}$) is the skew between specified outputs of a single logic device with all driving inputs connected together and the outputs switching in opposite directions while driving identical specified loads.

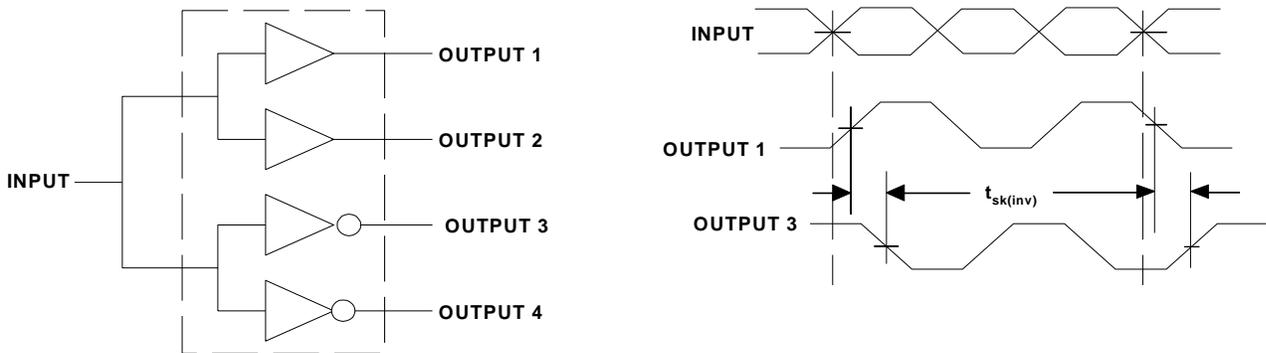


Figure 6. Inverting Skew

1.7 Multiple-Frequency Skew

Multiple-frequency skew ($t_{sk(\omega)}$) is the skew between the controlled-edge position of two different output frequencies of a PLL or counting device that has more than one output frequency, when both signals are rising or both signals are falling.

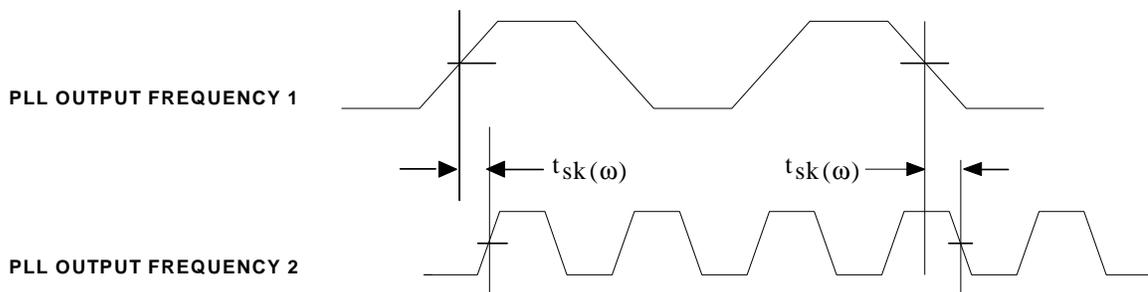


Figure 7. Multiple-Frequency Skew

1.8 PLL Tracking Skew

PLL tracking skew is the phase difference between the input clock and output clock due to the PLL's inability to instantaneously update the output clock when the period of the input clock changes. Tracking skew normally applies to a PLL with SSC induced input clock [4]. Therefore, tracking skew is the phase offset of a PLL resulting from a time-varying reference input. If the total measured phase offset due to tracking skew is lumped with phase jitter, including input jitter, then it is referred to as the accumulated tracking skew. Note that tracking skew can either lead or lag the reference clock input.

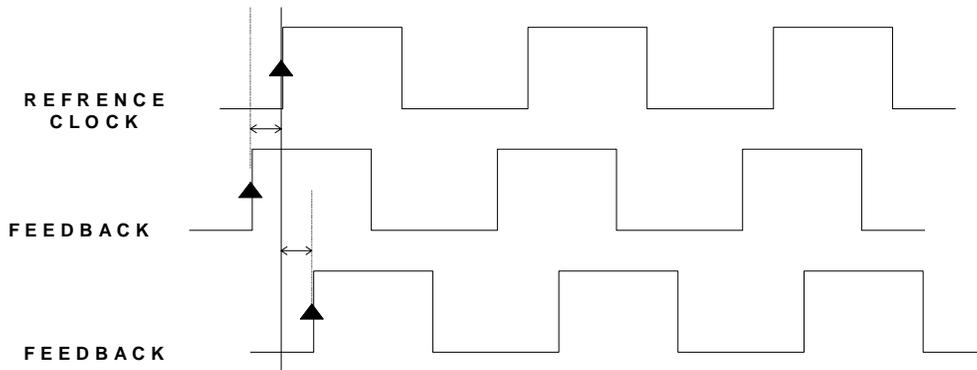


Figure 8. PLL Tracking Skew

1.9 Input Skew

Input skew ($t_{sk(i)}$) is the difference between any two propagation delay times that originates at different inputs and terminates at a single output. Input skew describes the ability of a device to manipulate (stretch, shrink, or chop) a clock signal. This is typically accomplished with a multi-input gate wherein one of the inputs acts as a controlling signal to pass the clock through. Input skew describes the ability of the gate to shape the pulse to the same duration regardless of the input used as the controlling input.

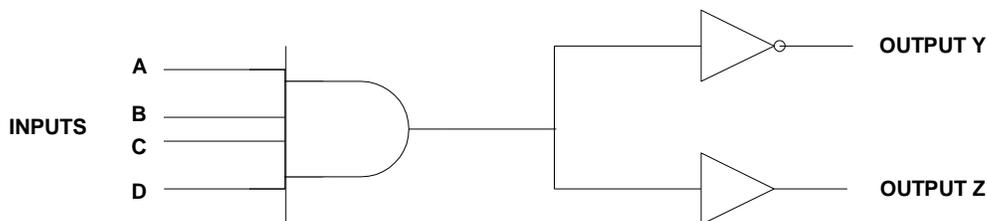


Figure 9. Example of a Gate With Input Skew

1.10 Limit Skew

Limit skew ($t_{sk(l)}$) is the difference between the greater of the maximum specified values of t_{PLH} and t_{PHL} , and the lesser of the minimum specified values of t_{PLH} and t_{PHL} . Limit skew is not observed directly on a device; rather it is calculated from the data sheet limits of t_{PLH} and t_{PHL} . Limit skew quantifies how much variation in propagation delay times are induced by operation over the entire ranges of V_{CC} , T_A , output load, process variation and any other specified operating conditions.

In general, not all-skew parameters are of interest, but their discussion is included for illustration. The goal is to minimize skew to an acceptable value. The rule of thumb is that clock skew should be < one-tenth of the system clock period. For example, a system operating at 100 MHz has a period of 10 ns, and the clock skew should be <1 ns. At 500 MHz, the period is reduced to 2 ns and clock skew should be <20 ps. Therefore, the operating frequency dictates the skew budget for a particular system.

1.11 Board Skew

Board skew ($t_{sk(pcb)}$) is introduced into the timing system by unequal trace lengths and unequal loading. It is independent of skew generated by the clock driver.

2 Propagation Delay

Propagation delay (t_{pd}) is the time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high-to-low) to the other (low-to-high) defined level ($t_{pd} = t_{PHL}$ or t_{PLH})

2.1 Propagation Delay Time, High-to-Low Level Output

Propagation delay time, high-to-low level output (t_{PHL}) is the time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

2.2 Propagation Delay Time, Low-to-High Level Output

Propagation delay time, low-to-high level output (t_{PLH}) is the time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.

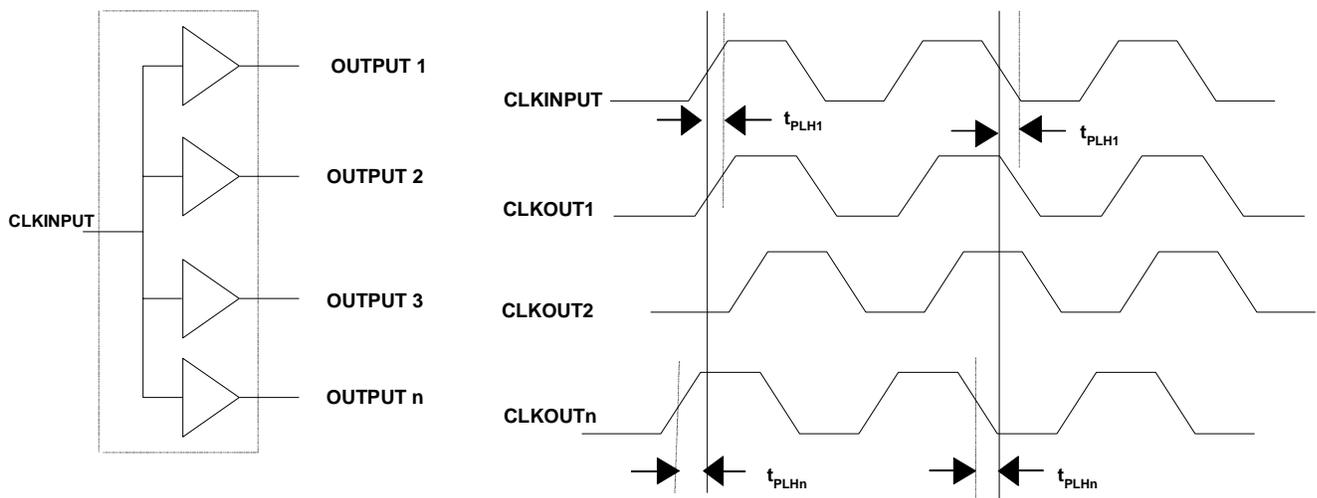


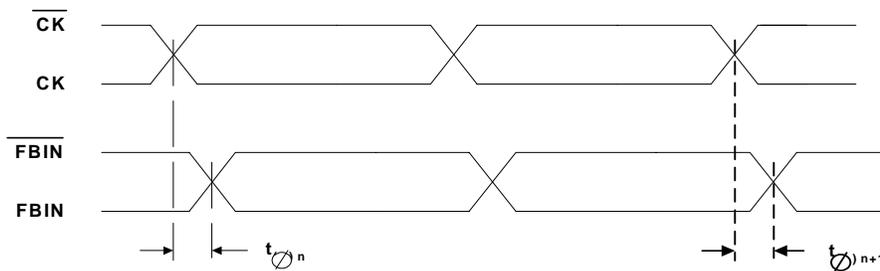
Figure 10. Propagation Delay Times, Low-to-High (t_{PLH}) and High-to-Low (t_{PHL})

3 Phase Offset (Phase Error)

Phase offset/phase error is the time difference between the reference input clock and the feedback input to the phase detector of a PLL. The two types of phase error, static and dynamic phase errors, are defined below.

3.1 Static Phase Offset

Static phase offset (t_{ϕ}) is the time difference between the *averaged* input reference clock and the *averaged* feedback input signal when the PLL is in locked mode. The word *average* implies that a comparison is made between the input of the PLL and its feedback over several thousand periods, and the resulting time differences are averaged. This method excludes jitter components, hence the name static phase offset. [1]



$$t_{\phi} = \frac{\sum_{n=1}^N t_{\phi n}}{N} \quad (\text{N is a large number of samples})$$

Figure 11. Static Phase Offset (Static Phase-Error)

3.2 Dynamic Phase Offset

Dynamic phase offset ($t_{d(\phi)}$) is the phase difference between input clock and output clock due to the PLL's inability to instantaneously update the output clock when the period of the input clock changes (due to input-clock SSC) [4]. This is also referred to as tracking skew. The dynamic phase offset includes jitter (specification not yet finalized in JEDEC).

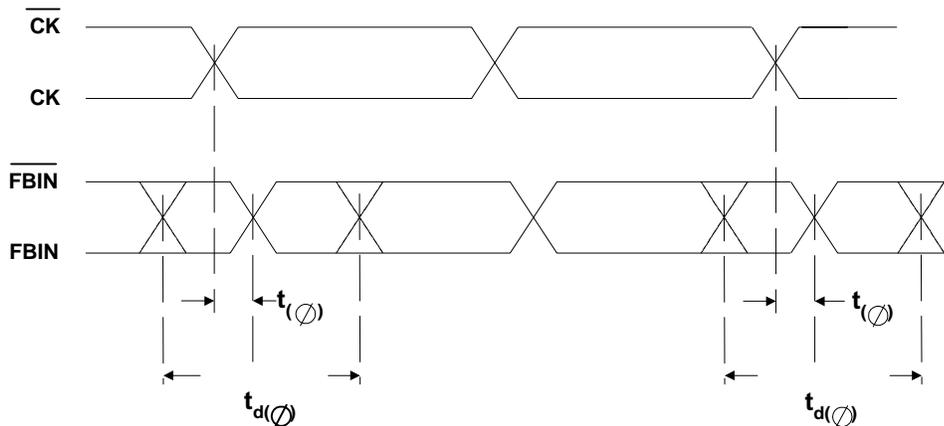


Figure 12. Dynamic Phase Offset (Dynamic Phase-Error and Tracking Skew)

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Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265