DC-Coupling Between Differential LVPECL, LVDS, HSTL, and CM

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ABSTRACT

This report describes various methods of interfacing different logic levels. The focus is dc-coupling between the following differential signaling: LVPECL (low-voltage positive-referenced emitter coupled logic), LVDS (low-voltage differential signals), HSTL (high-speed transceiver logic), and CML (current-mode logic). The report discusses sixteen various interface cases between the aforementioned differential signaling levels.

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1 AC-Coupling

DC-coupling is used in a system when there is a need for a wide bandwidth, or when dc-unbalanced code is used. Both interfaces must have the same ground potential on the same board or system. DC-coupling directly connects the components together without any coupling capacitors. Among the advantages of dc-coupling are: simple board design, no dc-wander issues, and it is useful in all coded-data streams including SONET and NRZ data applications. One disadvantage of dc-coupling is that it requires careful power supply design. Figure 1, Table 1, and Table 2 provide the I/O levels for these differential signals.

![Figure 1. Input and Output Parameters](image)

<table>
<thead>
<tr>
<th>Output</th>
<th>LVPECL</th>
<th>LVDS</th>
<th>HSTL</th>
<th>CML</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OH}$ (Min)</td>
<td>2.275 V</td>
<td>1.249 V</td>
<td>VDDQ$^1$ - 0.4 V</td>
<td>$V_{CC}^2$</td>
</tr>
<tr>
<td>$V_{OL}$ (Max)</td>
<td>1.68 V</td>
<td>1.252 V</td>
<td>0.4 V</td>
<td>$V_{CC}$ - 0.4 V</td>
</tr>
</tbody>
</table>

Table 2. Typical LVPECL, LVDS, CML, and HSTL Input Levels

<table>
<thead>
<tr>
<th>Input</th>
<th>LVPECL</th>
<th>LVDS</th>
<th>HSTL</th>
<th>CML</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IH}$ (Min)</td>
<td>2.135 V</td>
<td>1.249 V</td>
<td>VRef + 0.2 V</td>
<td>$V_{CC}$</td>
</tr>
<tr>
<td>VRef or VCM</td>
<td>2</td>
<td>1.2</td>
<td>0.75</td>
<td>$V_{CC}$ - 0.2 V</td>
</tr>
<tr>
<td>$V_{IL}$ (Max)</td>
<td>1.825 V</td>
<td>1.252 V</td>
<td>VRef - 0.2 V</td>
<td>$V_{CC}$ - 0.4 V</td>
</tr>
<tr>
<td>$V_{ID}$ (Min)</td>
<td>310 mV</td>
<td>200 mV</td>
<td>400 mV</td>
<td>400 mV</td>
</tr>
</tbody>
</table>

$^1$ VDDQ = 1.5 V ±10%

$^2$ $V_{CC}$ = 3.3 V ±10%
### Table 3. Interface Table

<table>
<thead>
<tr>
<th>FROM</th>
<th>LVPECL</th>
<th>LVDS</th>
<th>CML</th>
<th>HSTL</th>
</tr>
</thead>
<tbody>
<tr>
<td>LVPECL</td>
<td>See Figure 3</td>
<td>See Figure 4 or Figure 5</td>
<td>See Figure 6 or Figure 7</td>
<td>See Figure 8</td>
</tr>
<tr>
<td>LVDS</td>
<td>See Figure 9 or Figure 10</td>
<td>See Figure 11 or Figure 12</td>
<td>See Figure 13</td>
<td>See Figure 14</td>
</tr>
<tr>
<td>CML</td>
<td>See Figure 15</td>
<td>See Figure 16 or Figure 17</td>
<td>See Figure 18</td>
<td>See Figure 22</td>
</tr>
<tr>
<td>HSTL</td>
<td>See Figure 19</td>
<td>See Figure 20</td>
<td>See Figure 21</td>
<td>See Figure 22</td>
</tr>
</tbody>
</table>

### 1.1 LVPECL

Figure 2. **LVPECL to LVPECL**

PECL and LVPECL are normally terminated though 50 Ω to \((V_{CC} - 2 \text{ V})\). Most systems normally do not have dual power supplies of both 3.3 V and 1.3 V; therefore Figures 2 and Figure 3 show alternative methods to terminate LVPECL output signals. The pullup and pulldown combination terminates the 50-Ω transmission line and establish the LVPECL common-mode voltage of 2 V at the receiver.
The Y-termination in Figure 3 is another alternative to LVPECL termination where a VTT supply is not readily available. This scheme saves one resistor over the scheme in Figure 2.

The 33-Ω resistor is usually required when the LVPECL output is too high for the LVDS receiver input stage. For the LVDS receivers listed above, it is not required and Figure 5 is recommended.
Most LVDS receivers are capable of accepting LVPECL signals and it is not necessary to attenuate the LVPECL signal prior to the LVDS receiver. This is due to the wide common-mode range of the LVDS receivers listed above.

The most widely used method of translating from LVPECL to CML is through ac-coupling. AC-coupling is recommended for dc-balanced signals. AC-coupling generates base-line wander in high-speed serial data transmission such as SONET and NRZ encoded data (non dc-balanced). Therefore, dc-coupling is recommended for such data streams. For detailed derivation, see the SCAA056.
Figure 7. LVPECL to CML Converter

The SN65CML100, in Figure 7, can be used as an LVPECL to CML converter. The 50-Ω pullup resistors are required to bias the SN65CML100 outputs as well as terminate the transmission line. In most cases, the two 50-Ω resistors are included in the CML receiver input stage and therefore are not required.

Figure 8. LVPECL to HSTL

Note:
For $V_{CC} = 3.3$ V, use $R_1 = 127 \, \Omega$, $R_2 = 35 \, \Omega$, $R_3 = 48 \, \Omega$
For $V_{CC} = 2.5$ V, use $R_1 = 100 \, \Omega$, $R_2 = 40 \, \Omega$, $R_3 = 60 \, \Omega$
1.2 LVDS

The resistors R1 in parallel with (R2+R3) should match the characteristic impedance \( Z_O = 50 \, \Omega \) of the transmission line. At point Y in Figure 8, the ratio of R3 to the sum of (R1+R2+R3) should be chosen to set the HSTL common-mode voltage \( (VCM = 0.75 \, V) \). At point X, the LVPECL common-mode voltage is 2 V, which is the voltage across R1 compared to the sum of all three resistors \((R1+ R2+R3)\).

![Diagram showing LVDS to LVPECL conversion](image.png)

**Figure 9. LVDS to LVPECL**

The Thevenin equivalent of the 83 \( \Omega \) and 130 \( \Omega \), in Figure 9, matches the 50-\( \Omega \) transmission line impedance as well as sets the common-mode voltage \( (VCM = 2 \, V) \) for the LVPECL receiver.
Figure 10. LVDS to LVPECL

The SN65LVDS101, in Figure 10, can be used as an LVDS to LVPECL converter. The 50-Ω pullup resistors are required to bias and terminate the LVPECL outputs to VTT (V_{CC} – 2 V). If the termination voltage, VTT is not available then, the Thevenin equivalent of the 83 Ω and 130 Ω, as in Figure 9 is recommended.

Figure 11. LVDS to LVDS Without On-Chip Termination
Figure 11 is the most commonly used termination for LVDS signals. The $100\,\Omega$ external resistor terminates the differential impedance of the transmission line assuming the LVDS receiver does not include an on-chip termination. The designer could also replace the $100\,\Omega$ termination with two $50\,\Omega$ resistors and tie the mid-point with a capacitor (10 nF) to GND in order to terminate any unbalanced noise within the differential transmission line as well as correct for line-length mismatches.

![Figure 11: LVDS to LVDS With On-Chip Termination](image)

**Figure 12. LVDS to LVDS With On-Chip Termination**

In Figure 12, the LVDS receiver includes a $100\,\Omega$ on-chip resistor; therefore no external termination is needed.

![Figure 13: LVDS to CML Converter](image)

**Figure 13. LVDS to CML Converter**
Most CML receivers have 50 Ω included on their input stage and external termination is not required. The 50-Ω pullup resistors are required to bias the SN65CML100 and terminate the transmission line.

\[ Z_0 = 50 \Omega \]

**Figure 14. LVDS to HSTL**

At the output of the LVDS driver, the ratio of \((R2+R3)\) to the sum of all three resistors \((R1+R2+R3)\) is the same ratio of \(V_{CM} = 1.2 \text{ V}\) to \(V_{CC}\). The ratio of \(R3\) to the sum \((R1+R2+R3)\) must be equal to the ratio 0.75: \(V_{CC}\). Furthermore; \(R1// (R2+R3)\) should match the transmission line impedance, \(Z_0 = 50 \Omega\). Solving these equations result in the values as in Figure 14 for \(V_{CC}\) of 3.3 and 2.5 respectively.
1.3 CML

Figure 15. CML to LVPECL Translator

Commonly, ac-coupling is recommended when driving LVPECL with CML. The SN65LVDS101 has a wide common-mode range and can accept CML while providing an LVPECL output.

Figure 16. CML to LVDS
Generally, ac-coupling is recommended when driving LVDS receiver with CML. If the LVDS receiver has a wide common-mode range that can accept a CML input (common-mode range must go to $V_{CC}$ rail), then a dc-coupled connection is a direct connection. The 50-Ω pullup resistors are required to bias the SN65CML100 and terminate the transmission line.

Figure 17. CML to CML

If both the CML driver and receiver have the same $V_{CC}$ supply voltage and on-chip pullup resistors, then a direct connection can be made without external components. If the output stage does not provide an internal 50-Ω pullup resistor (TLK1501), then 50-Ω pullup resistors are required at the transmitter output or at the receiver input. The 50-Ω pullup resistors (see Figure 17) could also be moved to the receive end instead. In addition to the 50-Ω pullup at the source, a 100-Ω line end termination could be implemented at the receiver to terminate the line-impedance at both ends of the link.
In Figure 18, the resistor network R1, R2, and R3 provides proper termination. The network also provides level shifting from CML to HSTL. Using the I/O tables, the following equations are used to solve for R1, R2, and R3. First, \((R2+R3)/(R1+R2+R3) = 3.1/3.3\). Second, \(R3/(R1+R2+R3) = 0.75/3.3\). Finally, \(R1||(R2+R3) = Z_0 = 50\ \Omega\).

1.4 HSTL

Figure 19. HSTL to LVPECL Converter

The CDCLVP110 in Figure 14 has dual inputs for either HSTL (CLK1 pair is optimized for HSTL levels) or LVPECL inputs (CLK0 pair accepts LVPECL). In both cases, the CDCLVP110...
provides LVPECL outputs.

Figure 20. HSTL to LVDS

HSTL signals are usually terminated to \( V_{TT} = V_{ref} = 0.75 \text{ V} \). Since most LVDS compatible receivers accept a 200-mV signal swing anywhere between 0 V and 2.4 V; then the HSTL signal is well within the LVDS receiver input range. The typical HSTL signal swing is 400 mV (minimum), 1.1 V (maximum) this amplitude is compatible with the LVDS receiver. The SN65LVDS100 requires a 3.3-V supply, while the CDCLVD110 is 2.5-V LVDS driver/receiver.

Figure 21. HSTL to CML Translator

The wide common-mode inputs range (0 V to 2.4 V) of the SN65CML100 accepts HSTL levels. The 50-Ω resistors are required to bias the SN65CML100 and terminate the transmission line.
HSTL signals are usually terminated 50-Ω to VTT (typically VTT = 0.75 V). When VTT is not available, an alternative is a 100-Ω differential termination.

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13. TLK1501 data sheet, Texas Instruments, (SLLS458)
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