Dual Purposes: Data Buffer, the Other Face of the CDCP1803

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ABSTRACT

The CDCP1803 is a clock driver by design, but can be used as a data buffer. The CDCP1803 performance as a data buffer is demonstrated both in terms of the bit error rate (BER) and eye pattern diagrams. The CDCP1803 is tested over several signaling rates and different PRBS patterns.

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1 Introduction

When choosing a data buffer the amount of jitter introduced by the buffer is crucial. One quantitative measurement that provides insight to the performance of the buffer is the bit error rate (BER). The BER is the ratio of bits that have errors to the total number of bits received. A buffer with more jitter gives the opportunity for more errors, thus a higher BER. The desired BER is dependent on the system requirements. Another measurement that is often used to judge the worthiness of the buffer is the eye pattern diagram. An eye pattern diagram is obtained by overlapping multiple cycles of the signal on the screen of an oscilloscope. The eye opening/closure is indicative of the signal integrity. The deviation of the signal crossing shows the jitter in the signal and its complement, the eye opening, which is usually given as a percentage of the unit interval (UI). A more open eye has a higher margin for the sampling window and therefore a lower chance of bit errors. While the jitter allowed is system dependent, 20% is the recommended maximum.

1.1 Test Setup

The CDCP1803 is a 3.3 V, 1:3 LVPECL (low voltage positive emitter coupled logic) clock buffer with a programmable divider. The CDCP1803 is characterized for industrial temperature (–40°C to 85°C) and has a maximum operating frequency of 800 MHz. The BER measurements were taken with the Anritsu MP1632C a 3.2G bit error rate analyzer with a total of 2E13 bits sent. A Tektronix TDS694C 4-channel digital real-time oscilloscope was used to capture the eye diagrams included in this report. Both test procedures included two meters of cable between the CDCP1803 output and the measurement tool. The block diagrams of the test setups are shown in Figure 1 and Figure 2.

Figure 1. Test Setup for BER Measurements
2 Measurement Results

2.1 BER and Eye Opening

<table>
<thead>
<tr>
<th>DATA RATE</th>
<th>PRBS PATTERN</th>
<th>BER</th>
<th>EYE OPENING</th>
<th>SHOWN IN</th>
</tr>
</thead>
<tbody>
<tr>
<td>700 Mbps</td>
<td>$2^7-1$</td>
<td>$&lt; 5 \times 10^{-14}$</td>
<td>93.49%</td>
<td>Figure 3</td>
</tr>
<tr>
<td>700 Mbps</td>
<td>$2^{23}-1$</td>
<td>$&lt; 5 \times 10^{-14}$</td>
<td>91.25%</td>
<td>Figure 4</td>
</tr>
<tr>
<td>900 Mbps</td>
<td>$2^7-1$</td>
<td>$&lt; 5 \times 10^{-14}$</td>
<td>88.29%</td>
<td>Figure 5</td>
</tr>
<tr>
<td>900 Mbps</td>
<td>$2^{23}-1$</td>
<td>$&lt; 5 \times 10^{-14}$</td>
<td>88.29%</td>
<td>Figure 6</td>
</tr>
<tr>
<td>1.1 Gbps</td>
<td>$2^7-1$</td>
<td>$&lt; 5 \times 10^{-14}$</td>
<td>84.03%</td>
<td>Figure 7</td>
</tr>
<tr>
<td>1.1 Gbps</td>
<td>$2^{23}-1$</td>
<td>$&lt; 5 \times 10^{-14}$</td>
<td>84.49%</td>
<td>Figure 8</td>
</tr>
<tr>
<td>1.3 Gbps</td>
<td>$2^7-1$</td>
<td>$&lt; 5 \times 10^{-14}$</td>
<td>84.78%</td>
<td>Figure 9</td>
</tr>
<tr>
<td>1.3 Gbps</td>
<td>$2^{23}-1$</td>
<td>$&lt; 5 \times 10^{-14}$</td>
<td>85.82%</td>
<td>Figure 10</td>
</tr>
<tr>
<td>1.5 Gbps</td>
<td>$2^7-1$</td>
<td>$&lt; 5 \times 10^{-14}$</td>
<td>84.56%</td>
<td>Figure 11</td>
</tr>
<tr>
<td>1.5 Gbps</td>
<td>$2^{23}-1$</td>
<td>$&lt; 5 \times 10^{-14}$</td>
<td>82.76%</td>
<td>Figure 12</td>
</tr>
</tbody>
</table>

At each data rate tested, the DUT buffered 2E13 total bits for both PRBS patterns of $2^7-1$ and $2^{23}-1$. For the eye pattern diagram test setup, the data and /data output from the DUT were sent to Channels 2 and 3, respectively, of the oscilloscope. The clock from the bit error rate analyzer was used as the trigger for the oscilloscope.
2.2 **Eye Diagrams**

The cursors are set to measure the openness of the eye diagram which is shown in the top right corner as delta (1.336 ns in Figure 3). Calculations of the % openness follow:

\[
\text{Delta/Unit Interval} = \frac{1.336 \text{ ns}}{1/700 \text{ Mbps}}
\]
\[
= \frac{1.336 \text{ ns}}{1.429 \text{ ns}}
\]
\[
= 0.9349
\]
\[
= 93.49\% \text{ eye open}
\]
Measurement Results

Figure 7. Eye Pattern Diagram at 1.1 Gbps, PRBS Pattern of $2^7-1$

Figure 10. Eye Pattern Diagram at 1.3 Gbps, PRBS Pattern of $2^{23}-1$

Figure 8. Eye Pattern Diagram at 1.1 Gbps, PRBS Pattern of $2^{23}-1$

Figure 11. Eye Pattern Diagram at 1.5 Gbps, PRBS Pattern of $2^{7}-1$

Figure 9. Eye Pattern Diagram at 1.3 Gbps, PRBS Pattern of $2^{23}-1$

Figure 12. Eye Pattern Diagram at 1.5 Gbps, PRBS Pattern of $2^{23}-1$
3 Summary

The data buffer is just one piece of the data communication chain and one contributor to the total interconnect jitter budget. While it is difficult to quantify how a part contributes to the jitter budget of a particular system, a sufficient measure of data performance is the BER or eye opening. The CDCP1803\(^{(1)}\) provides an 80% or greater eye opening for signaling rates ranging from 700 Mbps to 1.5 Gbps and for PRBS patterns of \(2^7-1\) and \(2^{23}-1\). While the CDC1803 is typically used with clocks, the CDC1803 can also be successfully applied to data applications.

\(^{(1)}\) It should also be noted that the CDCM1802 LVPECL output has similar performance characteristics.

3.1 References

1. CDCP1803 data sheet, Texas Instruments, (SCAS727)
2. CDCM1802 data sheet, Texas Instruments, (SCAS759)
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