Phase-Noise Performance of the CDC7005 at UMTS and CDMA Frequencies

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ABSTRACT

This application brief presents phase-noise data taken on Texas Instruments CDC7005 jitter cleaner and synchronizer PLL. The phase noise performance of CDC7005 depends on the phase noise of the reference clock, the voltage-controlled crystal oscillator (VCXO) clock, and the CDC7005 itself. This applications brief shows the phase noise performance of the CDC7005 clock synthesizer at the most popular Universal Mobile Telecommunications System (UMTS) and Code Division Multiple Access (CDMA) frequencies. It helps the user in choosing the right clocking solution for their particular applications. The test results reveal that the CDC7005 can provide clock outputs better than −145-dBc/Hz phase noises at 1-MHz offset from the carrier frequency with proper VCXO and loop bandwidth selection. Low phase noise is required for most base station applications such as UMTS and CDMA and its derivatives as well as many other jitter stringent applications.

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1 Introduction

Phase noise (PN) is the short-term instability caused by variation of frequency (phase) of a signal referenced to the carrier level and a function of the carrier offset (i.e., relative noise level within a 1-Hz bandwidth). Integration of PN over a given frequency band yields phase jitter RMS.

The CDC7005 is a low phase noise/low jitter clock synthesizer and jitter cleaner with five programmable LVPECL outputs. It requires either an external or internal low pass loop filter in addition to an external VCXO to complete the phase locked loop. By selecting VCXO and loop bandwidth, the device achieves the best performance at its outputs. This brief includes phase noise plots of the most common frequencies used in base station applications. In addition, the phase noise of the clock source feeding the CDC7005 is included for completeness.

2 Test and Measurements Setup

The block diagrams of the test setup are shown in Figure 1. An input reference clock from the HP8664A signal generator is fed into the Agilent E5250 and the phase noise of the source is measured (indicated by the dotted line). The same signal is then fed into one leg of the VCXO_IN of the CDC7005 and the phase noise is measured through the Agilent E5250 analyzer (open-loop).

All measurements were taken at nominal 3.3-V power supply, room temperature, and open loop PLL. The HP8644 as a signal generator, the CDC7005 evaluation module (EVM) in 1x mode, and the Agilent E5250 phase noise test system were used. The test setup below was used for most the phase noise testing. The phase noise can be measured up to 40 MHz from the carrier frequency, although some measurements were taken up to 10 MHz or 1 MHz from the carrier depending upon the desired clock frequency.
3 Summary and Conclusion

The CDC7005 PLL tracks the input reference signal up to the loop bandwidth, while it follows the VCO (here VCXO) phase noise floor at frequencies above the loop bandwidth. The VCXO phase noise performance is critical in achieving good phase noise performance and meeting stringent phase noise requirements in base station applications.
1. 10 Hz − 75.5874 dBc/Hz
2. 1 kHz − 106.659 dBc/Hz
3. 1 MHz − 144.084 dBc/Hz
4. 5 MHz − 144.51 dBc/Hz

Figure 3. Phase Noise of the CDC7005 at 30.72 MHz Driven by HP8664A

1. 10 Hz − 75.0862 dBc/Hz
2. 1 kHz − 105.163 dBc/Hz
3. 1 MHz − 142.517 dBc/Hz
4. 5 MHz − 142.937 dBc/Hz

Figure 4. Phase Noise of the HP8664A at 30.72 MHz
Phase Noise Performance of the CDC7005 at UMTS and CDMA Frequencies

1. 10 Hz − 77.0162 dBc/Hz
2. 1 kHz − 107.236 dBc/Hz
3. 1 MHz − 146.885 dBc/Hz
4. 5 MHz − 147.466 dBc/Hz
5. 10 MHz − 148.262 dBc/Hz

Figure 5. Phase Noise of the CDC7005 at 61.44 MHz Driven by HP8664A

1. 10 Hz − 77.1897 dBc/Hz
2. 1 kHz − 105.744 dBc/Hz
3. 1 MHz − 143.748 dBc/Hz
4. 5 MHz − 144.156 dBc/Hz
5. 10 MHz − 144.156 dBc/Hz

Figure 6. Phase Noise of the HP8664A at 61.44 MHz

Phase-Noise Performance of the CDC7005 at UMTS and CDMA Frequencies
1. 10 Hz − 78.0359 dBc/Hz
2. 1 kHz − 108.087 dBc/Hz
3. 1 MHz − 147.987 dBc/Hz
4. 5 MHz − 148.734 dBc/Hz
5. 10 MHz − 149.718 dBc/Hz

Figure 7. Phase Noise of the CDC7005 at 76.8 MHz Driven by HP8664A

1. 10 Hz − 77.9758 dBc/Hz
2. 1 kHz − 106.112 dBc/Hz
3. 1 MHz − 143.914 dBc/Hz
4. 5 MHz − 144.392 dBc/Hz
5. 10 MHz − 144.841 dBc/Hz

Figure 8. Phase Noise of the HP8664A at 76.8 MHz
Figure 9. Phase Noise of the CDC7005 at 78.6432 MHz Driven by HP8664A

Figure 10. Phase Noise of the HP8664A at 78.6432 MHz
Phase-Noise Performance of the CDC7005 at UMTS and CDMA Frequencies

1. 10 Hz − 76.6538 dBc/Hz
2. 1 kHz − 108.389 dBc/Hz
3. 1 MHz − 148.518 dBc/Hz
4. 5 MHz − 149.393 dBc/Hz
5. 10 MHz − 150.613 dBc/Hz

Figure 11. Phase Noise of the CDC7005 at 92.16 MHz Driven by HP8664A

1. 10 Hz − 77.7433 dBc/Hz
2. 1 kHz − 106.648 dBc/Hz
3. 1 MHz − 143.909 dBc/Hz
4. 5 MHz − 144.424 dBc/Hz
5. 10 MHz − 154.872 dBc/Hz

Figure 12. Phase Noise of the HP8664A at 92.16 MHz

Phase-Noise Performance of the CDC7005 at UMTS and CDMA Frequencies
1. 10 Hz − 76.8611 dBc/Hz
2. 1 kHz − 106.727 dBc/Hz
3. 1 MHz − 148.64 dBc/Hz
4. 5 MHz − 150.804 dBc/Hz
5. 10 MHz − 151.123 dBc/Hz

Figure 13. Phase Noise of the CDC7005 at 122.88 MHz Driven by HP8664A

1. 10 Hz − 79.3768 dBc/Hz
2. 1 kHz − 108.21 dBc/Hz
3. 1 MHz − 146.912 dBc/Hz
4. 5 MHz − 147.405 dBc/Hz
5. 10 MHz − 147.796 dBc/Hz
6. 40 MHz − 147.799 dBc/Hz

Figure 14. Phase Noise of the HP8664A at 122.88 MHz
1. 10 Hz − 87.637 dBc/Hz  
2. 1 kHz − 121.691 dBc/Hz  
3. 1 MHz − 154.294 dBc/Hz  
4. 5 MHz − 154.346 dBc/Hz  
5. 10 MHz − 154.286 dBc/Hz  
6. 40 MHz − 154.917 dBc/Hz

Figure 15. Phase Noise of the CDC7005 at 245.76 MHz Driven by HP8664A

1. 10 Hz − 87.8742 dBc/Hz  
2. 1 kHz − 120.598 dBc/Hz  
3. 1 MHz − 155.134 dBc/Hz  
4. 5 MHz − 155.144 dBc/Hz  
5. 10 MHz − 154.94 dBc/Hz  
6. 40 MHz − 156.072 dBc/Hz

Figure 16. Phase Noise of the HP8664A at 245.76 MHz
Phase-Noise Performance of the CDC7005 at UMTS and CDMA Frequencies

1. 10 Hz − 83.0617 dBc/Hz
2. 1 kHz − 115.261 dBc/Hz
3. 1 MHz − 151.95 dBc/Hz
4. 5 MHz − 152.654 dBc/Hz
5. 10 MHz − 152.8 dBc/Hz
6. 40 MHz − 153.369 dBc/Hz

Figure 17. Phase Noise of the CDC7005 at 491.52 MHz Driven by HP8664A

Phase Noise (Start: 10 Hz) Stop: 40 MHz

1. 10 Hz − 77.5303 dBc/Hz
2. 1 kHz − 114.707 dBc/Hz
3. 1 MHz − 154.733 dBc/Hz
4. 5 MHz − 155.218 dBc/Hz
5. 10 MHz − 155.272 dBc/Hz
6. 40 MHz − 155.579 dBc/Hz

Figure 18. Phase Noise of the HP8664A at 491.52 MHz
1. 10 Hz − 86.8405 dBc/Hz
2. 1 kHz − 132.619 dBc/Hz
3. 1 MHz − 146.408 dBc/Hz
4. 5 MHz − 146.945 dBc/Hz
5. >5 MHz − 147.566 dBc/Hz

Figure 19. Closed-Loop Phase Noise of the CDC7005 at 61.44 MHz

1. 10 Hz − 68.9273 dBc/Hz
2. 1 kHz − 134.918 dBc/Hz
3. 1 MHz − 146.210 dBc/Hz
4. 5 MHz − 147.044 dBc/Hz
5. >5 MHz − 147.765 dBc/Hz

Figure 20. Phase Noise of Toyocom 61.44 MHz VCXO
From the data above, it is evident that a low phase noise clock output is easily attainable from the CDC7005, with the proper selection of differential or single-ended VCXO’s.

### 4 Test Summary

The test results reveal that the CDC7005 can provide clock outputs better than $-145$-dBc/Hz phase noises at 1-MHz offset from the carrier frequency. Low phase noise is required for most base station application such as UMTS and CDMA and its derivatives as well as many other jitter stringent applications.

### 5 Acknowledgments

The authors of this application brief would like to thank the following people for proving the necessary samples and equipments in conducting these tests:

1. Doyce Ramey, Texas Instruments Inc., RF Wireless group, dramey@ti.com
2. Paul Woodley, O&M Sales, Inc., Paul.Woodley@o−m−sales.com
3. Micky Kilpatrick, Agilent Technologies, micky_kilpatrick@agilent.com

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