

Driving the TLK10002 10Gbps SERDES with the CDCM6208 Clock Generator

Falk Aliche, Matt Sunna, Jonathan Nerger, Max Robertson

Interface Products

ABSTRACT

The TLK10002 is 10Gbps Multi-Rate Transceiver. To enable a stable, error-free 10Gbps link, the device requires a reference clock with sufficient noise properties. The CDCM6208 is a highly integrated clock generator and jitter cleaner compatible with the TLK10002 reference clock requirements. The CDCM6208 derives its output clocks from an on-chip oscillator which can be buffered through integer or fractional output dividers. This application note provides a test report of the total system performance when combining the TLK10002 and the CDCM6208 together. The report provides verification of the TLK10002 meeting the system specification when driven by the CDCM6208. The report includes analysis of the transmit data eye opening, receiver jitter tolerance test, and a loop back test of the SERDES utilizing the recovered SERDES clock as a reference to the CDCM6208 to build a synchronous transmit and receive system. The CDCM6208 was used in three different modes during each test

1. Integer clock synthesizer mode
2. Integer clock jitter cleaner mode
3. Fractional clock divider mode

Transmit Jitter Data Eye

The TLK10002 offers data transmission for a variety of standards and input clock reference frequencies, including all CPRI and OBSAI data rates up to 9.8304Gbps. These standards are similar in their requirements for minimum transmit data eye opening, and require the data eye to be open by a minimum of 70%. At 10Gbps data transmission rate with a bit width of 100ps, this transmit mask translates into a jitter requirement of less than 30ps-pp Total Jitter (TJ) on the TLK10002 transmitter output. The combination of CDCM6208 and TLK10002 achieved the following performance with respect to this test:

First the CDCM6208 output was measured directly with the 40Gsp/s sampling scope. The total jitter of the 122.88MHz output clock derived from a 30.72MHz XTAL measured 7.7ps-pp. An ONET1191P limiting amplifier is used for this measurement to reduce the impact of the oscilloscope noise floor by sharpening the clock edges. The noise floor of this real-time scope is 1-2ps. Therefore, the RJ number of 1.2ps-rms reported on the oscilloscope is limited by the noise floor and a phase noise analyzer is required for an accurate measurement. The actual CDCM6208 random jitter in this configuration measured by a phase noise analyzer is 263fs-rms.

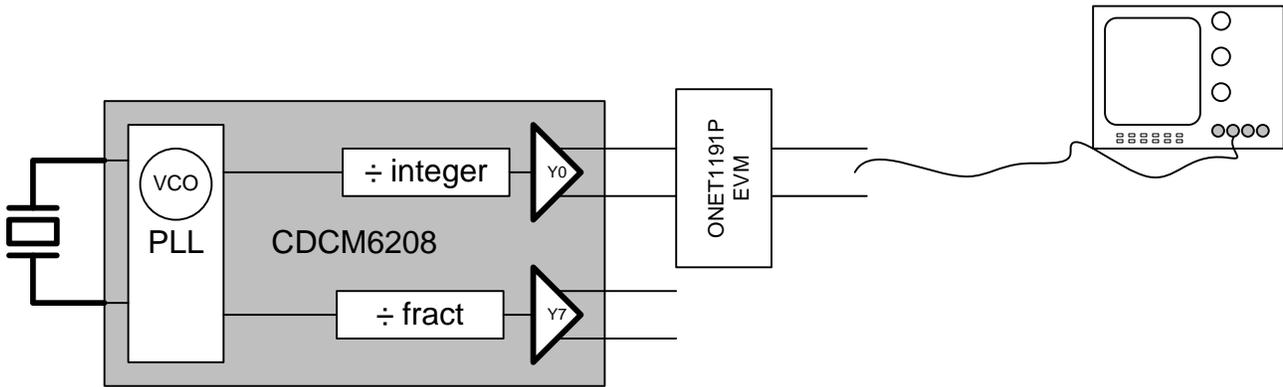


Figure 1. CDCM6208 output jitter measured directly on the CDCM6208 clock output

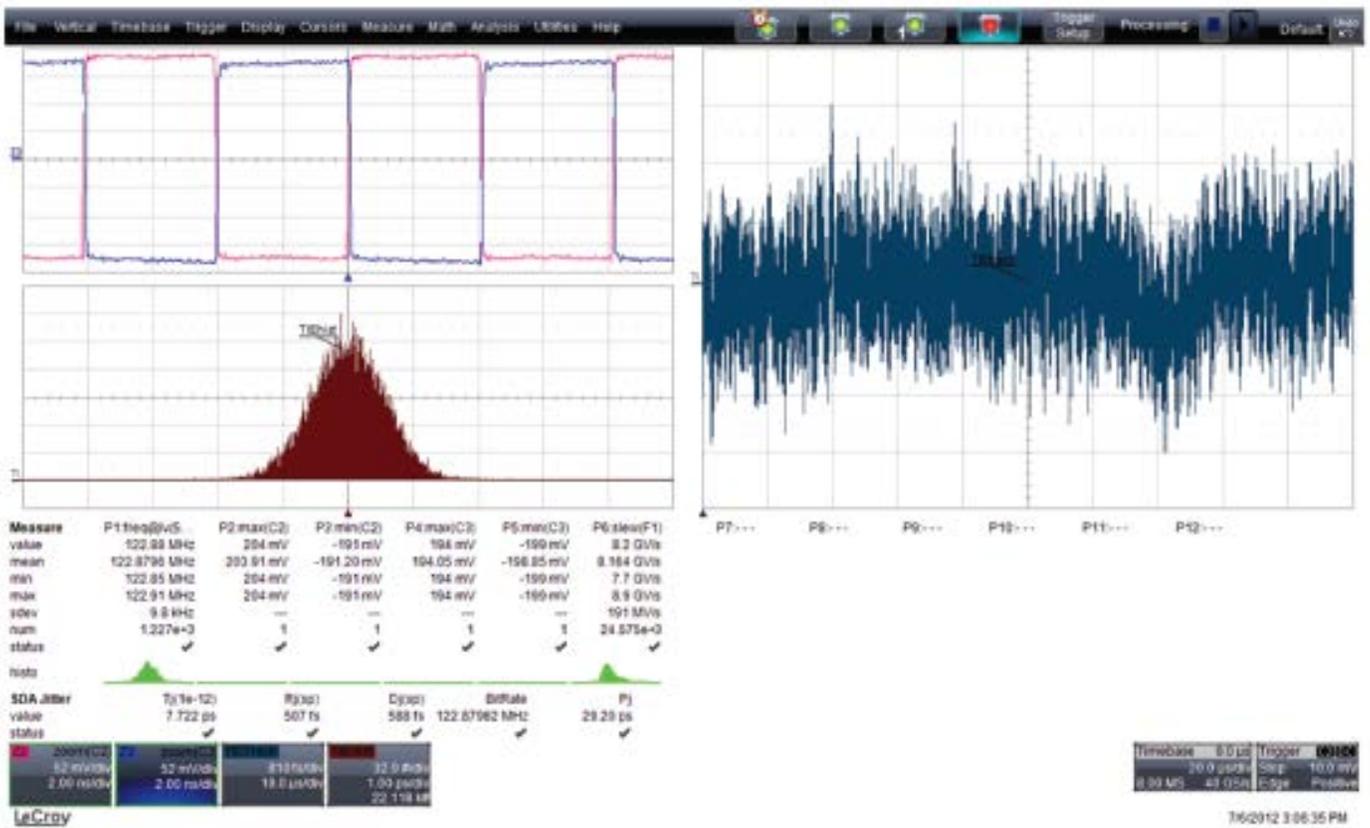


Figure 2. CDCM6208 output jitter 7.7ps-pp

For all other transmitter mask tests, the following test setup was used (either with Y0 or Y4 connected to the TLK10002 reference clock input):

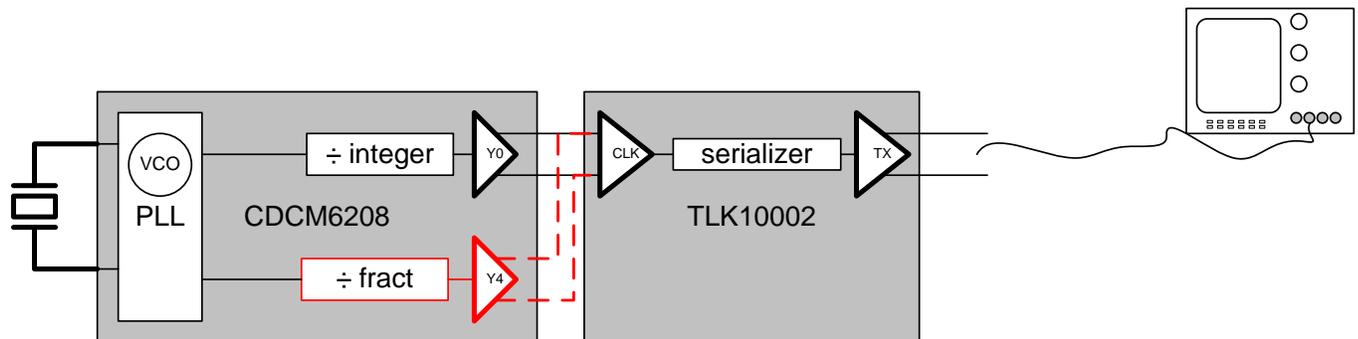


Figure 3. TLK10002 and CDCM6208 test configuration for all further transmitter mask tests

The TLK10002 was then driven from this 122.88MHz reference clock to output a 1010 repeating output signal at 9.8304Gbps. The TJ measured 18.3ps-pp

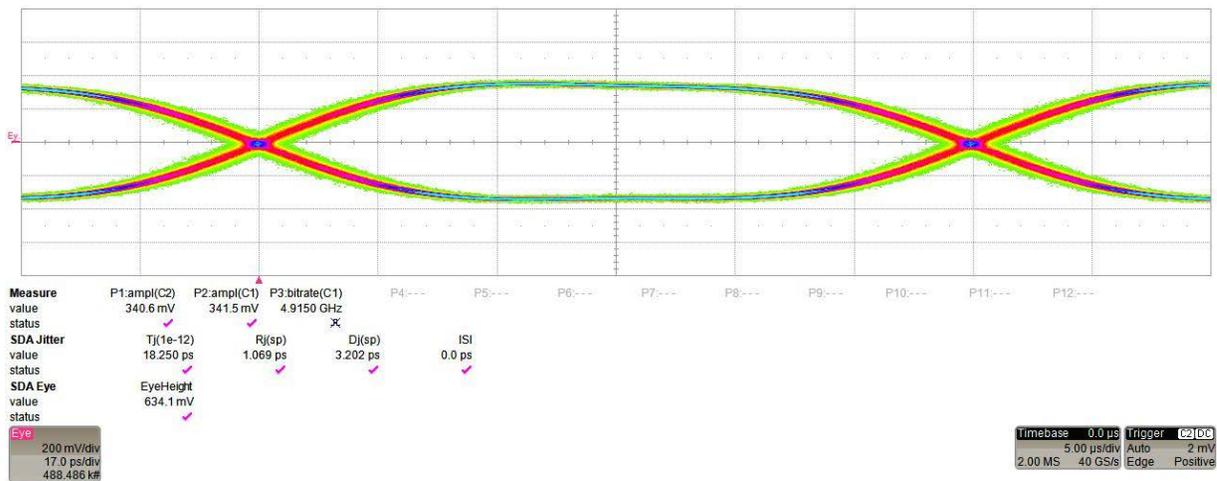


Figure 4. TLK10002 TX output jitter of a 1010-pattern driven by 122.88MHz clock: 18.3ps-pp

Next the TLK10002 was driven from this 122.88MHz reference clock to output an output signal of 9.8304Gbps using a PRBS test pattern. The TJ measured 22.1ps-pp, 8ps below the allowed budget of 30ps. The performance was compared to driving the TLK10002 from a standard lab reference clock and it was found that the TLK10002 performs equal or better driven by the CDCM6208 compared to the lab clock source. It also did not matter which output type CDCM6208 was selected (that is, CDCM6208 output Y0 with PECL signal swing performed nearly identical as Y4 configured to drive LVDS signal swing). Increasing the CDCM6208 output frequency to a higher frequency enhances the overall performance further. This is because the TLK10002 internal frequency multiplication required to generate 10GHz is smaller, and also, the CDCM6208 output phase noise floor is less of a limitation.

- ☑ 122.88MHz integer mode: 8ps margin
- ☑ 153.6MHz integer mode: 9ps margin
- ☑ 245.76MHz integer mode: 11ps margin

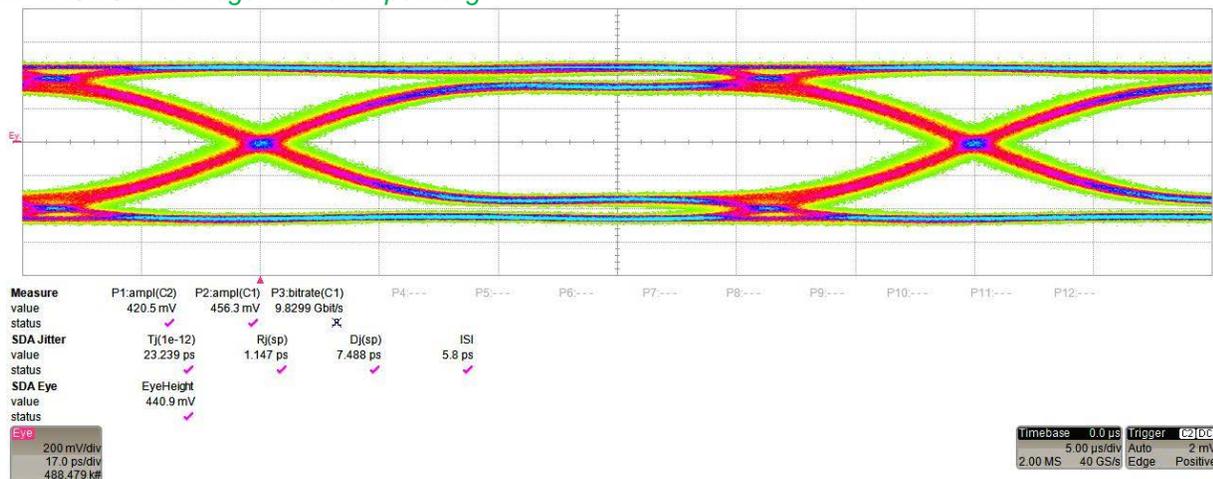


Figure 5. TLK10002 TX output jitter driven by 122.88MHz clock from lab reference: 22.3ps-pp

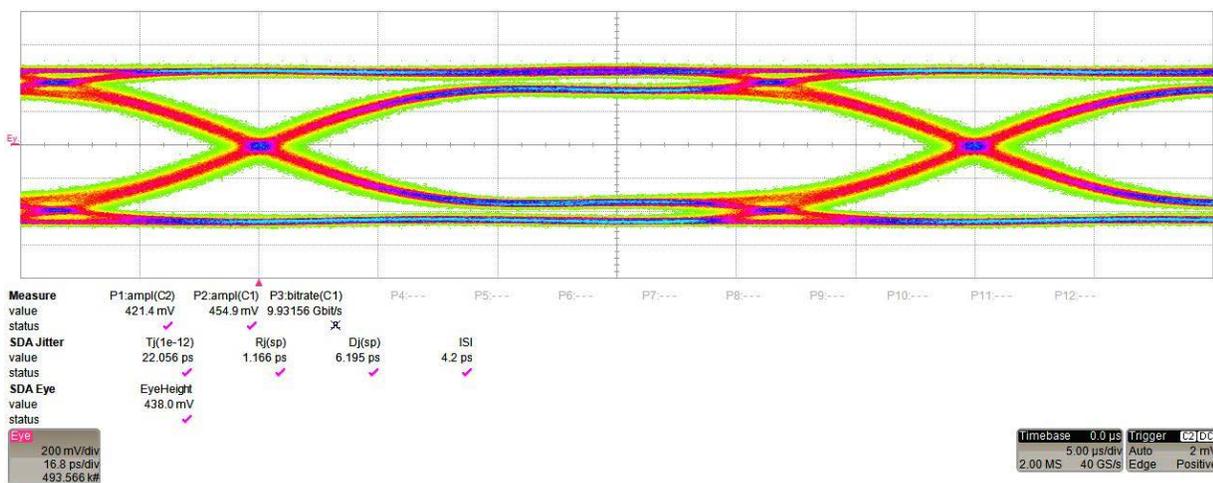


Figure 6. TLK10002 TX output jitter driven by 122.88MHz clock from CDCM6208 Y0 (PECL): 22.1ps-pp

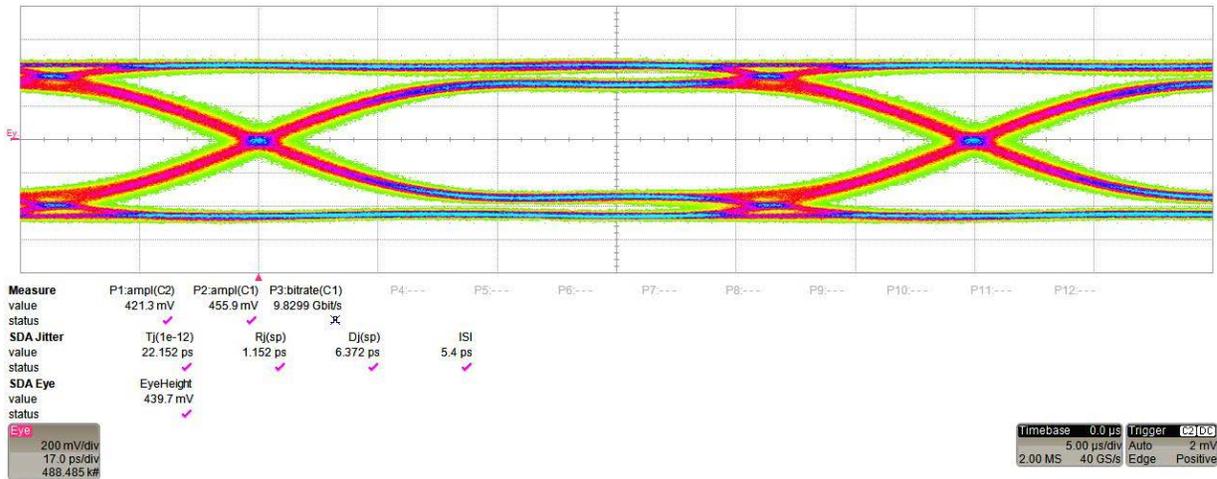


Figure 7. TLK10002 TX output jitter driven by 122.88MHz clock from CDCM6208 Y4 (LVDS): 22.2ps-pp

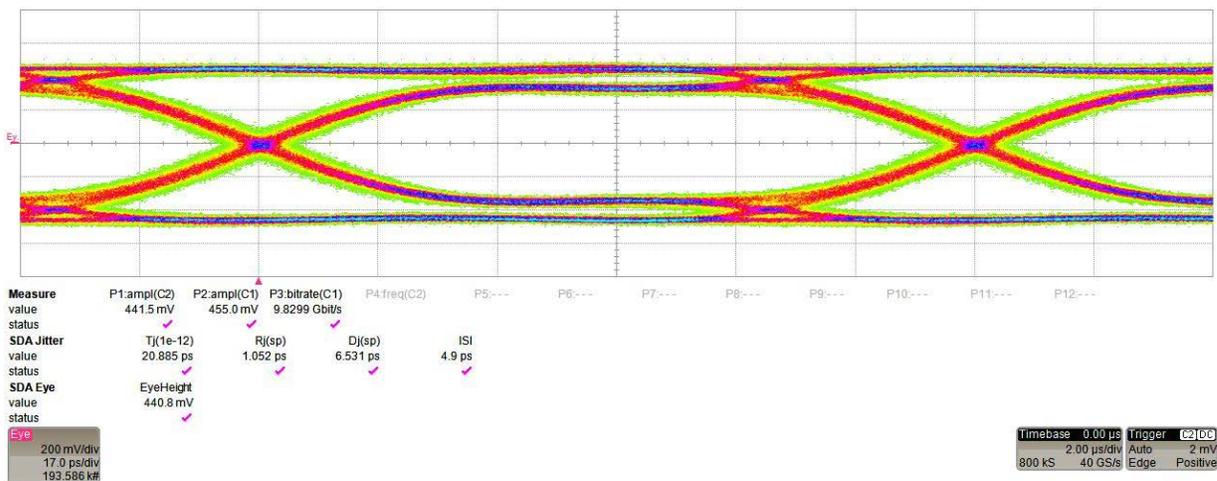


Figure 8. TLK10002 TX output jitter driven by 153.6MHz clock from CDCM6208: 20.9ps-pp

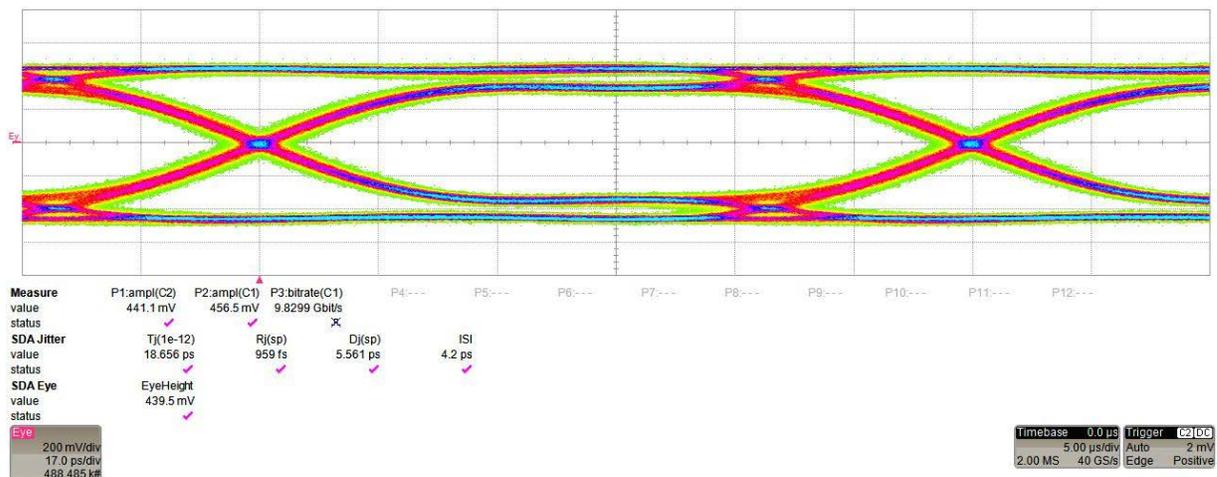


Figure 9. TLK10002 TX output jitter driven by 245.76MHz clock from CDCM6208: 18.7ps-pp

The CDCM6208 enables very flexible frequency planning with fractional output dividers that enable multiple unrelated frequencies from a single clock generator. Driving the TLK10002 from a fractional down-divided signal of the CDCM6208 from 30.72MHz XTAL at 156.25MHz meets the overall transmitter jitter specification if the fractional divider is configured to utilize only a minimum number of bits. The fractional divider allows exercising up to 20-bit depth. Engaging more bits improves the frequency accuracy at the expense of jitter. Most systems require a reference clock better than ± 100 ppm. Therefore two measurements were taken, one with the full 20-bit fractional division utilized (less than 0.06ppm frequency error), and another with only 6-bit fractional division, resulting in 33ppm frequency error. While the 20-bit test violates the TX mask slightly, the 6-bit configuration easily meets the overall CPRI transmit mask jitter spec.

Fractional divider setting $FRACDIV[19:0]=5BFADh$ (20-bit) vs. $FRACDIV[19:0]=5C000h$ (6-bit)

- 156.25MHz fractional divider output with 20-bit deep division: -2.6ps margin
- 156.25MHz fractional divider output with 6-bit deep division: 3.5% margin

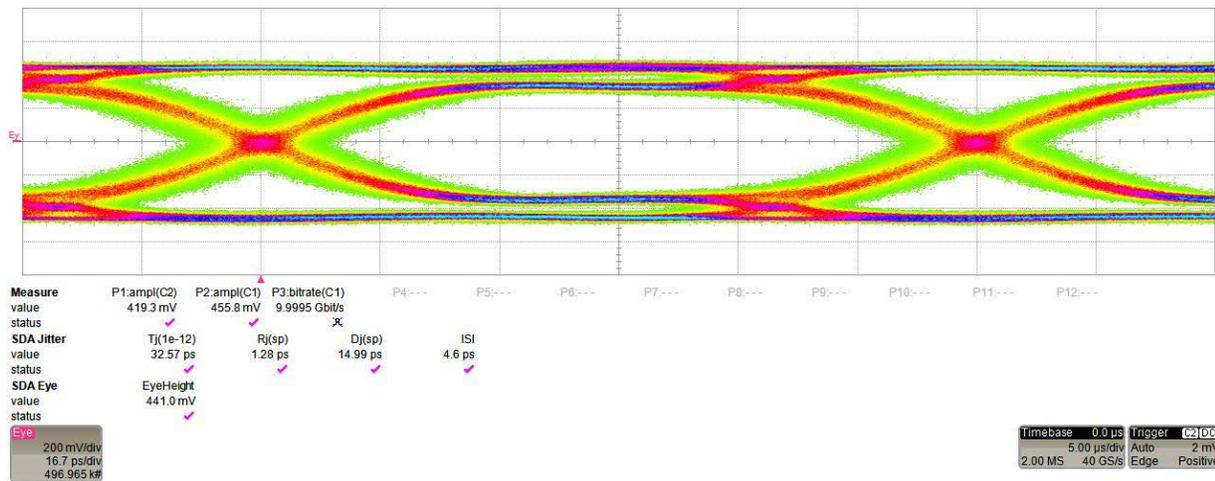


Figure 10. TLK10002 TX output jitter driven by 156.25MHz derived fractional divider with full 20-bit dept and therefore only 0.06ppm frequency error: 32.6ps

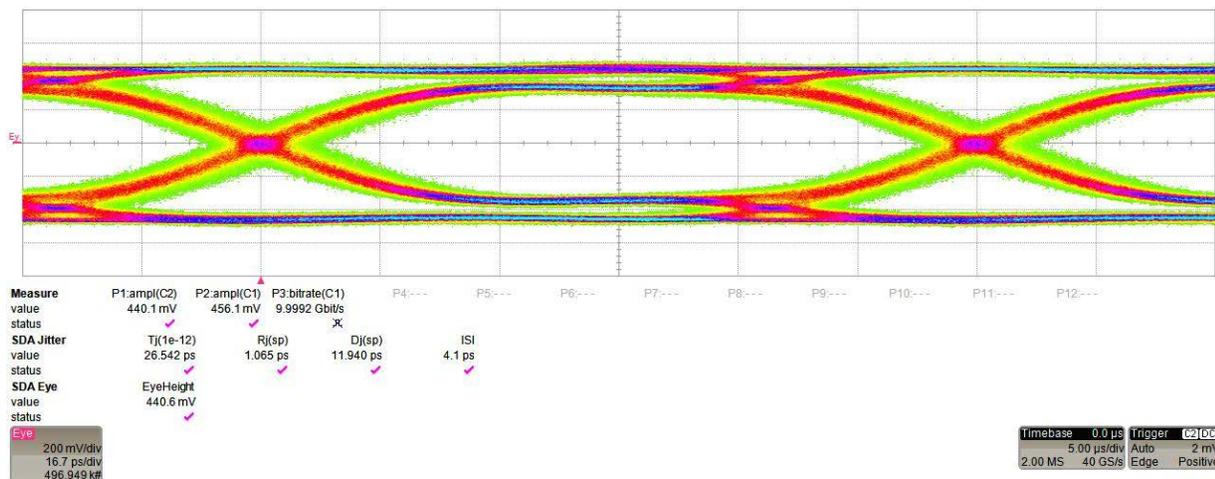


Figure 11. TLK10002 TX output jitter driven by 156.25MHz derived from fractional divider with 33ppm frequency error, therefore only using 6-bit fractional division: 26.5ps

The observation made at 156.25MHz also holds true when testing the system with a 312.5MHz reference clock. The CDCM6208 and TLK10002 combination meet the overall transmitter jitter specification if the fractional divider is configured to utilize only 6 bits but not when all 20 bits are utilized. The 20-bit fractional division in this would meet -0.3ppm frequency error, while the 6-bit deep fractional division established an output frequency with -33ppm frequency error, well within the ± 100 ppm maximum spec typically required.

Fractional divider setting $FRACDIV[19:0]=2DFD7h$ (20-bit) vs. $FRACDIV[19:0]=2E000h$ (6-bit)

- ❑ 312.5MHz fractional divider output with 20-bit deep division: -1.9ps margin
- ❑ 156.25MHz fractional divider output with 6-bit deep division: 3.5% margin

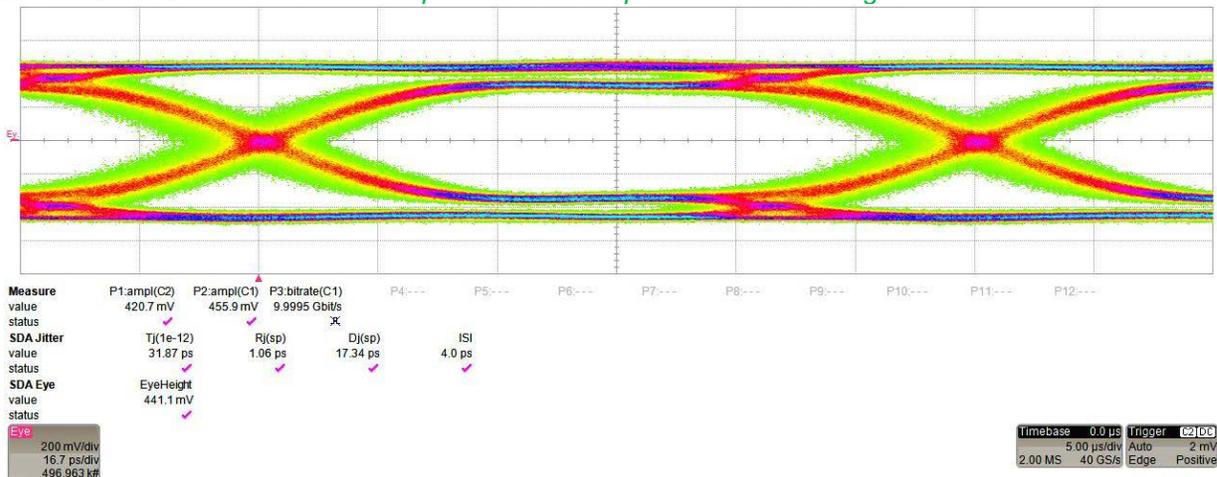


Figure 12. TLK10002 TX output jitter driven by 312.5MHz derived fractional divider with full 20-bit depth and therefore only 0.06ppm frequency error: **31.9ps**

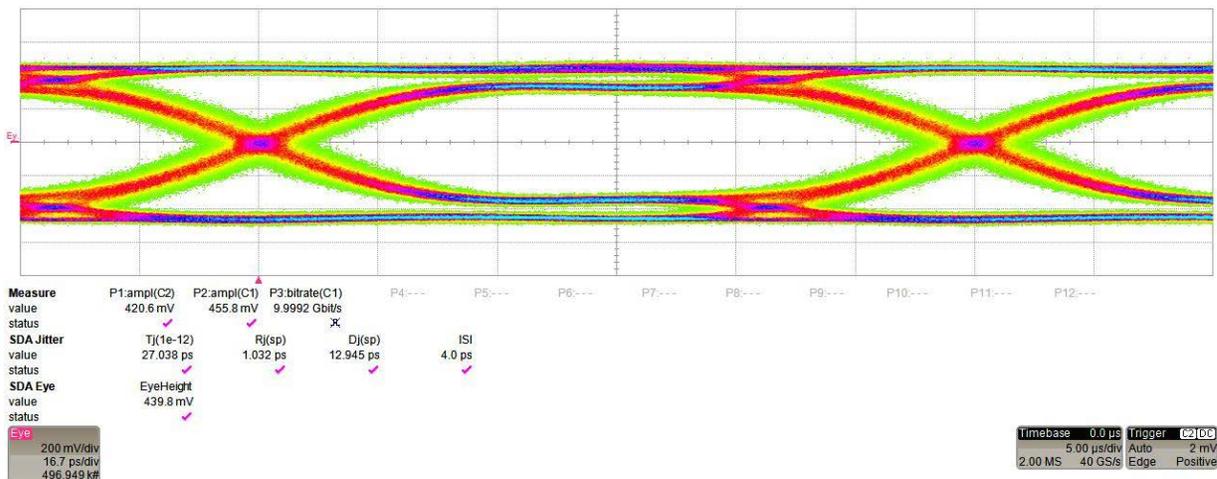


Figure 13. TLK10002 TX output jitter driven by 312.5MHz derived from fractional divider with 33ppm frequency error, therefore only using 6-bit fractional division: **27ps**

Summary of the transmitter jitter tolerance test

If the TLK10002 clock signal can be derived with integer division from the CDCM6208 internal PLL frequency, the overall transmitter jitter is equal to or less than a very clean lab clock supply. The CDCM6208 in this mode is a superior clock source for the TLK10002.

More care is needed for the frequency planning if the CDCM6208 PLL frequency is operated at a non-integer multiple of the TLK10002 desired reference frequency. One such case is if the CDCM6208 is required to generate a 122.88MHz reference clock to an antenna interface, while the TLK10002 requires a clock to enable a data rate of 10Gbps. In this case, with careful configuration of the fractional divider the overall transmitter output jitter mask can in many configurations still pass. An example is to generate a 156.25MHz clock from a 2949.12MHz VCO frequency by using a 6 bit fractional divider of 2.359375. For more information on optimizing the fractional dividers, visit <http://www.ti.com/product/cdc6208> for the datasheet, EVM software, and instructional videos.

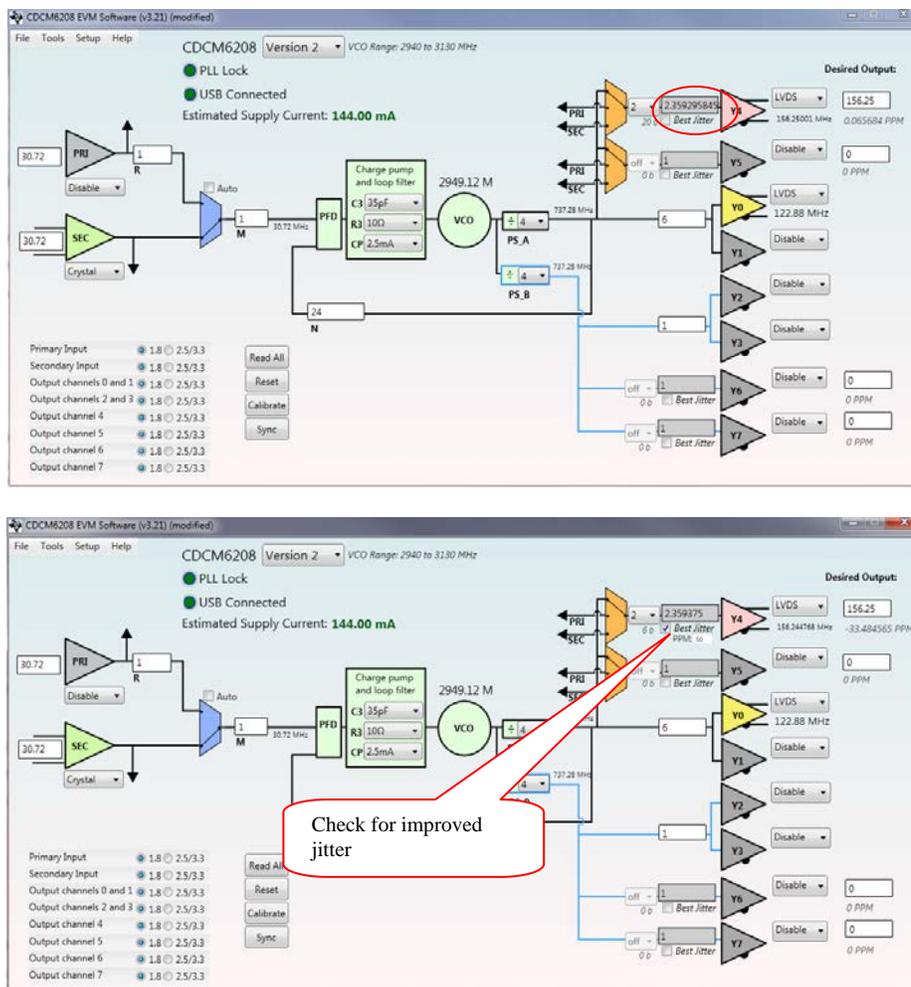


Figure 14. Example of system with 30.72MHz reference clock and 122.88MHz output, in which the actual TLK10002 would be driven from a 156.25MHz reference from output Y4; The configuration on the left (a) enables a 20-bit division on output Y4, which elevates jitter beyond the allowable transmitter jitter mask. The configuration to the right (b) utilizes only 6 bits of the fractional divider and ends up meeting the overall jitter specification of the TLK10002 output.

Receiver Jitter Tolerance

The next test performed was with the TLK10002 receiver. For the test, a transmit signal was generated by a signal generator (Agilent J-Bert) allowing to modulate random and DJ components. Jitter was configured such that it presented the maximum allowable jitter on the RX input. The recovered data signal on the TLK10002 was then verified for bit errors over an observation period of at least 5 minutes. A test passed if within this observation window no bit error occurred. The CDCM6208 reference clock generator was again adjusted in frequency plan identical to the tests already described during the transmitter transmit test.

☑ All tests passed the receiver jitter specification flawlessly.

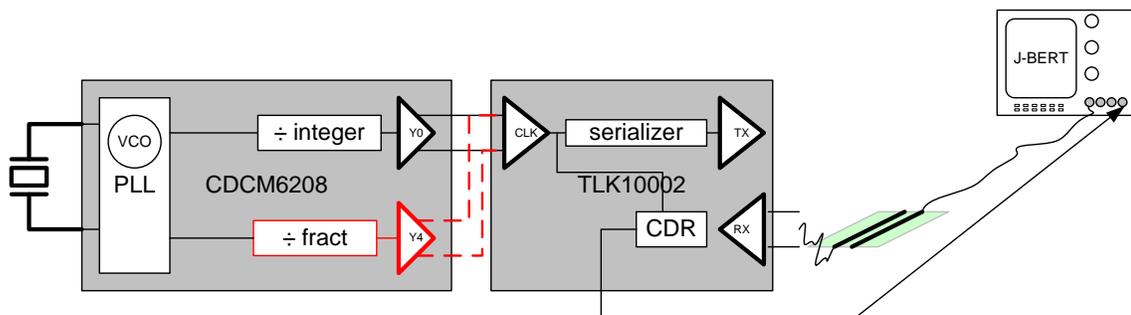


Figure 15. Test setup for Receiver jitter tolerance

To see the amount of additional margin available in the jitter tolerance test, the data signal from the J-BERT was furthermore modulated with a sinusoidal noise source. The amplitude was varied until a bit error rate of roughly 10^{-11} was observed. Clocking the TLK10002 from the CDCM6208 in integer output mode achieved the same performance as when using a lab clock source. Using the CDCM6208 fractional divider as the TLK10002 clock source cut the total margin into approximately half, which is sufficient in the application. For example, if with the lab source the additional sinusoidal jitter caused a 10% extra eye closure, the fractional jitter would cut this margin to 5% only, which is still sufficient margin for the application. Overall this means that the CDCM6208 with fractional divider can drive a TLK10002 receiver reference clock effectively and reliably.

Loop Back test

The final test consisted of the Receiver recovering a clock from the J-BERT generated stressed data signal. This recovered clock is brought out of the TLK10002 into the CDCM6208. The CDCM6208 cleans this clock signal up and feeds it back to the TLK10002 as a clock reference, driving now the TLK10002 output. Therefore the transmitter output mask test is not only stressed due to the fractional output divider, but also because the CDCM6208 functions as a jitter cleaner, conditioning the TLK10002 recovered RX clock.

The loop back test passed the transmitter jitter tolerance with the same performance level as already described in the transmit jitter mask test. The CDCM6208 was able to sufficiently clean the TLK10002 recovered clock and no significant signal degradation was noticed.

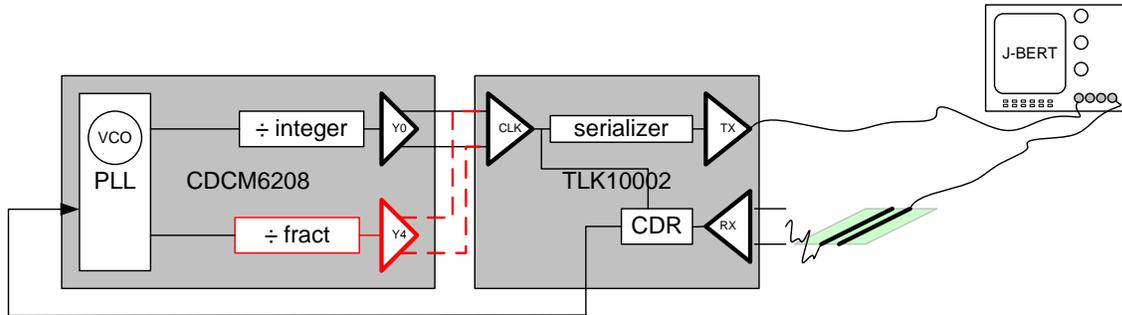


Figure 16. Loop Back Test: the TLK10002 recovered clock is cleaned within the CDCM6208 and fed back as reference clock to the TLK10002

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