

# ***32-Bit Logic Families in LFBGA Packages:***

***96 and 114 Ball  
Low-Profile Fine-Pitch BGA Packages***

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**Philips  
Semiconductors**



**32-Bit Logic Families in LFBGA Packages:  
96 and 114 Ball Low-Profile Fine-Pitch BGA Packages**

**Application Note**

*October 26th, 1998 by:*

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# 1 Introduction

With increasing systems and circuit complexity and the constant downward pressure on system prices, the requirements for bus interface solutions demand new approaches to system needs. One of the major challenges and goals of the digital processing industry is to continue decreasing the overall system costs as system complexity increases. Consequently, circuit integration and board miniaturization have become key words and key trends in present and future applications. A direct consequence of these trends is the need for wider bus interfacing. Today, as many networking, telecom and computer systems begin using DSP's and MPU's that require 32-bit, or even 64-bit wide interfacing, there is an increasing demand for 32-bit wide buffer, driver and transceiver functions. These new functions will become the standard in the years to come. To address evolving customer requirements, three suppliers, Integrated Device Technology, Philips Semiconductors and Texas Instruments have come together to define a package for 32-bit functions. Collectively Integrated Device Technology, Philips Semiconductors and Texas Instruments evaluated many customer inputs and identified a Low-Profile Fine-Pitch Ball Grid Array (LFBGA) package solution that would best serve customers' needs. Studies have shown that the LFBGA is an optimal solution for reducing the inductance, improving thermal performance and minimizing board real estate in support of integrated bus functions. Together, our objective is to provide multi-source products in a package that enables significant electrical improvements when compared to existing packages, as well as cost savings to the OEM manufacturing process. From a supplier standpoint, we can now guarantee the multi-sourcing of a package that will become the standard in the very near future.

The purpose of this document is to discuss the two new LFBGA solutions, the 96 and 114 ball LFBGA packages. Five 32-bit functions will initially be introduced in LFBGA package. Additional products will be manufactured per market interest and customer demand. A definition and description of the 96 and 114 ball LFBGA packages are discussed in this application note. Content and technical exhibits from the application note should be used to develop PCB layouts using the 96 and/or 114 ball LFBGA packages. Examples of routing, layout and mechanical dimensions are also included in this document. The initial introduction of the 32-bit logic is noted in the table below:

LVCH Functions	Number of Balls			
	Package	GND	V <sub>CC</sub>	No Connection
74LVCH32244	96	16	8	NA
74LVCH32245	96	16	8	NA
74LVCH32373	96	16	8	NA
74LVCH32374	96	16	8	NA
<b>ALVCH Function</b>				
74ALVCH32501	114	16	8	2

**Table 1.1 – Initial 32-Bit Functions**

LFBGA packages offer lower inductance and parasitic capacitance than any other TSSOP, TVSOP and Millipaq™ packages. The LFBGA package characteristics supports improvements in ground bounce,  $V_{CC}$  undershoot, pin-to-pin skew, and signal propagation delay of 20 to 50 ps.

The definition of these two packages in terms of standardization, both physical and mechanical, was developed by Integrated Device Technology, Philips Semiconductors and Texas Instruments to provide the industry pin out compatible solutions.



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## 2 Examples of Applications with LFBGA Packages

### 2.1 Industry Expressed Requirements for 32-Bit Logic

With the growing trend towards increased bus widths, OEMs are looking to consolidate logic functions in an effort to effectively make use of board real estate. This requirement from customers is prevalent across many end equipments. The requirement to reduce board real estate also necessitates a packaging solution, which integrates logic as well as addresses improved thermal packaging characteristics in addition to minimizing pin-to-pin skew. The selection of the 96 and 114 Ball LFBGA addresses all of these careabouts with improved performance and standardization of pin outs agreed upon by Integrated Device Technology, Philips Semiconductors and Texas Instruments. In the initial 8 month study, consisting of 15 OEMs and several worldwide subcontractors, we found that the preferred pitch for introducing logic in either the LFBGA is a 0.8 mm with a 0.5 mm ball diameter. Both packages are being offered by Integrated Device Technology, Philips Semiconductors and Texas Instruments to support customer requirements and enable easier PCB design/layout along with a more robust solder joint based on life cycle studies.

While other solutions were looked at such as staggered depopulated balls, with a smaller pitch, as well as, a smaller ball diameter, none were considered suitable to address the current market needs for OEM's and the subcontractors. The LFBGA packages selected by IDT, Philips Semiconductors and Texas Instruments is the optimal solution as it addresses our current customer needs. More details for package comparison are noted within the other subsections of this application note.

### 2.2 Customer Needs and Problems Targeted

#### **Workstations:**

- Workstation buses extend to 128-, 256-bit, or wider bus structures
- Require denser and faster logic products

#### **PCs:**

- The trend is to integrate as much logic as possible into fewer packages
- Due to space constraint, PC Cards require dense integration and small package foot-prints
- PCI bus structures may require 5-V tolerance, in addition to integrating logic circuits

#### **Datacommunication:**

“Intelligent” routers and switches require more logic to support interfaces and build real time lookup tables for routing addresses with statistics.

### Telecommunication:

- Base stations are becoming small and ubiquitous requiring the repackaging of many circuits into dense boards
- New complex and smaller equipment must interface with legacy equipment.

## 2.3 Application Examples

- PC Motherboards
- Data communications
- Telecommunications
- Back Planes
- Base stations
- Cellular and cordless telephone

## 2.4 Existing or Alternative Solutions: A Comparison

While other packages have been introduced to address integrated logic solutions, these packages have only had limited success, such as the 100-pin TQFPs or the 80/96-pin MillipaQ™. As a comparison, these two solutions have a reduce number of ground and V<sub>CC</sub> pins leading one to believe that ground bounce and pin-to-pin skew cannot be optimally designed to address these design issues.

Comparisons of the foot print space show that the 100-pin TQFP and 80/96-pin MillipaQ™ packages takes up respectively 245% and 66% more area than the corresponding 96 ball LFBGA. For further details refer to tables 2.1 and 2.2.

The 96 ball LFBGA package provides an optimal area/bit ratio and improved pin-to-pin skews. Pin-to-pin skew is minimized by the number of pin signals connected to the same ground connection.

Package	Footprint Area (mm <sup>2</sup> )	Area/Bit (mm <sup>2</sup> )	Weight (g)	Total # of Balls or Pins
LFBGA-96	74.25	2.32	0.132	96
MillipaQ™ 80/96 pin	123.0	3.84	0.332	80/96
2 x TVSOP 48 pin	132.5	4.14	0.227	96
2 x TSSOP 48 pin	213.0	6.66	0.383	96
2 x SSOP 48 pin	342.0	10.7	1.180	96
TQFP 100 pin	256.0	8.00	0.660	100

Note 1: The Area/Bit is computed for 32 bits and assumes a 1.3 mm PCB spacing for two-package solution.

Note 2: The MillipaQ™ offers 32-bit logic functions with reduced ground and V<sub>CC</sub>'s; such configuration compromises the signal integrity of the logic functions.

**Table 2.1 – Comparison of Foot Print Size with LFBGA-96**

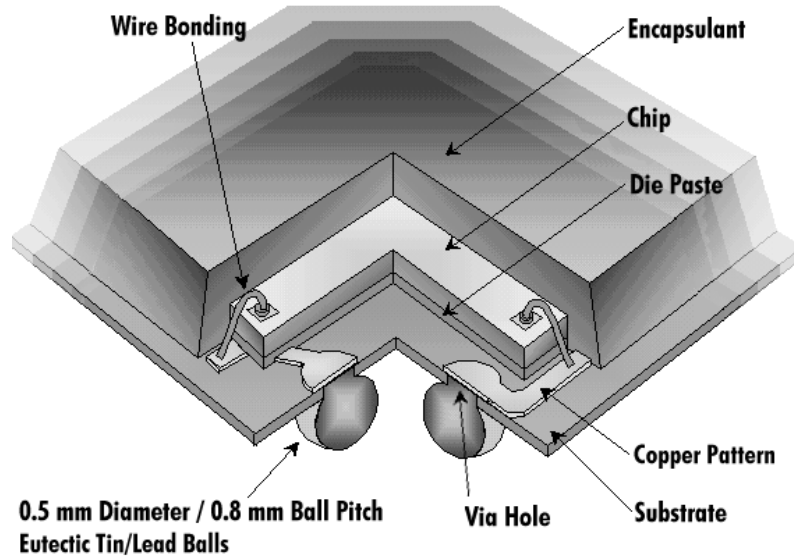
<b>Package</b>	<b>Footprint Area (mm<sup>2</sup>)</b>	<b>Area/Bit (mm<sup>2</sup>)</b>	<b>Weight (g)</b>	<b>Total # of Balls or Pins</b>
LFBGA-114	88.00	2.44	0.167	114
2 x TVSOP 56 pin	153.0	4.25	0.271	112
2 x TSSOP 56 pin	237.3	6.59	0.423	112
2 x SSOP 56 pin	394.6	11.0	1.360	112
TQFP 120 pin	256.0	7.11	0.660	120

Note 1: The Area/Bit is computed for 36 bits and assumes a 1.3 mm PCB spacing for two-package solution.

**Table 2.2 - Comparison of Foot Print Size with LFBGA-114**

### 3 Package Descriptions

Figure 3.1 shows a cross section of the LFBGA package.



**Figure 3.1 - LFBGA Cross Section**

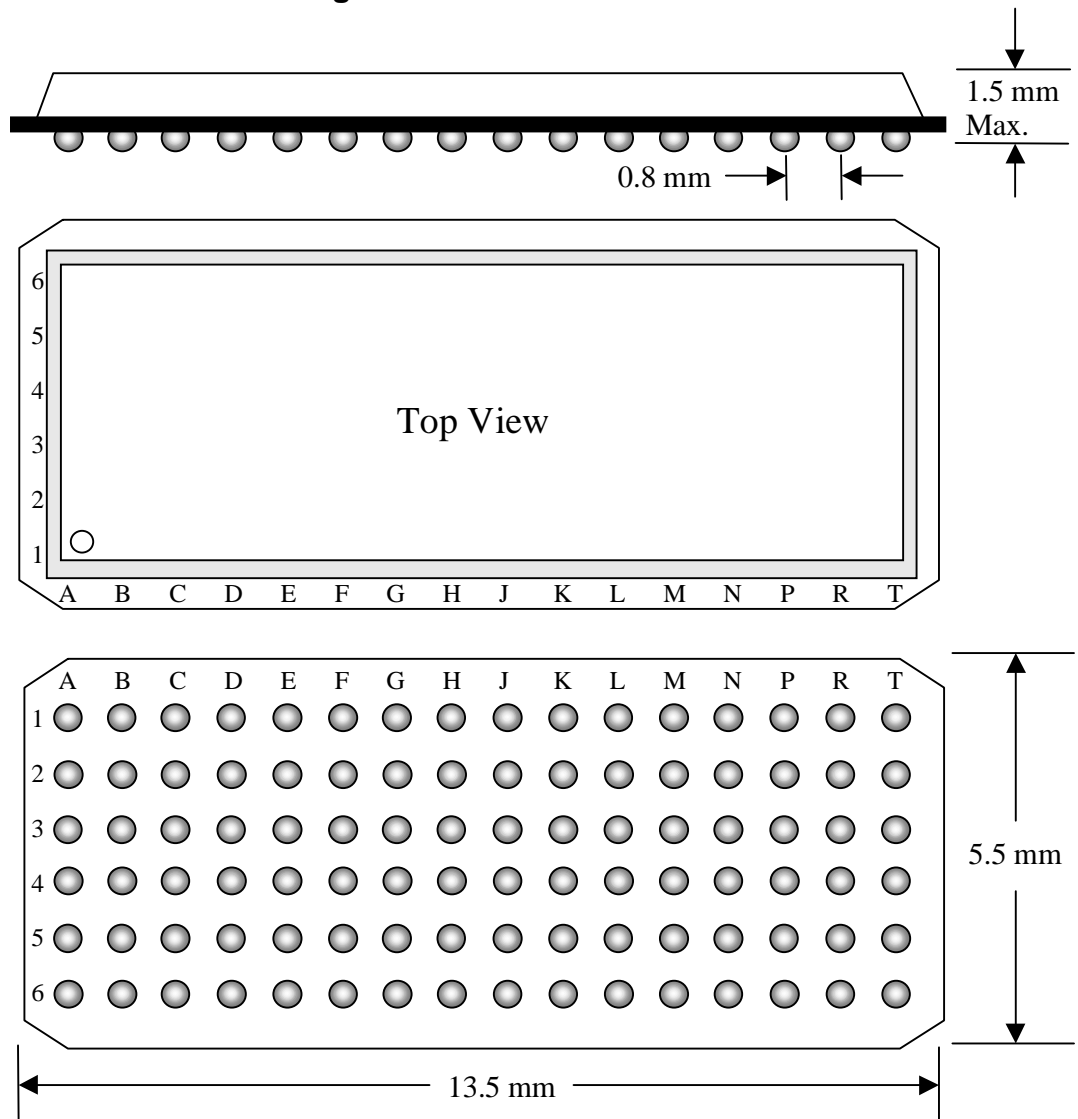
Table 3.1 summarizes the package attributes for the LFBGA.

	<b>LFBGA-96</b>	<b>LFBGA-114</b>
Ball count	96	114
Ball configuration (rows, columns)	6 x 16	6 x 19
Square/Rectangular	R	R
Ball-to-ball pitch (mm)	0.8	0.8
Ball diameter (mm)	0.5	0.5
Package body width (mm)	5.5	5.5
Package body length (mm)	13.5	16
Package thickness (mm)	1.2 min – 1.5 max	1.2 min – 1.5 max
Package weight (mg)	132	167
Shipping media tape & reel (units)	1000	1000
Desiccant pack	Level 3	Level 3

**Table 3.1 – LFBGA Package Attributes**

### 3.1 LFBGA Package Characteristics

#### 3.1.1 LFBGA-96 Package Dimensions



Ball organization: 6 x 16 = 96 balls; grid = 0.8 mm;  
Footprint: 74.25 mm<sup>2</sup>

**Figure 3.2 - LFBGA-96 Package Layout**

#### **Advantages:**

- Industry accepted 0.8 mm pitch industry standard; easy pad-via-to-ball routing
- Easy customer PCB layout; easy to locate near connectors
- Robust solderability due to standard 0.5 mm ball size

### LFBGA-96 Pin Out Configuration:

Note: The pin out configuration below adopts the same naming convention applied in the industry to logic devices in 48-pin packages (i.e. TSSOP, SSOP, TVSOP).

6	A46	A43	A40	A37	A35	A32	A29	A27	B46	B43	B40	B37	B35	B32	B29	B27
5	A47	A44	A41	A38	A36	A33	A30	A26	B47	B44	B41	B38	B36	B33	B30	B26
4	A48	A45	A42	A39	A34	A31	A28	A25	B48	B45	B42	B39	B34	B31	B28	B25
3	A1	A4	A7	A10	A15	A18	A21	A24	B1	B4	B7	B10	B15	B18	B21	B24
2	A2	A5	A8	A11	A13	A16	A19	A23	B2	B5	B8	B11	B13	B16	B19	B23
1	A3	A6	A9	A12	A14	A17	A20	A22	B3	B6	B9	B12	B14	B17	B20	B22
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T

Gnd

Vcc

Control

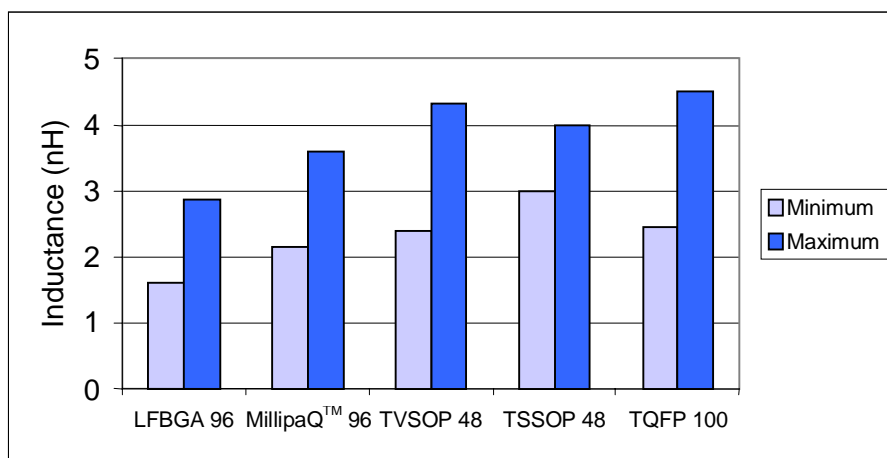
Note: This is a topside view

**Figure 3.3 – Top View Pin Assignment**

### Electrical:

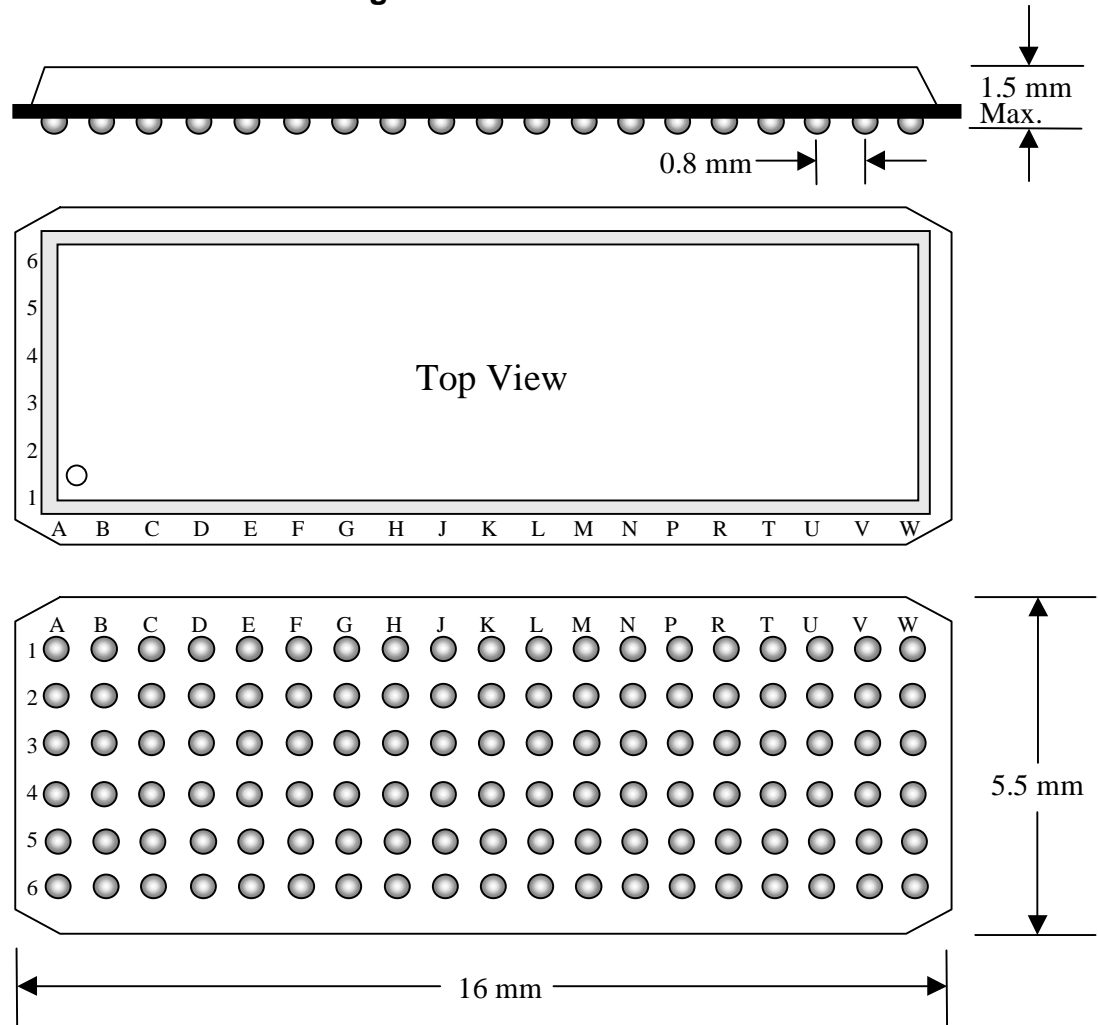
The electrical parameters of a package are dependant upon parasitic elements, which include inductance, capacitance, and electrical or propagation delays throughout the package. The following values summarize the nominal parasitic components of the LFBGA-96 package: self inductance 2.2nH, pin-to-ground capacitance 0.2pF. One should note that the reported values for the LFBGA package are about 35% better than the TVSOP package and greater that 50% compared to the TSSOP package. Overall the LFBGA package is better than any existing industry standard package on the market today.

Figure 3.4 provides an electrical comparison of the LFBGA-96 with other industry standard packages.



**Figure 3.4 - Electrical Comparisons**

### 3.1.2 LFBGA-114 Package Dimensions



Ball organization: 6 x 19 = 114 balls (112 used); grid = 0.8 mm;

Footprint: 88 mm<sup>2</sup>

**Figure 3.5 - LFBGA-114 Package Layout**

**Advantages:**

- Industry accepted 0.8 mm pitch; easy pad-via-to-ball routing
- Easy customer PCB layout; easy to locate near connectors
- Robust solderability due to standard 0.5 mm ball size

### **LFBGA-114 Pin Out Configuration:**

Note: The pin out configuration below adopts the same naming convention applied in the industry to logic devices in 56-pin packages (i.e. TSSOP, SSOP, TVSOP).

6	A52	A49	A47	A44	A42	A40	A37	A36	A33	NC	B52	B49	B47	B44	B42	B40	B37	B36	B33
5	A54	A51	A48	A45	A43	A41	A38	A34	A31	B55	B54	B51	B48	B45	B43	B41	B38	B34	B31
4	A55	A56	A53	A50	A46	A39	A35	A32	A30	A29	B56	B53	B50	B46	B39	B35	B32	B30	B29
3	A2	A1	A4	A7	A11	A18	A22	A25	A27	A28	B1	B4	B7	B11	B18	B22	B25	B27	B28
2	A3	A6	A9	A12	A14	A16	A19	A23	A26	B2	B3	B6	B9	B12	B14	B16	B19	B23	B26
1	A5	A8	A10	A13	A15	A17	A20	A21	A24	NC	B5	B8	B10	B13	B15	B17	B20	B21	B24
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W

<div style="border: 1px solid black; background-color: #f08080; width: 40px; height: 15px; margin: 0 auto;"></div> <p>Gnd</p>	<div style="border: 1px solid black; background-color: #00b0f0; width: 40px; height: 15px; margin: 0 auto;"></div> <p>Vcc</p>	<div style="border: 1px solid black; background-color: #ffff00; width: 40px; height: 15px; margin: 0 auto;"></div> <p>Control</p>	<div style="border: 1px solid black; background-color: #cccccc; width: 40px; height: 15px; margin: 0 auto;"></div> <p>GND or Control</p>	
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Note: This is a topside view

**Figure 3.6 – Top View Pin Assignment**

### **Electrical:**

The electrical parameters of a package are dependent upon parasitic elements, which include inductance, capacitance and electrical propagation delays throughout the package. One should note that the reported values for the LFBGA-114 package are about 35 % better than the TVSOP package and greater than 50 % compared to the TSSOP package. Overall the LFBGA packages are better than any existing industry standard package on the market today.



### 3.1.3 LFBGA Power Dissipation

The power dissipation of LFBGA is very much dependent upon the thermal conduction paths between the chip and the printed circuit board (PCB). The 96 and 114 ball LFBGA package outline is small, thereby limiting the amount of power dissipation due to convection or radiation, so the PCB becomes the major heat source for the package. The thermal performance of the packages is good when the chip overlaps the solder balls due to the fact that the balls under the chip act as thermal conduction paths to the PCB. The thermal resistance of LFBGA packages is 35% better than the TVSOP package and 30% better than the TSSOP package.

A well-designed PCB board further enhances the power dissipation of both LFBGA packages. By adding thermal vias (i.e via from the solder ball to the top buried ground plane), a significant benefit of 15 to 20% is obtained over existing PCB designs.

Note: The maximum power dissipation is calculated using a junction temperature of 150°C.

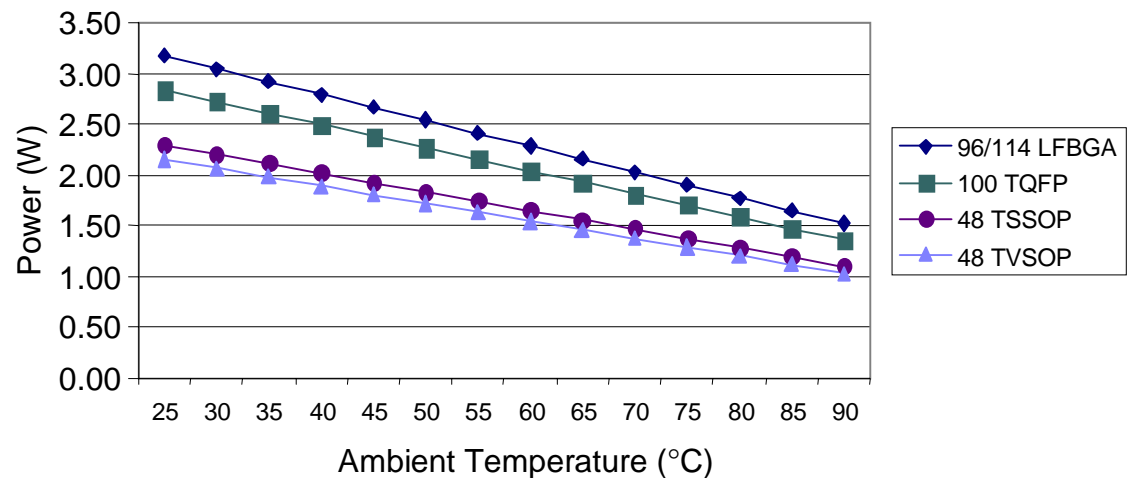
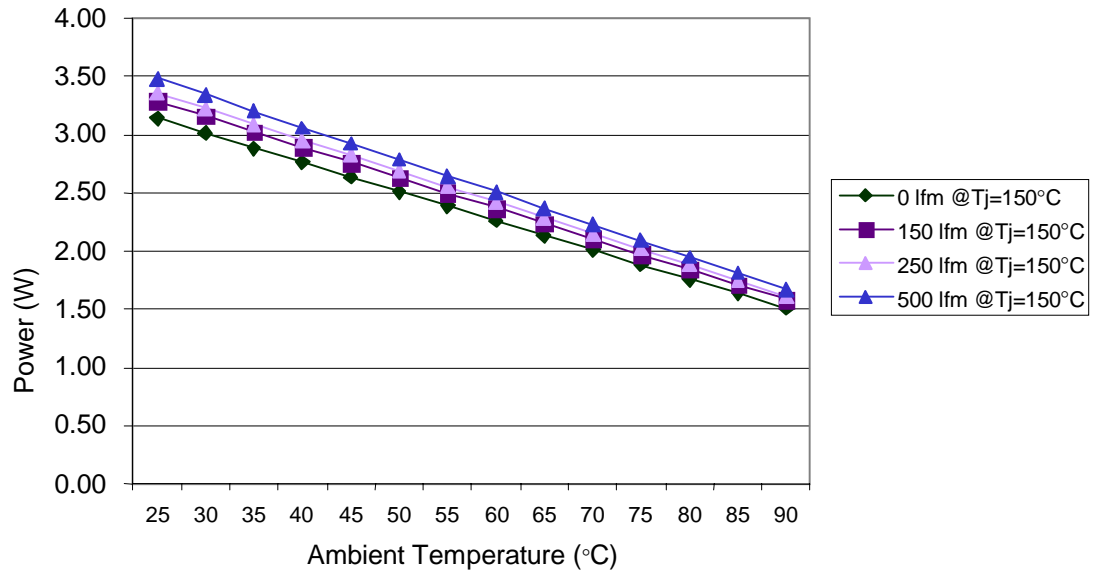


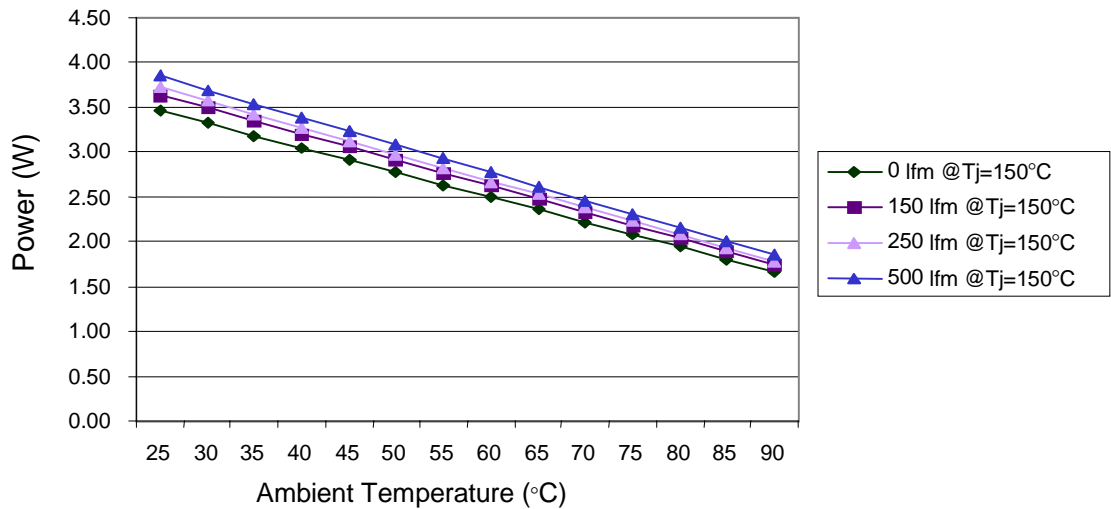
Figure 3.7 - Thermal Comparisons on Multi-Layer JEDEC Board



Note: The maximum power dissipation is calculated using a junction temperature of 150°C.

Air Velocity (ft/min)	0	150	250	500
$\theta_{JA}$ (°C/W)	39.8	38.0	37.2	35.9

**Figure 3.8 – LFBGA Thermal Derating Curves without Thermal Vias Using Multilayer JEDEC Board**



Note: The maximum power dissipation is calculated using a junction temperature of 150°C.

Air Velocity (ft/min)	0	150	250	500
$\theta_{JA}$ (°C/W)	36.1	34.4	33.6	32.5

**Figure 3.9 – LFBGA Thermal Derating Curves with Thermal Vias Using Multilayer JEDEC Board**

### 3.2 LFBGA vs. TVSOP, TSSOP, and Millipaq™ footprint

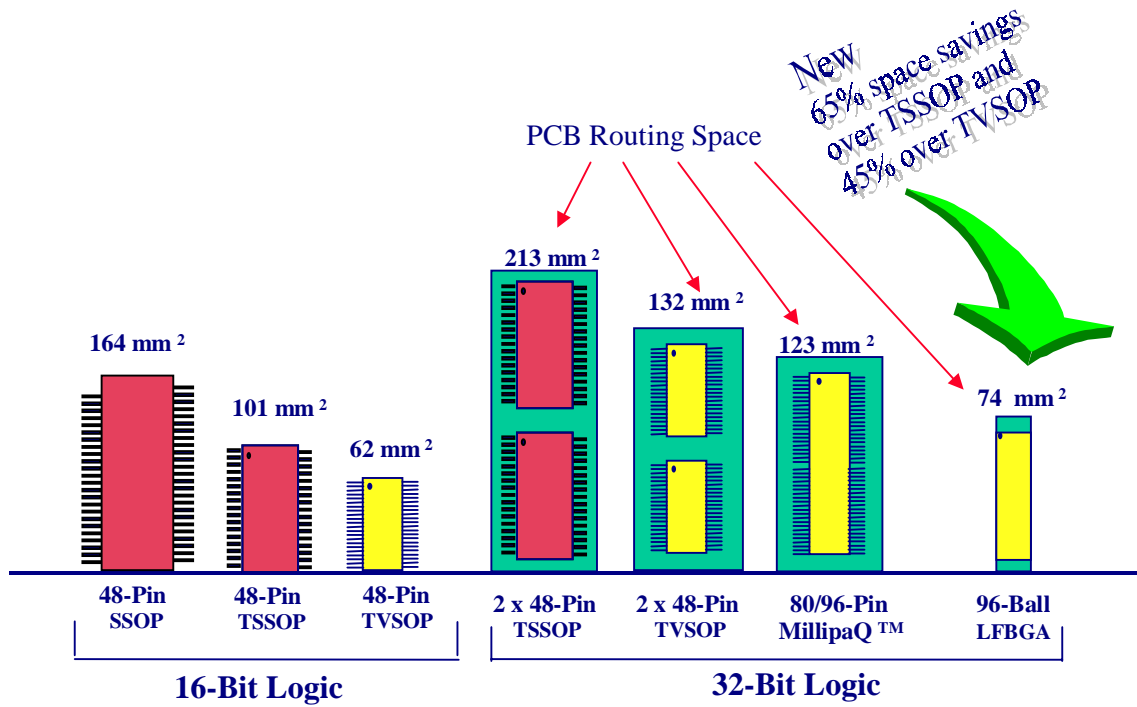


Figure 3.10 – Package Comparisons

Comparison of the normalized thermal dissipation for the TSSOP, TVSOP, and the LFBGA-96 shows that the LFBGA-96 with thermal vias exceeds by a factor of 2 the capability of 2 x 48 TSSOP packages.

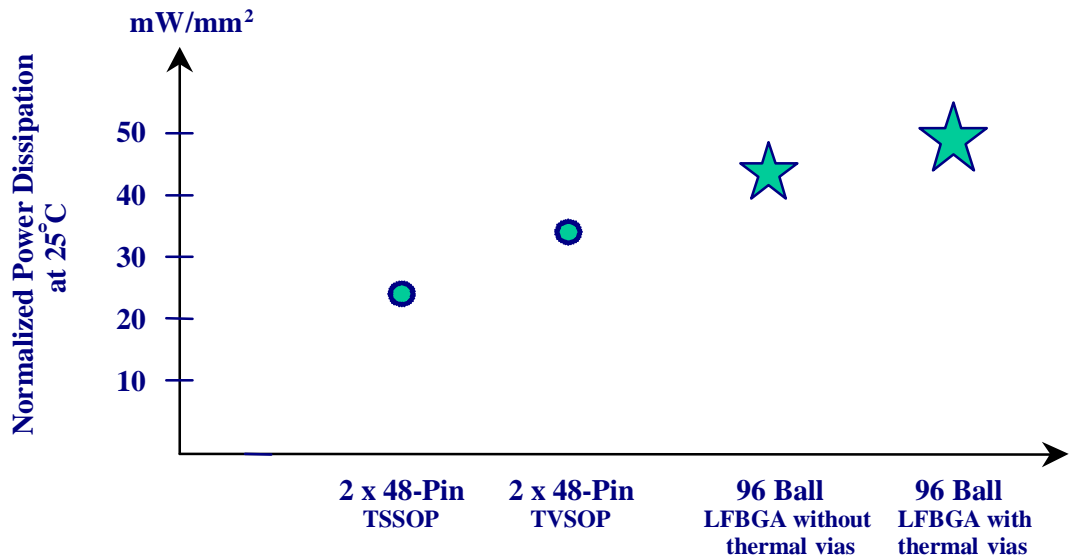


Figure 3.11 – Normalized Power Dissipation at 25°C

Note: Calculations are based on the data from figure 3.7 and figure 3.10.

### 3.3 Benefits to the Customer

The following table summarizes key features and corresponding benefit for logic products assembled in LFBGA packages.

Feature	Benefit
Offer the minimum foot print to industry	Uses the smallest real estate among industry standard packages. Cost savings for PC boards.
Minimize the skew parameter	Provides the user with a reliable solution in new faster bus configurations.
Minimize package propagation delay	Provides the user with additional design margin in high speed buses.
Rise time and fall time is 1ns typical	Again, $t_r$ and $t_f$ are optimized to meet good duty cycle at 100 MHz and 133 MHz while keeping the ground bounce under 500 mV.
Lower ground bounce	Allows more noise margin.
Selected as a JEDEC standard package	Meet mechanical and electrical specifications define by the IDT/Philips/TI working group.
No external components other than bypass capacitors	Can use 2.5V or other special supply from 2.5 to 3.3V.
Supports/enables high speed applications	Low cost, low maintenance, better reliability.
	LFBGA packages has less capacitance pin-to-pin inductance and ground inductance. This provides better support for high-speed applications.

**Table 3.2 – Feature/Benefits of LFBGA Packages**

### 3.4 Contribution to JEDEC Definition

The 96 and 114 ball LFBGA packages have received JEDEC (Joint Electronics Device Engineering Council) JC-11 under semiconductor package standard MO-205 and EIAJ (Electronic Industry Association Japan) registration. IDT, Texas Instruments and Philips Semiconductors have also submitted to JEDEC a proposed 96 and 114 ball LFBGA pin-out to the JC-40 council and final voting by JEDEC participants is expected by the end of 1998.

### 3.5 Evaluation Units

For evaluation units, contact authorized distributors or for more information refer to the following URLs:

Integrated Device Technology URL: <http://www.idt.com>

Philips Semiconductors URL: <http://www.philipslogic.com>

<http://www.semiconductors.philips.com/logic>

Texas Instruments URL: <http://www.ti.com/sc/lfbga>

## 4 LFBGA Package Marking, Shipping Media and Handling

The following section describes the symbolization of these new LFBGA packages.

### 4.1 Marking

Integrated Device Technology, Philips Semiconductors and Texas Instruments use laser marking to identify the vendor, product number, year and month of fabrication, manufacturing site, lot trace code. Each vendor adopted a specific package designator for the LFBGA packages and is reported in table 4.1:

	<b>Integrated Device Technology</b>	<b>Philips Semiconductors</b>	<b>Texas Instruments</b>
LFBGA-96	BF	GKE	GKE
LFBGA-114	BF	GKF	GKF

**Table 4.1 – Vendor Package Designator**

Marking examples for the LVCH32244 device:

IDT Marking:

Part #: LVCH32244A  
Date Code, Marking Location  
Lot number, Assembly Location

Logo	LVCH32244A X9848Y
○	Xmax10xX

Texas Instruments Marking:

Part #: CH244A  
Year, Month, Site  
Lot trace code

Logo	CH244A YMS
○	LLLL

Philips Semiconductors Marking:

Part #: LVCH32244A  
Lot number, Site  
Date Code

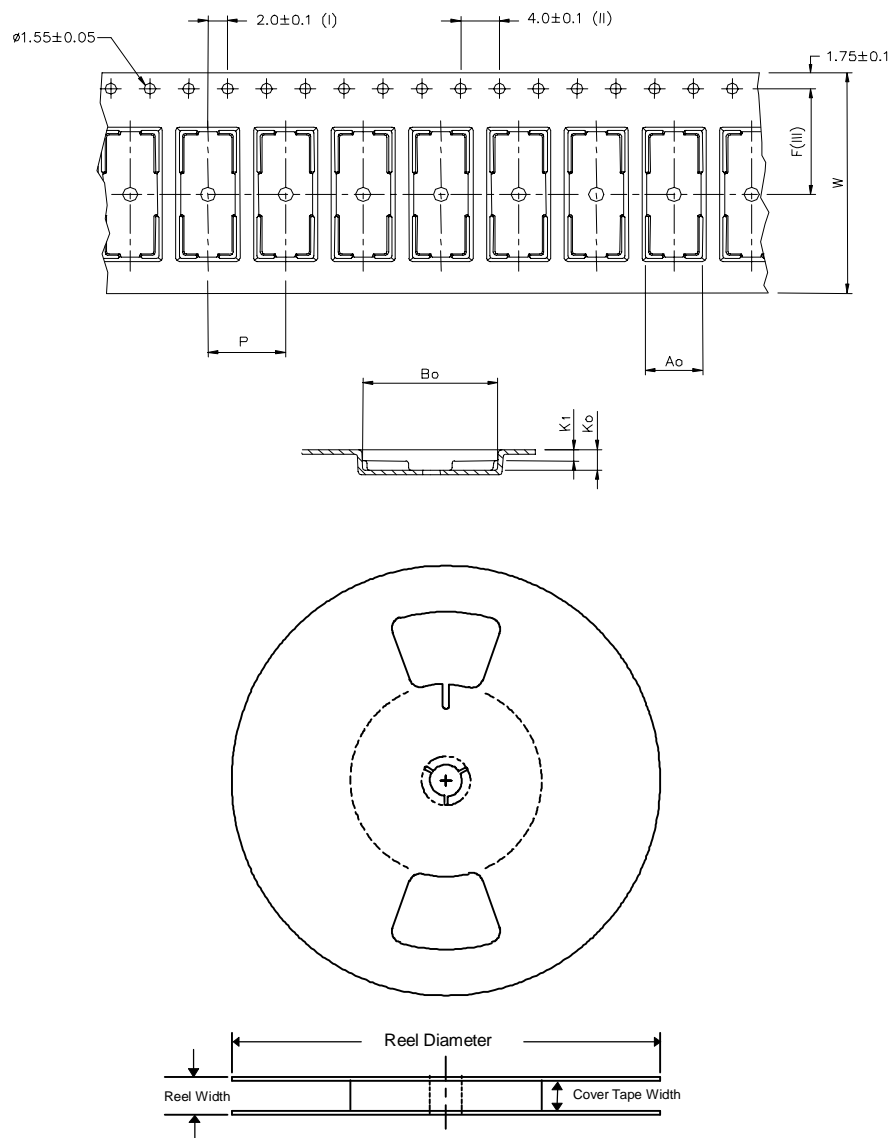
Logo	LVCH32244A Lot Trace
○	YYWW

<b>Device Name</b>	<b>Integrated Device Technology</b>	<b>Philips Semiconductors</b>	<b>Texas Instruments</b>
LVCH32244A	LVCH32244A	LVCH32244A	CH244A
LVCH32245A	LVCH32245A	LVCH32245A	CH245A
LVCH32373A	LVCH32373A	LVCH32373A	CH373A
LVCH32374A	LVCH32374A	LVCH32374A	CH374A
ALVCH32501	ALVCH32501	ALVCH32501	ACH501

**Table 4.2 – Vendor Part Number Marked on Top of Package**

## 4.2 Tape & Reel

The embossed Tape & Reel method is preferred by automatic pick-and-place machines. Integrated Device Technology, Philips Semiconductors and Texas Instruments offer Tape & Reel packaging for the 96 and 114 ball LFBGA packages. The packaging materials used include Carrier Tape, Cover Tape and a Reel. All material used meets industry guidelines for ESD protection and the design is in full compliance with EIA Standard 481-A, "Taping of Surface Mount Components for Automatic Placement." The dimensions that are of interest to the end-user are tape width (W), pocket pitch (P) and quantity per reel. The figure below illustrates the Tape & Reel design for LFBGA package.



**Figure 4.1 – Tape & Reel Mechanical Dimensions**

Package	Cover Tape Width (W)	Pocket Pitch (P)	Reel Width	Reel Diameter	Quantity Per Reel
LFBGA-96	21.0	8.00	24.0	330	1000
LFBGA-114	21.0	8.00	24.0	330	1000

**Table 4.3 – Tape & Reel Assembly Information**

Package	Pocket Width (A <sub>p</sub> )	Pocket Length (B <sub>p</sub> )	Pocket Depth (K <sub>p</sub> )	Pedestal Depth (K <sub>1</sub> )	Hole to Pocket Centerline (F)
LFBGA-96	5.7	13.7	2.0	1.2	11.5
LFBGA-114	5.7	16.2	2.0	1.2	11.5

All dimensions are in millimeters

**Table 4.4 – Tape & Reel Dimension for LFBGA Package**

### 4.3 Sockets, and Socket Manufacturer (Ordering Information)

**Yamaichi Socket numbers:** LFBGA-96 PN# IC280-096-144  
LFBGA-114 PN# IC280-114-145

*Yamaichi Electronics USA, Inc.  
2235 Zanker Road  
San Jose, CA 95131*

*Tel: (408) 456-0797*

**Loranger Socket numbers:** LFBGA-96 PN# 135055096U6617  
LFBGA-114 PN# 169055114U6617

*Loranger International Corp.  
817 Fourth Avenue  
Warren, PA 16365  
California Contact Office*

*Tel: (814) 723-2250  
Tel: (408) 727-4234*

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## 5 PCB Manufacturing Considerations

The following section describes the assembly on PCBs of the LFBGA products.

### 5.1 Land Pads

The design of the land pads for LFBGA packages on the printed circuit board is critical, if the end-user wants to achieve good manufacturability and optimum reliability. An optimum design is when the diameter of the land pad is equal to the diameter of the package vias; (i.e. the fatigue life of the solder balls is enhanced when the ratio of these dimensions is equal to 1.0).

There are two methods of defining land pads on PCB – *solder mask defined* and *non-solder mask defined*. In the *solder mask defined*, the desired land area is defined by the opening of the solder mask. The advantage of this technique is that the land pad size is controlled and the solder mask promotes the adhesion of the copper pad to the PCB. However, the copper pad dimension is larger which makes routing more difficult. In the *non-solder mask defined*, the land area is etched inside the solder mask area. The final land pad dimension is dependent on the accuracy of the copper etching method. The advantage of *non-solder mask defined* over the *solder mask defined* methods is routability (it allows larger trace width/spacing between the solder balls). Figure 5.1 illustrates the land pad dimension for the 96 and 114 ball LFBGA package using the solder mask defined and non-solder mask defined method.

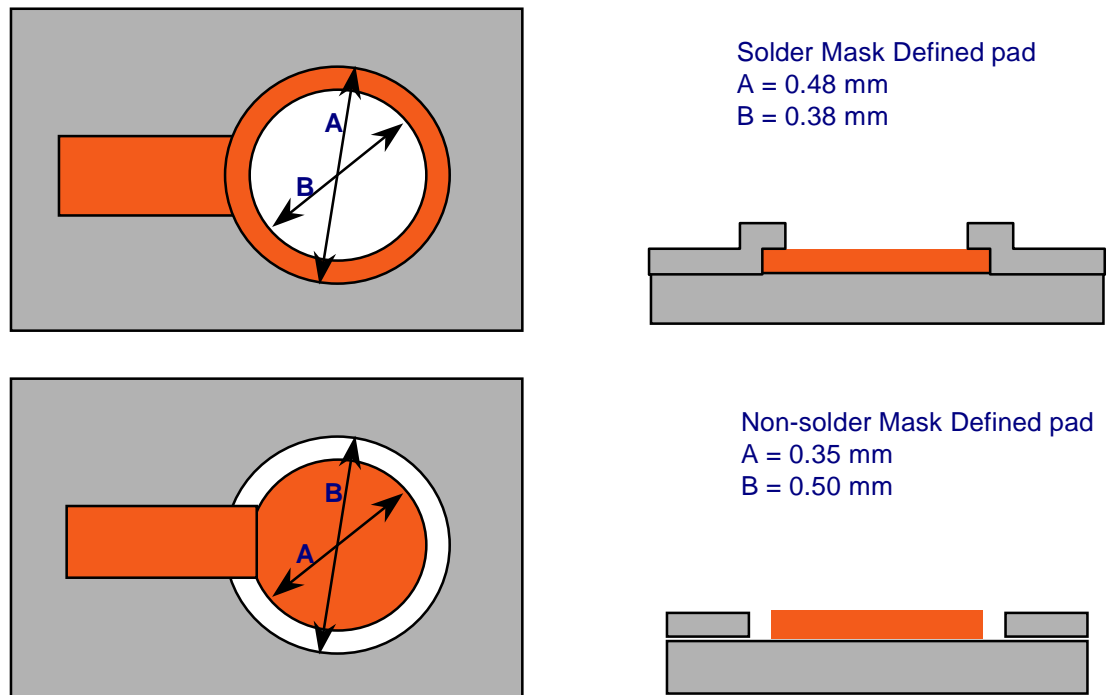


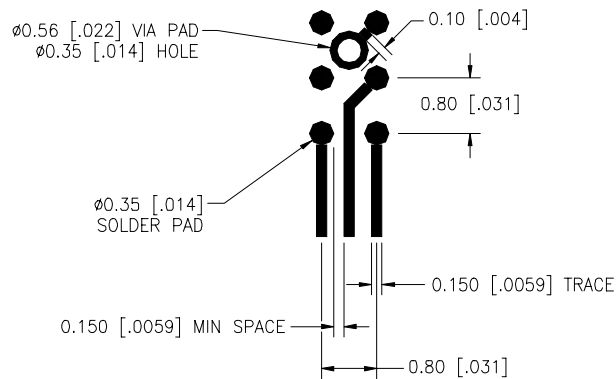
Figure 5.1 – LFBGA Recommended Land Pad Design

### 5.2 Line and Spaces



This section describes the maximum trace width/spacing dimension allowed for 0.8mm ball pitch LFBGA packages with 0.5 mm ball diameter. It becomes a challenge to the designers to route this package on a single layer board unless the PCB supplier has fine pitch trace width/spacing capabilities. PCB capabilities are currently in the 4 to 5 mil (100 – 125  $\mu\text{m}$ ) trace width/spacing range and using a finer pitch trace width/spacing will increase the overall PCB cost to the end-user. The optimum design is to use current PCB capability, which allows one signal to be routed between the land pads. Using the recommended land pad dimension outlined in section 5.1, the PCB supplier needs to have trace width/spacing capabilities of 4.2 mil (107  $\mu\text{m}$ ) and 5.9 mil (150  $\mu\text{m}$ ) respectively for the solder mask and non-solder mask defined pads.

Figure 5.2 represents a visual layout as described in section 5.2 and 5.3.



**Figure 5.2 – LFBGA Trace Width/Spacing Dimensions (mm)**

### 5.3 Vias

Via density can be just as challenging to the designers when routing a high-density board. Via density is defined as the number of vias in a particular board area. Using smaller vias increases the via density and the routability of the board by requiring less board space. Holes can be mechanically drilled down to 6 mil (152  $\mu\text{m}$ ), however, mechanically drilled holes less than 12 mil (305  $\mu\text{m}$ ) begin to add cost to the PCB. To avoid higher PCB costs, other via technology exist (such as laser, punched and plasma-etched) and can be used to form smaller holes. The invention of the micro-via has solved many of the problems associated with via density. Micro-vias are often created using a plasma-etched technique, which penetrates layers of dielectric and allows signal routing to the internal layers. Current micro-via technology allows a 2.4 to 4.0 mil (60 – 100  $\mu\text{m}$ ) via diameter. Micro-vias can also be designed directly into the land pad thereby obsoleting trace fan-outs.

Table 5.1 summarizes the maximum via diameter that can be used for routing the LFBGA package using recommended land pad dimensions outlined in section 5.1.

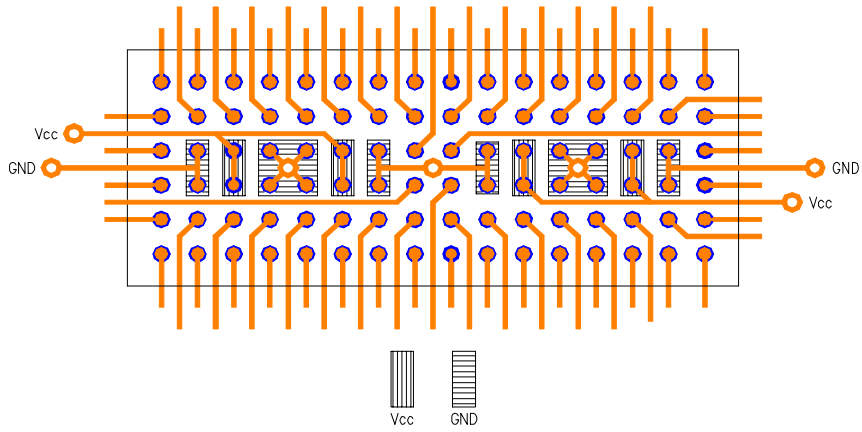
	<b>Solder Mask Defined Land Pad</b>	<b>Non-solder Mask Defined Land Pad</b>
Trace width/spacing	0.107 mm (4.2 mil)	0.150 mm (5.9 mil)
Drill bit diameter	0.23 to 0.25 mm (9 to 10 mil)	0.35 to 0.38 mm (14 to 15 mil)
Unplated hole	0.23 to 0.25 mm (9 to 10 mil)	0.35 to 0.38 mm (14 to 15 mil)
Finished via size (plated)	0.178 to 0.2 mm (7 to 8 mil)	0.30 to 0.33 mm (12 to 13 mil)

Note: Unplated via diameter assumes a 0.2 mm (8 mil) via land dimension and a 0.1 mm (4 mil) clearance between the via land to the adjacent land pad.

**Table 5.1 – Maximum Via Diameter**

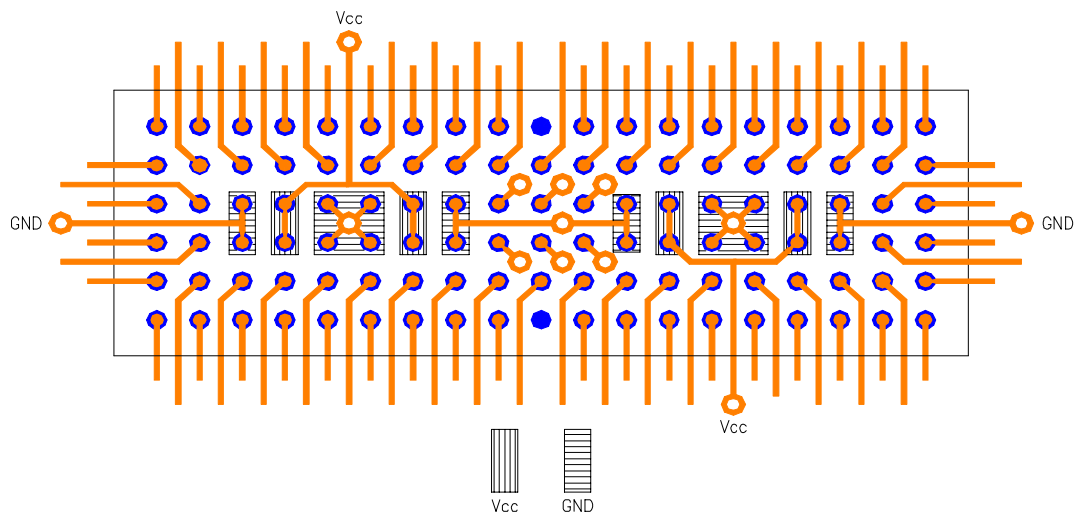
## 5.4 Routing

The figures below are examples of a PCB routing with two layers of PCB interconnect:



Note 1: Ground balls are connected together within the PCB.

**Figure 5.3 – LFBGA-96 Recommended Routing**



Note 1: Ground balls are connected together within the PCB.

**Figure 5.4 – LFBGA-114 Recommended Routing**

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## 6 Conclusion

This joint study by Integrated Device Technology, Philips Semiconductors and Texas Instruments shows the 96 and 114 LBGA packages as the most effective solution for addressing performance issues:

(1) minimal skew due to package layout design; (2) improved thermal power dissipation by taking advantage of the chip overlap over the solder balls; and (3) reduced inductance as functions in these packages take advantage of less capacitance for pin-to-pin inductance, thereby enabling support for high speed applications with close to 2X the bandwidth.

In terms of board integration and miniaturization, these LFBGA packages will reduce board space by up to 65% compared to the corresponding TSSOP package for the same functionality.

Additionally, designers may take advantage of improved reliability and reduced manufacturability costs when the diameter of the PCB land pad is equal to the diameter of package vias as explained in section 5.

With the introduction of the LFBGA by Integrated Device Technology, Philips Semiconductors and Texas Instruments, OEMs are assured of an agreed upon JEDEC standardized package, pin out and availability of the product families and functions to be initially introduced. Integrated Device Technology, Philips Semiconductors and Texas Instruments will continue to work with the market identifying new requirements in terms of product family, and functions.

### Acknowledgements:

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