Application Report
SCEA045–September 2011

Voltage Clamps Made Easy

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ABSTRACT

This document presents designers with several methods of voltage clamping cascaded FET's with common gates.

Today's complex electronic systems involve a multitude of power planes. In order for these mixed-mode systems to operate properly, some type of voltage translation or clamping is necessary. This allows the different input/outputs (I/O) to communicate with each other without damage from overvoltage,

A simple and inexpensive way to accomplish this is with an FET voltage clamp circuit. For this example, the Texas Instruments SN74TVC3306 dual voltage clamp is used. By connecting one I/O of the FET to Vcc, the designer is able to use one of the I/Os on the opposite side as a voltage reference (Vref). This allows the designer to regulate the outgoing voltage by adjusting Vref. Vref is not able to adjust above Vdd – 0.8 V.

The advantages of using a voltage clamp are:

1. High-speed translation
2. Direction control unnecessary
3. Excellent ESD performance
4. Low Ron
5. With a 5-V supply, the designer can regulate the voltage between 1 V and 5 V on the inputs or the outputs.

Voltage clamps can be used for:

1. Simple unidirectional voltage translation
2. Bidirectional I^2C™ translation
3. GTL to TTL/LVTTL translation
4. Translation from one voltage to several different voltages using a single part

The following examples illustrate different ways to use the voltage clamp.

In Figure 1, the output voltage can be adjusted between 0.8 V and 4.2 V.

I^2C is a trademark of Philips Electronics N.V.

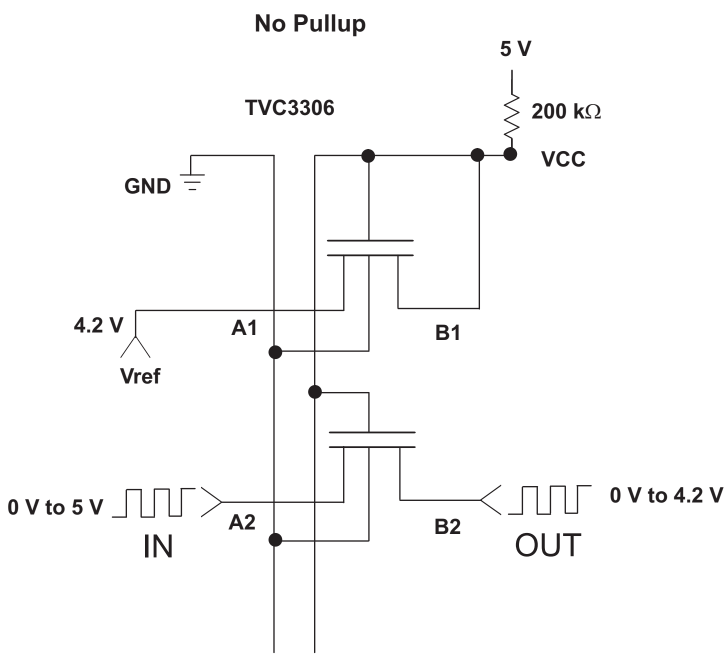

Figure 1. Example 1

Figure 2 shows the same setup but uses a pullup resistor. This allows the output to swing up to the pullup voltage. Several output voltage levels are possible by pulling up to different nodes, but Vref must be set to the lowest output voltage. The designer is able to pull up to any voltage between Vref and Vcc.

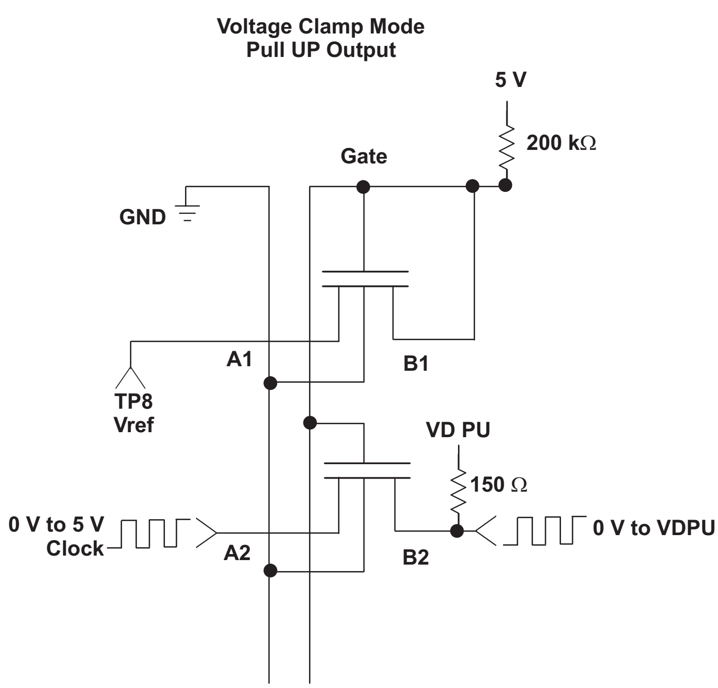

Figure 2. Example 2

Figure 3 uses a pulldown resistor. By using the pulldown resistor, the output is clamped to Vref.

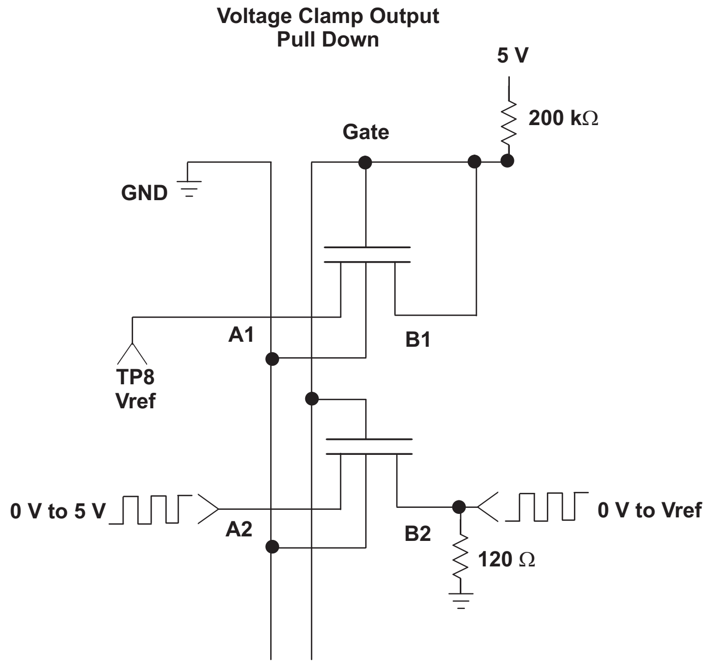

Figure 3. Example 3

In Figure 4, both sides are clamped by using an open-drain device on the input of the TVC. In example 4, the open drain is low when the input signal is high, and the TVC pulls the signal high when the input is low. This produces a 0 V to Vref inverted signal on the input and a 0-V to the pullup voltage on the output side. This type of circuit is often used on open-drain-type CPU interfaces found in personal computers. This can help eliminate glitches or spikes from the driving side. In example 4, a SN74LVC1G07 is used for the open-drain device. A simple transistor can be used instead. Additional information about this type of setup can be found in the application information in the SN74TVC3306 data sheet (SCDS112).

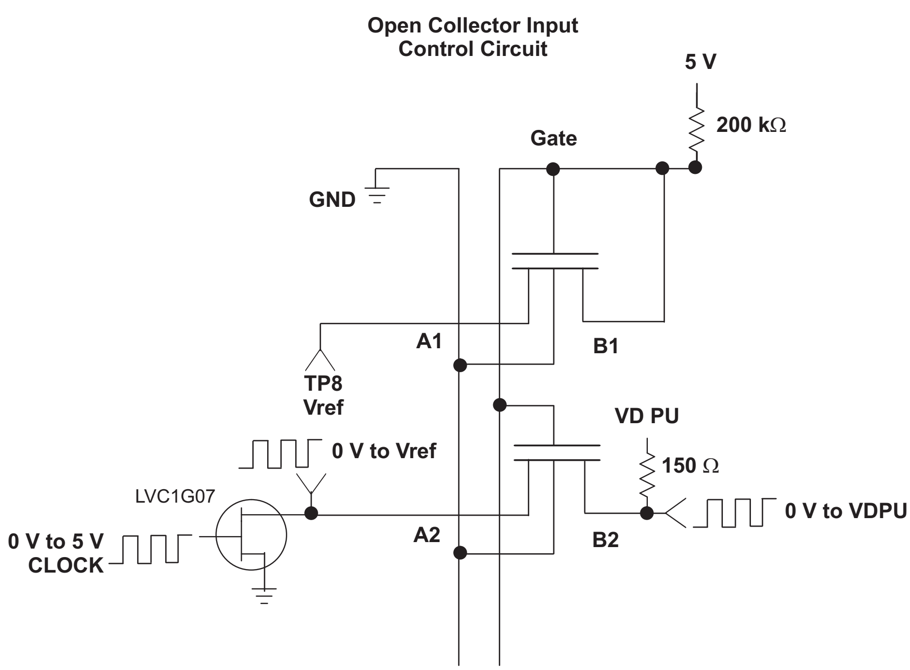

Figure 4. Example 4

The Texas Instruments portfolio contains many other types of voltage level translators. See the application report *Selecting the Right Level-Translation Solution* (SCEA035) for more information about voltage clamps and many other types of translators.

Sizing Pullup Resistor

The pullup resistor value needs to limit the current through the pass transistor, when it is in the on state, to about 15 mA. This ensures a pass voltage of 260 mV to 350 mV. If the current through the pass transistor is higher than 15 mA, the pass voltage also is higher in the on state. To set the current through each pass transistor at 15 mA, the pullup resistor value is calculated as:

$$R_{PU} = \frac{V_{DPU} - 0.35\ V}{0.015\ A}$$

The following table summarizes resistor values, reference voltages, and currents at 15 mA, 10 mA, and 3 mA. The resistor value shown in the +10% column (or a larger value) should be used to ensure that the pass voltage of the transistor is 350 mV or less. The external driver must be able to sink the total current from the resistors on both sides of the device at 0.175 V, although the 15 mA applies only to current flowing through the device.

PULLUP RESISTOR VALUES (1) (2)

V_{DPU}	PULLUP RESISTOR VALUE (Ω)					
	15 mA		10 mA		3 mA	
	NOMINAL	+10% (3)	NOMINAL	+10% (3)	NOMINAL	+10% (3)
5 V	310	341	465	512	1550	1705
3.3 V	197	217	295	325	983	1082
2.5 V	143	158	215	237	717	788
1.8 V	97	106	145	160	483	532
1.5 V	77	85	115	127	383	422
1.2 V	57	63	85	94	283	312

(1) Calculated for V_{OL} = 0.35 V
(2) Assumes output driver V_{OL} = 0.175 V at stated current
(3) +10% to compensate for V_{DD} range and resistor tolerance

Bandwidth

The maximum frequency is dependent on the application. The device can operate at speeds of > 100MHz given the correct conditions. The maximum frequency is dependent upon the loading of the application. The clamp behaves like a standard switch where the bandwidth of the device is dictated by the on resistance and on capacitance of the device.

Figure 5 shows a bandwidth measurement of the clamp using a two-port network analyzer.

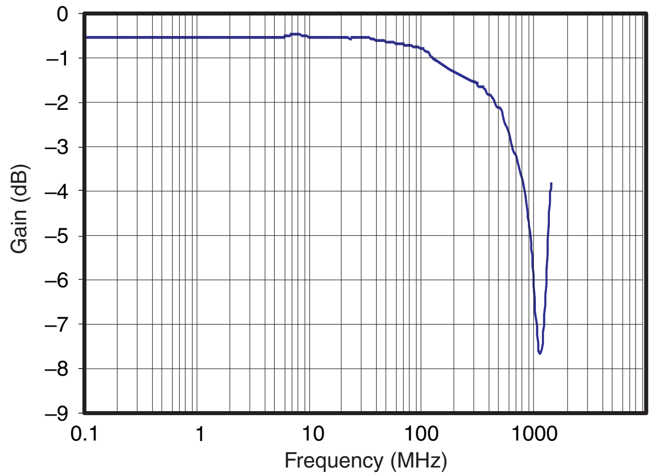

Figure 5. Bandwidth

The 3-dB point of the clamp is ≈600 MHz. However, this measurement is an analog type of measurement. For digital applications the signal should not degrade up to the fifth harmonic of the digital signal. As a rule of thumb, the frequency bandwidth should be at least five times the maximum digital clock rate. This component of the signal is very important in determining the overall shape of the digital signal. In most cases, digital clock frequency of >100 MHz can be achieved.

The clamp does not provide any drive capability. Therefore higher frequency applications will require higher drive strength from the host side. No pullup resistor is needed on the host side (3.3 V) if the clamp is being driven by standard CMOS totem pole output driver. Ideally, it is best to minimize the trace length from the clamp on the sink side (1.8 V) to minimize signal degradation.

You can then use a simple formula to compute the maximum "practical" frequency component. Or the "knee" frequency (f_{knee}). All fast edges have an infinite spectrum of frequency components. However, there is an inflection (or "knee") in the frequency spectrum of fast edges where frequency components higher than f_{knee} are insignificant in determining the shape of the signal.

To calculate f_{knee}:

f_{knee}= 0.5/RT (10–80%)

f_{knee} = 0.4/RT (20–80%)

For signals with rise time characteristics based on 10- to 90-percent thresholds, f_{knee} is equal to 0.5 divided by the rise time of the signal. For signals with rise time characteristics based on 20- to 80-percent thresholds, which is very common in many of today's device specifications, f_{knee} is equal to 0.4 divided by the rise time of the signal.

Some guidelines to follow that will help maximize the performance of the device:

- Keep trace length to a minimum
- The trace length should be less than half the time of flight to reduce ringing and line reflections or non monotonic behavior in the switching region
- To reduce overshoots, a pullup resistor can be added on the 1.8 V side; be aware that a slower fall time is to be expected