Application Report
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Steps to Configure TIC12400-Q1 Multiple Switch Detection Interface (MSDI)

Helen Wanchie Sun

ABSTRACT

This application report explains the procedures to configure the TIC12400-Q1 using two examples including a set of digital and analog switches.

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1 Automotive Body Control Module

The body control module (BCM) is an electronic control unit responsible for monitoring and controlling electronic accessories in a vehicle body. Detecting mechanical switch status in a vehicle is an important task handled by the BCM. The automotive body has on-and-off type of switch (digital switch) such as door locks and resistor coded switch (analog switch) with three or more states used in wiper speed control. A typical switch detection implementation with a MSDI device is shown in Figure 1.

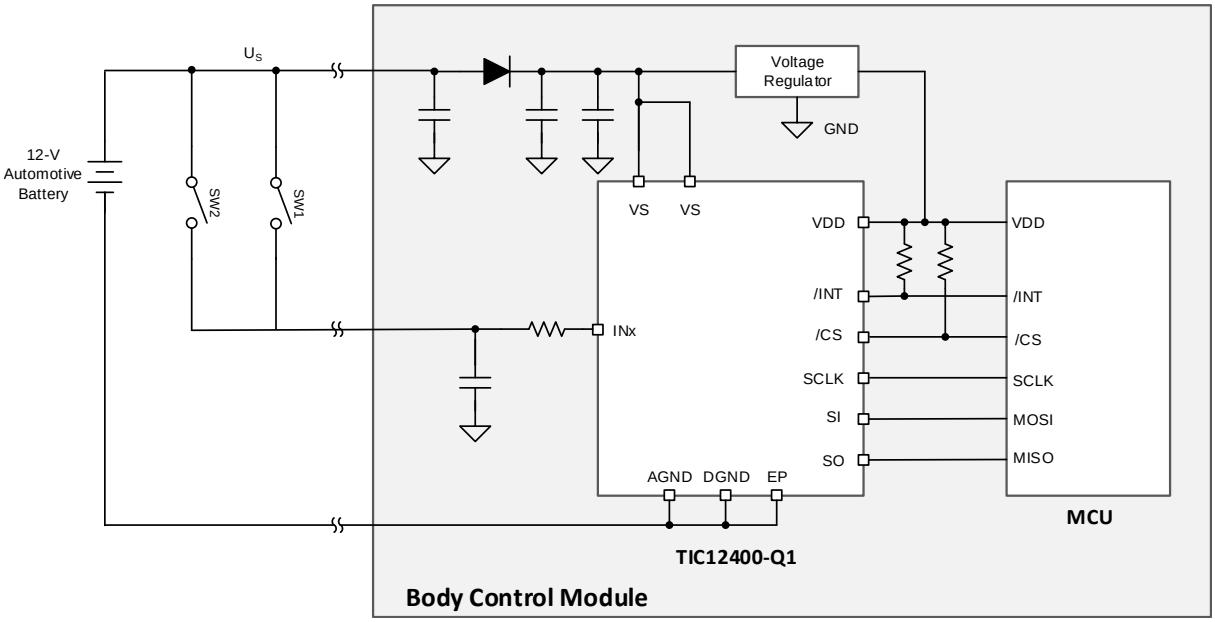


Figure 1. Typical switch detection

2 TIC12400-Q1 device 101

The TIC12400-Q1 is an integrated multiple switch detection interface (MSDI) designed to detect external switch status in a 12-V automotive system. The TIC12400-Q1 features an integrated 10-bit ADC that saturates at 6V to monitor analog switches and a comparator with four thresholds(2-V, 2.7-V, 3-V, 4-V) to monitor digital switches. The ADC and the comparator threshold can be programmed to support a wide variety of switch types. The TIC12400-Q1 has 24 direct switch inputs, 10 inputs (IN0-IN9) are configurable to monitor switches connected to either ground or battery and 14 inputs (IN10-IN23) are for general use. Each input can be easily programmed through SPI interface to support different application scenarios. The TIC12400-Q1 input can also be programmed to monitor more than 24 switches. The ability to monitor more than 24 switches with the same number of inputs reduces the overall system cost. (See: *Input Sharing with the TIC12400-Q1*) A simplified block diagram of TIC12400-Q1 is shown in Figure 2.

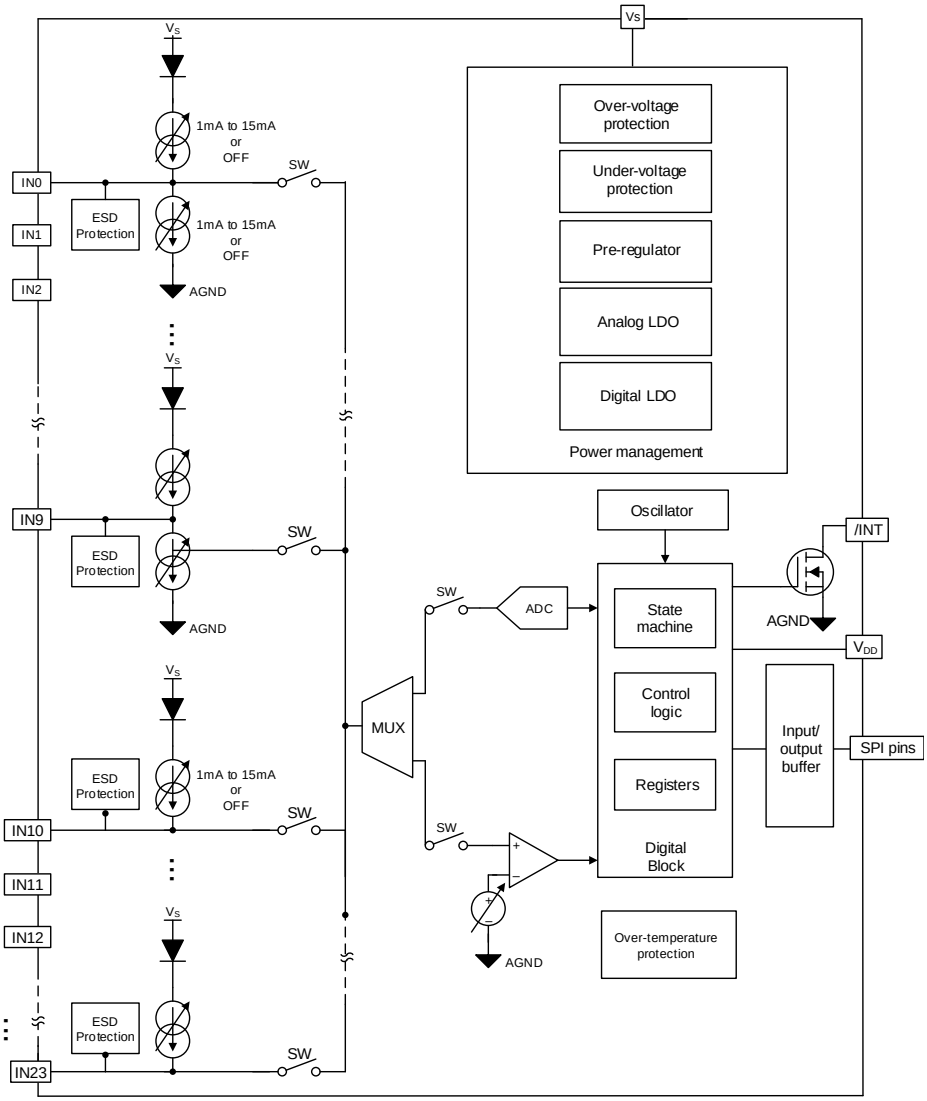


Figure 2. Simplified block diagram

3 How to configure TIC12400-Q1

There are only a handful of registers to configure to start monitoring switch status. Follow the steps in Figure 3 to configure the TIC12400-Q1 registers:

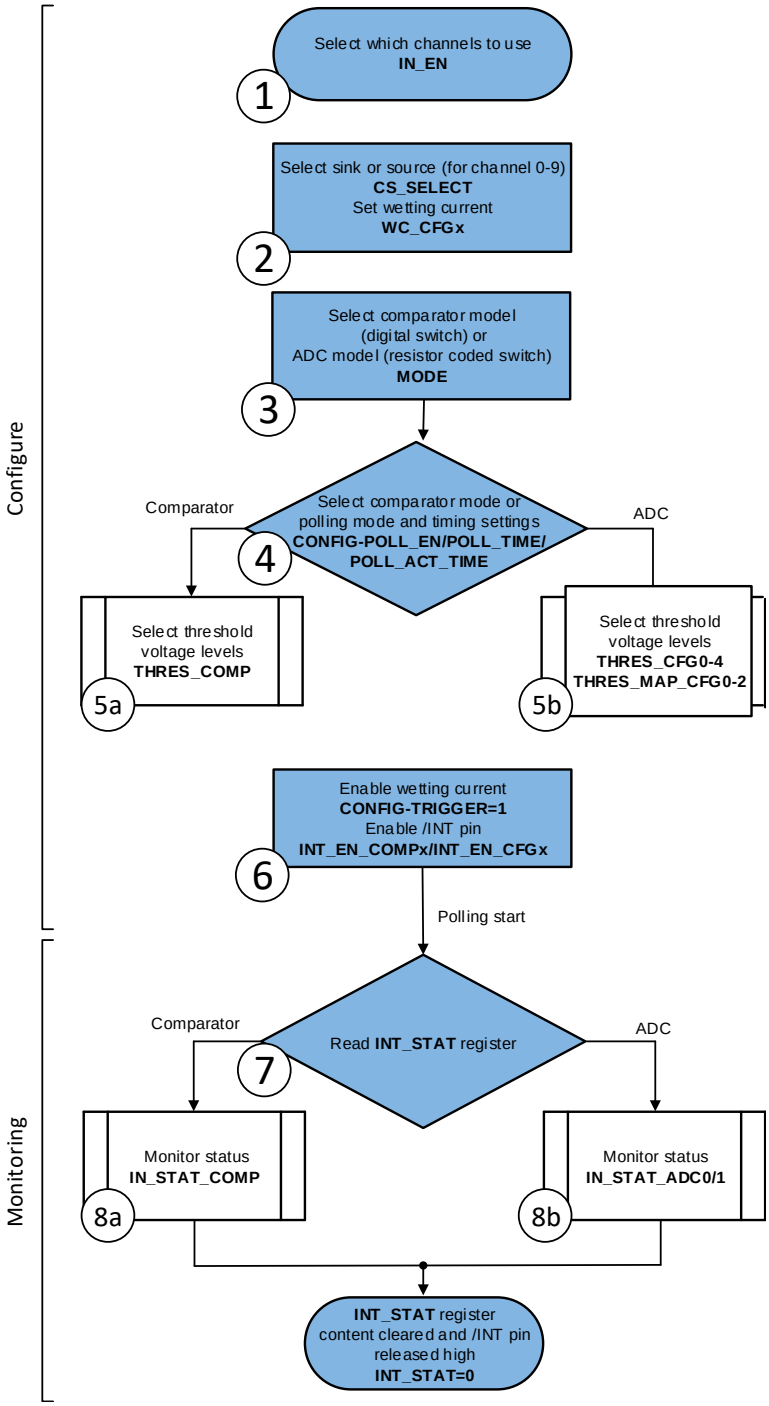


Figure 3. Flow chart

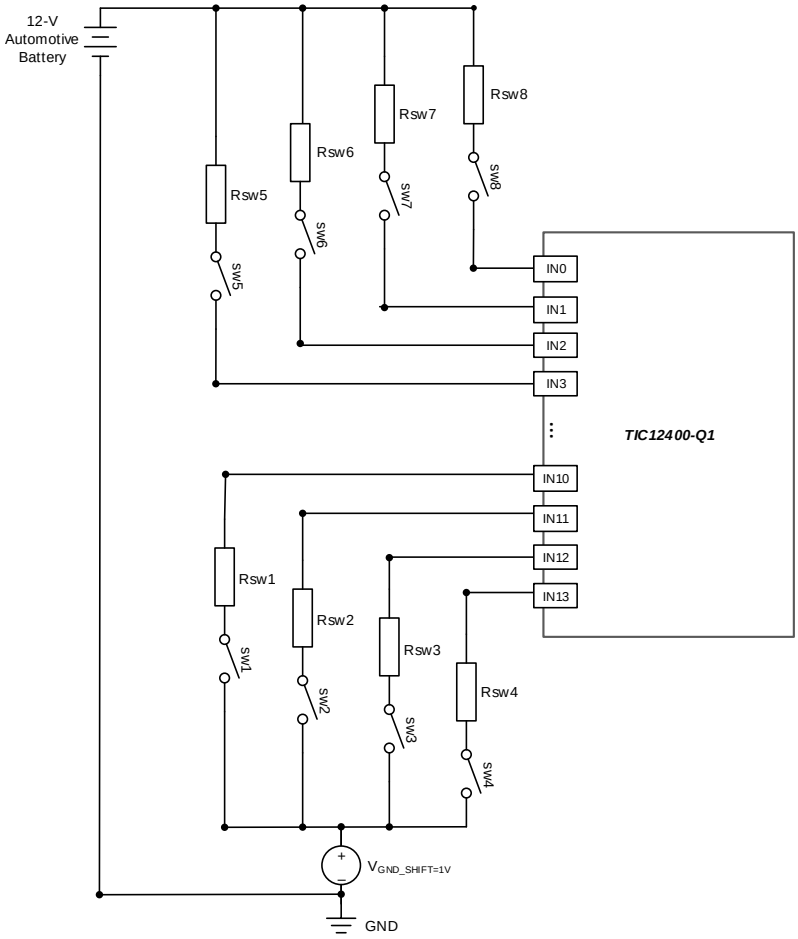
After polling and wetting current have been activated, the monitored digital switch status is stored in IN_STAT_COMP register for comparator inputs and the monitored analog switch status is stored in IN_STAT_ADC0/1 for ADC inputs. Once wetting current has been enabled, the TRIGGER bit (CONFIG register) must be set to “0” to apply changes to the register settings.

4 Interrupt configuration

The $\overline{INT}$ pin is used to monitor events detected by the TIC12400-Q1. Example of monitored events include: switch state change, temperature warning, over-voltage shutdown, and so on. These events are communicated to the micro-controller by the $\overline{INT}$ pin output asserting logic low. To configure $\overline{INT}$ pin, select static or dynamic assertion scheme (selected in INT_CONFIG bit in the CONFIG register). Each switch input (IN0-IN23) can be programmed to have the event interrupt enabled or disabled by configuring registers INT_EN_COMP1 to INT_EN_COMP2 (for comparator assigned inputs) and INT_EN_CFG1 to INT_EN_CFG4 (for ADC assigned inputs). After the end of the first polling cycle, the $\overline{INT}$ pin asserts logic low to notify the micro-controller that the default switch status is ready to be read. It is essential to read and clear the $\overline{INT}$ pin after the first polling cycle is completed and read the corresponding the switch position in the INT_STAT_COMP and INT_STAT_ADC registers. $\overline{INT}$ pin can also be used to wake up a micro-controller in sleep mode which provides significant system-level power savings.

5 Digital switch-using comparator to detect switch states

Digital switch is defined to have two states, typically switch closed resistance less than 100-Ω, and switch open resistance larger than 5000-Ω. Figure 4 is an example of how to configure MSDI to monitor digital switch with 50-Ω resistance in closed state and 5000-Ω resistance in open state:



Notes

- Digital switches: four battery-connected, four ground-connected
- State 1: switch is opened > 5000-Ω
- State 2: switch is closed: 50-Ω
- Minimum Vs = 6-V (lowest battery voltage during cranking), grounded shift = 1-V

Figure 4. Digital switch

5.1 Configure channels

Enable channel used by setting IN_EN_x bit to 1 in the IN_EN register (*Flow chart step 1*) . For battery-connected switches, only inputs IN0-IN9 of TIC12400-Q1 may be enabled. In this example, inputs IN0-IN3 are configured for battery-connected switches, and inputs IN4-IN7 are configured for ground-connected switches.

Select source/sink mode and program the wetting current:

- For ground-connected switches, program the wetting current to source mode by setting CS_INx bits to 0 in the CS_SELECT register. For battery-connected switches, program the wetting current to sink mode by setting CS_INx bits to 1. The wetting current magnitude can be programmed from 0 to 15-mA by configuring WC_CFG0 and WC_CFG1 registers (*Step 2*). Since we are using the comparator in this case, assign 0 to bit 0-3 (IN0-IN3) of MODE register (*Step 3*).
- In CONFIG register, program the POLL_EN bit to enable continuous mode or polling mode, then select total period time in POLL_TIME bits and the active polling time is programmed in the POLL_ACT_TIME bits (*Step 4*).

5.2 Program threshold voltage of comparator

Four thresholds can be selected for the comparator: 2-V, 2.7-V, 3-V and 4-V. There are several factors involved to determine which threshold of the comparator should be picked:

- Using Equation 1 calculate the voltage drop when the switch is closed. The switch closed resistance is 50-Ω, assuming the worst case for digital switches of 100-Ω. With I_{WETT} set at 10-mA, V_{INX} is calculated to be 1-V.

$$V_{INX} = R_{EQ} \times I_{WETT} \quad (1)$$

- Ground shift and other non- ideal situation should be considered. With 1-V ground shift adding onto the previously calculated V_{INX}, the total voltage change is 1.5-V when switch is closed.
- Minimum V_S requested for correct detection is specified in Table 1. In this example, the minimum V_S = 6-V, so 3-V is the highest threshold that can be selected.

Table 1. V_S required for proper detection

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{S_COMP}	Minimum V_S requirement for proper detection	THRES_COMP = 2 V	4.5			V
		THRES_COMP = 2.7 V	5			
		THRES_COMP = 3 V	5.5			
		THRES_COMP = 4 V	6.5			

- If ground-connected switch is used, the threshold voltage should be as high as possible so switch status would not be misread. For our ground-connected switches example (IN0-IN3), considering detection range of the threshold (Table 2), the highest threshold we pick is 3-V due to minimum Vs.
- If battery-connected switch is used, the threshold voltage should be as low as possible so switch status would not be misread. For our battery-connected switches example (IN12-IN15), considering detection range of the threshold (Table 2), the lowest threshold we can pick is 2.7-V due to maximum switch closed voltage of 2-V.

Table 2. Comparator threshold

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{TH\_COMP\_2V}$	Comparator threshold for 2 V	THRES_COMP = 2 V	1.85		2.25	V
$V_{TH\_COMP\_2p7V}$	Comparator threshold for 2.7 V	THRES_COMP = 2.7 V	2.4		2.9	V
$V_{TH\_COMP\_3V}$	Comparator threshold for 3 V	THRES_COMP = 3 V	2.85		3.3	V
$V_{TH\_COMP\_4V}$	Comparator threshold for 4 V	THRES_COMP = 4 V	3.7		4.35	V

- To program the comparator threshold, set the THRES_COMP_IN0_IN3 to 10 (threshold = 3-V) and THRES_COMP_IN4_IN7 (IN4-IN7) bits to 00 (threshold = 2-V) in the THRES_COMP register (*Step 5a*).

5.3 Interrupt enable and start monitoring

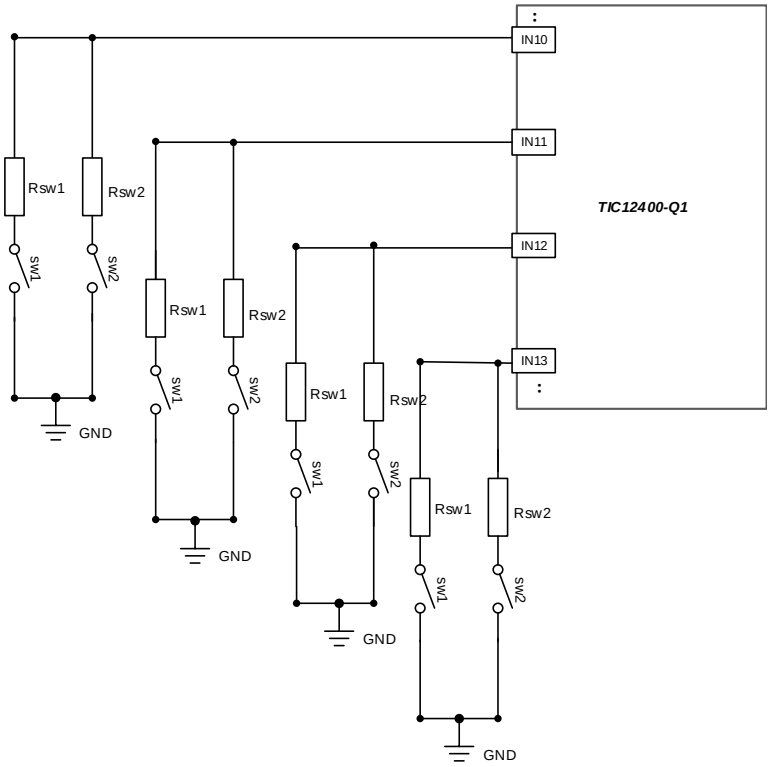
After the voltage thresholds had been set, the interrupt needs to be set properly for TIC12400-Q1 to start the switch monitoring process.

- The Switch Status Change (SSC) interrupt need to be enabled so when switch state had changed, interrupt will be generated and alert the micro-controller. SSC interrupt can be enabled by setting the SSC bit to 1 in the INT_EN_CFG0 register. Start TIC12400-Q1 operation by setting the TRIGGER bit in CONFIG register to 1 and read the INT_STAT register to clear the baseline SSC interrupt (*Step 6*).
- Start monitoring by reading the interrupt status register INT_STAT when /INT pin is asserted and then read the IN_STAT_COMP for comparator status (*Step 8a*).

6 Analog (Resistor-coded) switch-using ADC to detect switch states

Using analog switches combining with an ADC decoding scheme in TIC12400-Q1, implementations such as wiper speed setting and sign control arms in a vehicle can be monitored. With a given set of resistor coded switches, the ADC in TIC12400-Q1 (saturates at 6-V) is able to detect statuses of the switches. The Figure 5 shows a typical connection between a BCM and a resistor coded switch with three states. A real life example of a three state switch is the power window switch in a vehicle where you can pull up, pull down or leave the window stationary.

The example of how to set the ADC for a given set of resistor coded switches with three states is shown in Figure 5:



Notes

- Analog switches: four ground-connected
- Rsw1 = 100-Ω ± 10%
- Rsw2 = 470-Ω ± 10%
- State 1: No switch is closed
- State 2: SW1 is closed
- State 3: SW2 is closed
- Minimum V_S = 6-V (lowest battery voltage during cranking)

Figure 5. Analog switch

In Figure 5, R_{SW1} and R_{SW2} are given and there are three different states that need to be detected by TIC12400-Q1. The following steps can be implemented to determine the threshold of the ADC values.

6.1 Configure channels

Enable channel used by setting IN_EN_x bit to 1 in the IN_EN register. In this example since IN0-IN7 is already used for digital switches and two thresholds are needed (Table 3), IN12-IN15 is enabled for analog switches (*Step 1*).

Table 3. TIC12400-Q1 IN12-15 pin Wetting Current and Threshold Setting Details

INPUT	THRESHOLD		WETTING CURRENT	CURRENT SOURCE/SINK	SWITCH POSITION DETECTION
	COMPARATOR INPUT MODE	ADC INPUT MODE			
IN12	THRES_COMP_IN12_IN15	THRES2A THRES2B	WC_IN12_13	CSO	Switch to GND
IN13		THRES2A THRES2B			
IN14		THRES2A THRES2B	WC_IN14_15	CSO	Switch to GND
IN15		THRES2A THRES2B			

Program the wetting current and select source/sink mode:

- For ground-connected switches, program the wetting current to source by setting CS_INx bits to 0 in the CS_SELECT register. The wetting current magnitude can be programmed from 0 to 15-mA by configuring WC_CFG0 and WC_CFG1 registers (*Step 2*). Since we are using the ADC in this case, assign 1 to bits 12-15 (IN12- IN15) of MODE register (*Step 3*).
- In CONFIG register, program the POLL_EN bit to enable continuous mode or polling mode, then select total period time in POLL_TIME bits and the active polling time is programmed in the POLL_ACT_TIME bits (*Step 4*).

6.2 Calculate the minimum and maximum resistance values in each state

In each state, the maximum resistance is calculated based on the resistance variation.

Table 4. Equivalent switch resistance

	Switch status	Equivalent min/ max resistance
State 1	No switch closed	∞
State 2	SW2 closed, SW1 open	423~517Ω
State 3	SW1 closed, SW2 open	90~110Ω

6.3 Calculate the voltage depending on which wetting current setting is selected

Using Equation 2 calculate the input voltage. Wetting current can be programmed from 0 to 15-mA. In this example wetting current is set to 2-mA by configuring WC_CFG0 and WC_CFG1 registers. The wetting current accuracy needs to be considered as well. For accurate wetting current to be applied, the V_S and V_{INX} conditions need to fulfill the following conditions:

$$V_{INX} = R_{EQ} \times I_{WETT} \quad (2)$$

Table 5. Wetting current accuracy for analog switches

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
WETTING CURRENT ACCURACY (ANALOG SWITCHES)							
I_{WETT}	Wetting current accuracy	1 mA setting	4.5 V ≤ V_S ≤ 35 V, V_S – V_{INX} ≥ 2.5 V	0.88	1	1.13	mA
		2 mA setting		1.8	2	2.25	
		5 mA setting	5.5 V ≤ V_S ≤ 35 V, V_S – V_{INX} ≥ 2.5 V	4.3	5	5.5	
			5.5 V ≤ V_S ≤ 35 V, V_S – V_{INX} ≥ 3 V	4.5	5	5.5	
		10 mA setting	6 V ≤ V_S ≤ 35 V, V_S – V_{INX} ≥ 4 V	9	10	11	
		15 mA setting	6.5 V ≤ V_S ≤ 35 V, V_S – V_{INX} ≥ 5 V	12.5	15	16.5	

In this example minimum V_S = 6-V. If 2-mA wetting current is selected, the highest voltage seen at V_{INX} is at the highest resistance value (517-Ω) multiply by the highest wetting current of 2-mA (2.25-mA) where maximum V_{INX} = 1.16-V, which fulfills the V_S – V_{INX} ≥ 2.5-V requirement for 2-mA wetting current setting. Table 6 values are calculated:

Table 6. Equivalent Voltage at INx

	Switch status	VINx
State 1	No switch closed	6V(max)
State 2	SW2 closed, SW1 open	0.76~1.16V
State 3	SW1 closed, SW2 open	0.16~0.25V

6.4 Convert the voltage established on the INx pin into equivalent ADC code

The integrated 10-bit ADC range of TIC12400-Q1 is from 0-V to 6-V, with 6-V corresponding to the full scale maximum code of 1023. Therefore, the ADC code for each of the three different states can be calculated with equation .

$$ADC_{code} = V_{INX} \times 1024 \div 6 \quad (3)$$

The calculated ADC codes are listed in Table 7:

Table 7. Equivalent ADC code

	Switch status	Code
State 1	No switch closed	1023
State 2	SW2 closed, SW1 open	130~198
State 3	SW1 closed, SW2 open	27~43

After the ADC code spread for each switch state is calculated, the detection can be set at the mid-point between the max code of one state and min code for the next state. For example, to select the threshold between state 2 and state 3, take the mid-point between the highest code of state 2 and lowest code of state 3 (code 87) to be the threshold code between state 2 and 3. For state 1 and state 2, the mid-point between state 1 and lowest code of state 2 (code 611) is selected to be the threshold code between state 1 and 2.

6.5 Set the threshold of the ADC and start monitoring

An additional register mapping step need to be done with ADC switch monitoring containing more than 2 states. Proper threshold configuration rules specified in Table 8 have to be followed for ADC inputs threshold adjustments (*Step 5b*).

Table 8. Proper Threshold Configuration For ADC Inputs

INPUT	PROPER THRESHOLD CONFIGURATION
IN12 to IN17	THRES2B ≥ THRES2A
IN18 to IN22	THRES3C ≥ THRES3B ≥ THRES3A
IN23	THRES9 ≥ THRES8 ≥ THRES3C ≥ THRES3B ≥ THRES3A

Two thresholds are set with THRES2B = code 611 and THRES2A = code 87. These 2 values can be set in THRES_CFG0 register . THRES_CFG0 is selected in this case with THRES1= 611 and THRES0 = 87.

Figure 6. THRES_CFG0 Register

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				THRES1										THRES0									
R-0h				R-0h										R-0h									

LEGEND: R/W = Read/Write; R = Read only

THRESMAP_CFG1 need to be set to map the THRES01 and THRES1 values the designated input pin thresholds. In this example, two thresholds need to be set and mapped.

THRES1 need to be map to THRES2B: THRESMAP_IN12_IN17_THRES2B is set to 1h (Table 9).

THRES0 need to be map to THRES2A: THRESMAP_IN12_IN17_THRES2A is set to 0h (Table 9).

Table 9. THRESMAP_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
23-18	RESERVED	R	0h	Reserved
17-15	THRESMAP_IN12_IN17_THRES2B	R/W	0h	0h = THRES0 1h = THRES1 2h = THRES2 3h = THRES3 4h = THRES4 5h = THRES5 6h = THRES6 7h = THRES7
14-12	THRESMAP_IN12_IN17_THRES2A	R/W	0h	0h = THRES0 1h = THRES1 2h = THRES2 3h = THRES3 4h = THRES4 5h = THRES5 6h = THRES6 7h = THRES7

6.6 Interrupt enable and start monitoring

After the thresholds had been set, the interrupt needs to be set properly for TIC12400-Q1 to start the switch monitoring process.

- The Switch Status Change (SSC) interrupt need to be enabled so when switch state had changed, interrupt is generated and alert the micro-controller. SSC interrupt can be enabled by setting the SSC bit to 1 in the INT_EN_CFG0 register and enable the desired channels by setting INT_EN_CFG1 to INT_EN_CFG4. Start TIC12400-Q1 operation by setting the TRIGGER bit in CONFIG register to 1 and read the INT_STAT register to clear the baseline SSC interrupt (*Step 6*).
- Start monitoring by reading the interrupt status register INT_STAT when $\overline{\text{INT}}$ pin is asserted and then read the IN_STAT_ADC0/ IN_STAT_ADC1 for switch status (*Step 8b*). The raw code can also be retrieved in ANA_STATx registers.

7 References

TIC12400-Q1 24-Input Multiple-Switch Detection Interface (MSDI), data sheet

To further training on the advantages of using TIC12400-Q1, please see *TIC12400-Q1 training*.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265