Built-In Self-Test (BIST) Using Boundary Scan

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Abstract

The IEEE standard boundary-scan framework and four-wire serial testability bus have a positive impact on design for testability at all levels of electronic assembly, but do not solve all the testing problems facing the electronics industry. They form the basis from which other test techniques can be developed to further facilitate the testing of chips and systems. This paper describes a test architecture, based on the IEEE 1149.1 boundary-scan and test-bus standard. This architecture extends the capability of boundary testing from a purely scan-based structure into one that also supports a built-in self-test (BIST) capability.

Introduction

Before the formation of the Joint Test Action Group (JTAG) and the IEEE 1149.1 standard, the Test Automation Department of TI's Defense Systems and Electronics Group (DSEG), had considered boundary scan as a method to improve the test, integration, and maintenance of systems being designed for the Department of Defense (DoD). From this study, an architecture was developed, along with a library of specialized test cells particularly well-suited for boundary-scan and BIST applications.

SCOPE Architecture

The test architecture, referred to as System Controllability, Observability, and Partitioning Environment (SCOPE™), provides boundary scan and BIST capability to each input and output pin of the host IC. The architecture is supported by a library of modular bit slice called SCOPE cells that offer a range of boundary test capability. Some of the cells are targeted for simple boundary-scan applications. Other cells support the design of more sophisticated boundary test circuits such as pseudorandom and binary pattern generators and parallel signature analysis registers. During test, the SCOPE cells receive control from the test bus interface to execute a boundary scan or BIST controllability and observability test operation. One novel feature of the SCOPE architecture is its ability to activate the boundary test circuits while the host IC is in a normal operational mode. This capability provides boundary test features to support system integration, emulation, and at-speed testing.

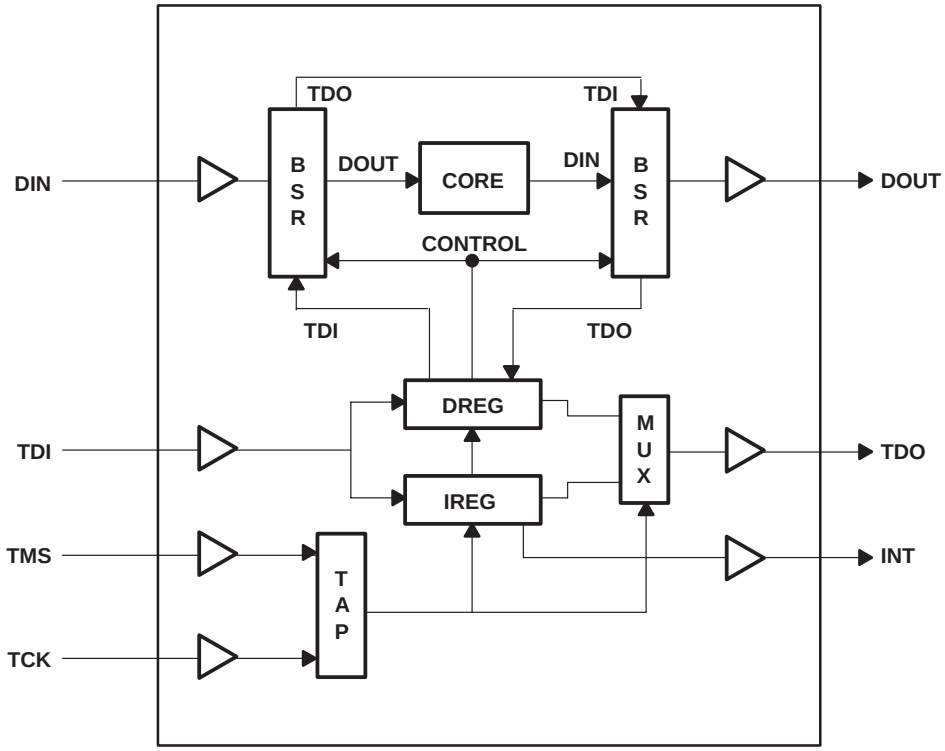

Figure 1. IEEE 1149.1 Architecture

Adapting SCOPE to 1149.1

Adapting the SCOPE architecture to the 1149.1 standard was simple because the existing test bus and architecture had similar functionality and required the same number of serial test bus pins. The following sections describe the boundary test features provided in the SCOPE architecture to support the mandatory test instructions required by the 1149.1 standard, as well as some of the internal test capabilities developed to extend the range of boundary testing.

1149.1 Architecture and Test Bus

The 1149.1 boundary-scan architecture and four-wire test bus interface is shown in Figure 1. The test architecture consists of a test access port (TAP), two separate shift register paths for data (DREG) and instruction (IREG) and a boundary-scan path bordering the IC's input and output pins. The boundary-scan path is one of two required scan paths residing in the DREG and is shown outside the DREG for clarity. The other required DREG scan path is a bypass register that consists of a single scan cell and is used to provide an abbreviated path through the DREG when testing is not being performed. In addition to these two required data registers, any number of user-defined shift registers can be included in the DREG to allow expanding the architecture to support additional test capabilities.

The 1149.1 test bus interface consists of a test data input (TDI), a test data output (TDO), a test mode select (TMS), and a test clock (TCK). The TDI is routed to both the DREG and IREG and is used to transfer serial data into one of the two shift registers during a scan operation. The TDO is selected to output serial data from either the DREG or IREG during a scan operation. The TMS and TCK are control inputs to the TAP. These control signals direct the operation of the architecture to perform scan operations to either the DREG or IREG, or to issue a reset condition to the test logic if test operations are not being performed.

Interrupt Pin and Application

The interrupt output signal is not defined in the IEEE 1149.1 specification but has been envisioned as a potential mode of operation for SCOPE architectures. Although this signal is not a standard function in every SCOPE IC product, it is a powerful function that can be implemented when using TI's ASIC library SCOPE cells.

In Figure 1, the interrupt (INT) output signal issued from the IREG is a signal defined in the SCOPE architecture. This signal can be used for, among other things, the output of a parity test indication of whether the instruction shifted into the IREG has the correct number of ones for even parity. The test instructions for the SCOPE architecture are all designed to a fixed length and include even parity. If an instruction is shifted in with odd parity, the interrupt output signal is set low when the TAP enters the pause-IR state to indicate the error back to a bus controller device. The pause-IR state is a steady state in the TAP controller's state diagram (see the IEEE 1149.1 specifications) that can be entered before terminating the instruction shift operation. The SCOPE architecture takes advantage of the pause-IR state to verify that the instruction shifted in has the correct parity. If the INT output is low, indicating a parity error condition, the bus master will repeat the instruction scan operation again. INT output high indicates a good parity condition. If so, the bus master will complete the instruction scan operation by updating the instruction into the IREG output latch to issue the appropriate test control to the architecture.

Test Bus and Interrupt Pin Connections

In the example circuit of Figure 2, three ICs are shown interconnected functionally via direct wiring bus paths. During normal operation, ICs 1, 2, and 3 receive input via their data input (DIN) buses and issue output via their data output (DOUT) buses to execute a designed circuit function. Also, the three ICs are shown interconnected in a serial ring configuration via the four-wire test bus. The TIC block in each IC stands for test interface and control and is representative of the TAP, IREG, and DREG sections shown in Figure 1. The 1149.1 test bus is designed to allow scan operations to occur through the TIC while the IC is operational. This is possible because the test pins and the required test logic of the boundary scan architecture (TAP, IREG, DREG boundary and bypass registers) are dedicated for test and cannot be reused for functional purposes.

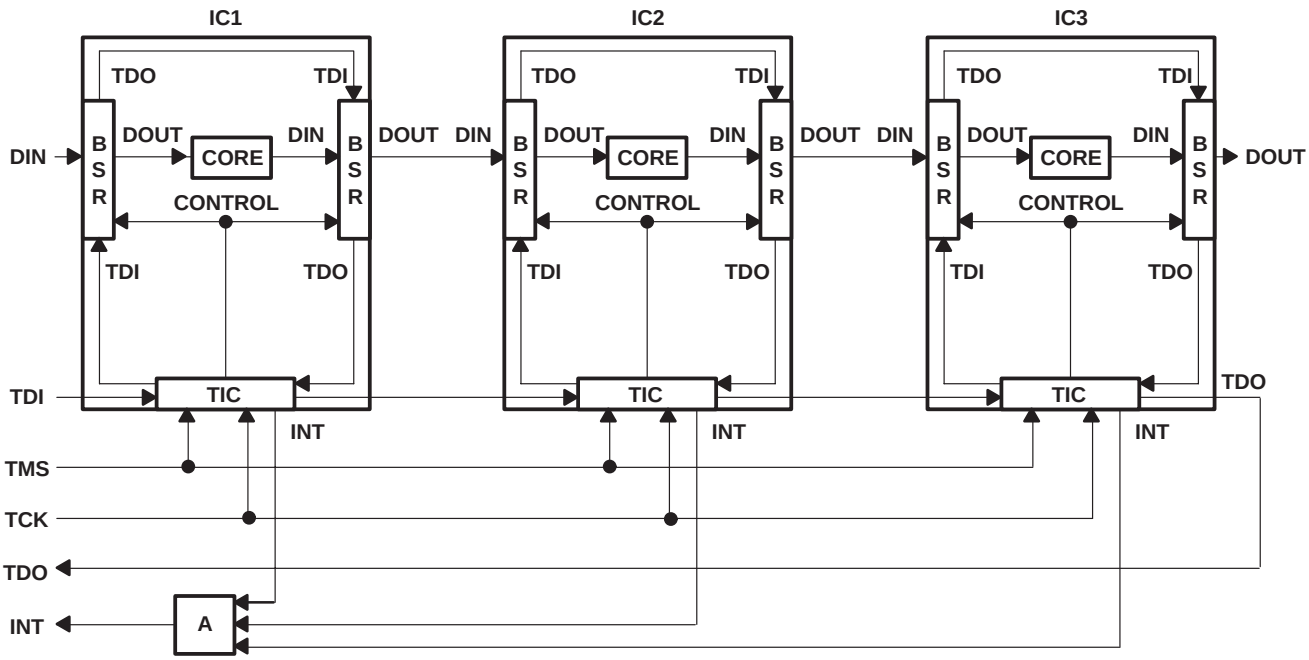

Figure 2. IEEE 1149.1 Architecture

The INT output signal from each IC is input to an external AND function to produce a global INT output signal. The global INT signal from the AND function is input to a bus master device. The device includes a five-pin interface to support the four required 1149.1 test bus signals and the additional INT signal. During the pause-IR state of an instruction register scan operation, each local INT signal outputs a parity pass or fail condition. If all local INT outputs are high, the AND function outputs a high to the bus master to confirm good parity. If one or more local INT outputs are low, the AND function outputs

a low to the bus master to indicate an instruction parity failure. The advantage of using an active AND function to combine the local INT outputs versus a passive wired-OR configuration is speed. Speed is not a high priority for global parity testing. Other INT functions defined in the SCOPE architecture do require a minimum delay between the occurrence of one or more local INT outputs and a resulting global INT output signal to the bus master.

1149.1 Boundary Test Instructions

The following is a description of the required 1149.1 test instructions that are included in the SCOPE architecture. The other optional 1149.1 instructions (INTEST, IDCODE, RUNBIST) can be implemented as required.

EXTEST Instruction

One of the required test instructions in the 1149.1 specification is defined as an external boundary test (EXTEST) instruction. When this instruction is shifted into the IREG of the ICs in Figure 2, the ICs are forced into an off-line test mode. While this instruction is in effect, the test bus can shift data through the boundary scan registers of each IC to observe and control the external DIN and DOUT buses, respectively. As seen in the circuit of Figure 2, serialized test patterns can be shifted in and applied from the output boundary scan register's DOUT to drive the wiring interconnect to the DIN of neighboring ICs. After the test pattern is output, the DIN of the receiving ICs are captured. Following the data capture operation, the boundary registers are shifted to load the next external test pattern and to extract the response from the first test pattern. This process is repeated until the wiring interconnects are tested. This test provides a simple and thorough verification of the wiring connections between ICs in a circuit and is the key motivation behind the JTAG initiative.

SAMPLE Instruction

A second required test instruction in the 1149.1 specification is defined as a boundary register sample instruction. When this instruction is shifted into the IREG of one or more of the ICs in Figure 2, the IC remains fully operational. While this instruction is in effect, a DREG scan operation will transfer serial data from the TDI, through the boundary scan register, to the TDO of the IC.

During this instruction, the data appearing at the DIN are captured and shifted out for inspection. The data are captured in response to control being input to the internal TAP controller via the TCK and TMS input signals.

While this is potentially a very powerful test instruction, it requires further definition by the user as to when control is issued on the TCK and TMS signal to capture data. If all the ICs in Figure 2 operate their input and output functions synchronous to the same system clock, the TCK and TMS input can be synchronized with the system clock to sample all the ICs simultaneously. However, if all ICs operate their functions synchronous to separate asynchronous system clocks, then the TMS and TCK control signals must be made to operate in sync with just one IC system clock to sample each individual IC.

BYPASS Instruction

A third required test instruction in the 1149.1 specification is defined as a bypass scan instruction. When this instruction is shifted into the IREG of one or more of the ICs in Figure 2, the IC remains fully operational. While this instruction is in effect, a DREG scan operation will transfer serial data from the TDI, through a single internal scan cell, to the TDO of the IC. The purpose of the instruction is to abbreviate the scan path through ICs that are not being tested to only a single-scan clock delay.

SCOPE Boundary Test Instructions

To expand the test capability of a boundary-scan architecture and thus support a broader range of testing needs, additional test instructions and hardware capabilities are defined in the SCOPE architecture. Following is a description of some of these additional test instructions and the benefits gained from them.

TOGGLE/SAMPLE Instruction

The 1149.1 EXTEST instruction is excellent for testing the integrity of wiring interconnects between the ICs. However, it cannot be used effectively to test for timing delay problems that may occur between an output buffer of a driving IC and an input buffer of a receiving IC. To test for signal-path time delays, data must be applied from the outputs of one IC and be sampled rapidly into the inputs of another IC. To perform a delay test by transitioning through the TAP controller's state

diagrams would take at least 1.5 TCK cycles from the time data are applied from one IC's output boundary in the update-DR state to when the data could be captured at the input boundary of another IC during the capture-DR state.

To perform faster, simple signal-path delay tests between an output and input boundary, SCOPE cells were designed to include a toggle mode. This mode can be invoked by a TOGGLE/SAMPLE test instruction to allow the output boundary of an IC to drive out alternating logic states on the falling edge of successive TCK inputs. The same instruction also configures the SCOPE cells on the IC input boundary into a sample mode. This allows the data appearing at the inputs to be captured on the rising edge of successive TCK inputs. Using this approach, signal-path delay testing can be performed over the time interval between a falling and rising edge of TCK. For example, with a 10-MHz, 50-percent duty-cycle TCK input, a signal-path delay exceeding 50 nanoseconds can be detected using this approach.

This instruction is executed while the TAP is in the run test/idle (RT/IDLE) state, so TAP state transitions are not required. After the input cells sample the toggled logic state, the data captured are shifted out for inspection. While this delay testing approach is still rather crude compared to the resolution of state-of-the-art test equipment, it still can serve a purpose at the circuit-board level. Using this technique, typical types of signal-path delays that can be identified are shown in Figure 3. These include combinational logic delays between the boundaries of larger ICs, delays associated with open collector-type output buffers, and delays associated with output buffers with high fanout loads.

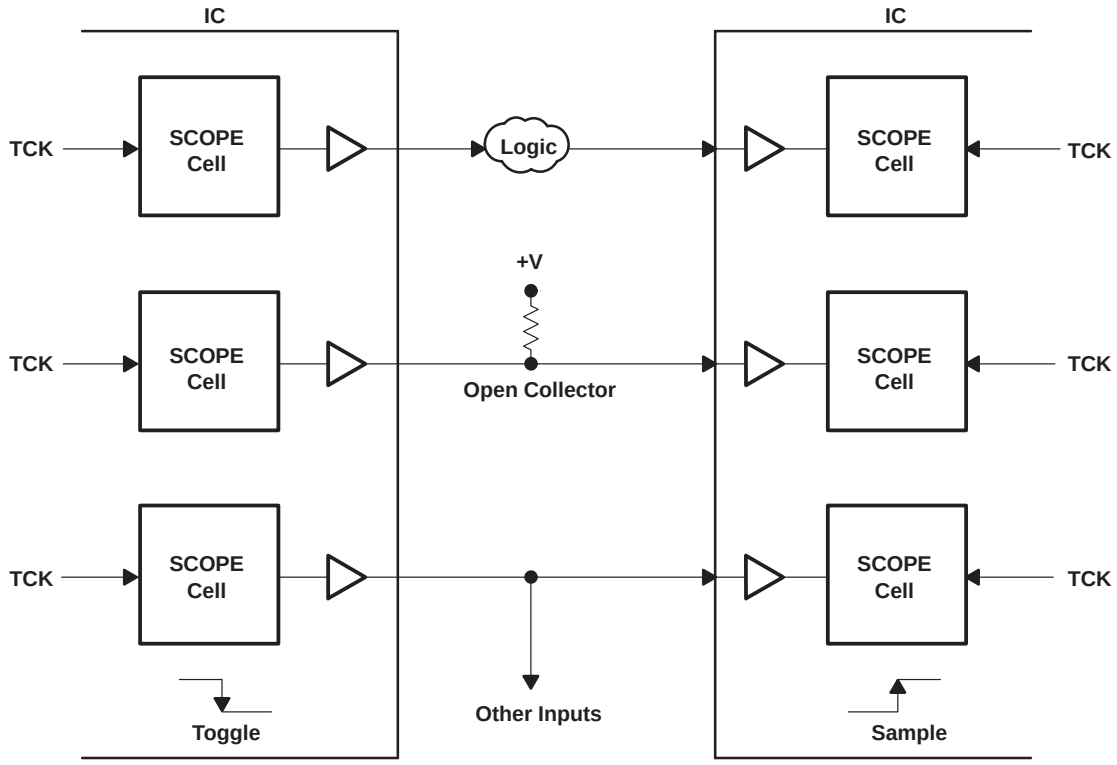

Figure 3. Using TOGGLE/SAMPLE to Test Path Delays

HIGHZ Instruction

When this instruction is shifted into the instruction register, the IC is set in an off-line test mode, and the output buffers are placed in a high-impedance state. While this instruction is in effect, the bypass register is selected to shift data through the DREG from the TDI to the TDO. This instruction is included to ease in-circuit testing of ICs in a circuit that does not incorporate boundary scan. Since the output buffers can be set tristate, the concerns with backdriving the output buffers of one IC to apply a test to a neighboring IC are reduced.

CLAMP Instruction

When this instruction is shifted into the instruction register, the IC is set in an off-line test mode. The input and output buffers are driven to a predetermined output pattern that has been scanned into the boundary register. While this instruction is in effect, the bypass register is selected to shift data through the DREG from the TDI to the TDO. This instruction allows the output

signals of one or more ICs in a circuit to be set and left in a preferred output state while testing is being performed on one or more neighboring ICs in the circuit. The key to this instruction is that it allows the bypass register to be selected while the IC remains in a test mode with outputs set, as required, for testing. The 1149.1 clamp instruction forces the IC into normal operation when the bypass register is selected; thus, any preferred output signal setting for test cannot be maintained during the instruction.

BOUNDARY SELF-TEST Instruction

When this instruction is shifted into the instruction register, the boundary scan cells are configured to allow self-testing of each cell in the scan path. The self-test exercises most of the logic in each test cell. The test involves initializing the cells with a test pattern via a scan operation, followed by a second scan operation to shift out the test results. If the cells pass the self-test, the pattern shifted out during the second scan operation will be the inverse of the first pattern shifted in. During this instruction, the IC remains in its normal operation mode to allow self-testing to occur in the background, if desired.

BOUNDARY READ Instruction

When this instruction is shifted into the instruction register, the boundary-scan register is selected to shift data from the TDI to the TDO. This instruction differs from the 1149.1 EXTEST and SAMPLE instruction in that the boundary cells remain in their present state during the TAP controller's capture-DR state. The reason for this instruction is to allow shifting out of the existing contents of the boundary-scan register. When a signature is collected in the boundary-scan register during a run test instruction, this instruction could disable the load function that normally occurs in the TAP controller's capture-DR state to allow shifting out the signature.

BOUNDARY BIST Instruction

In the example of Figure 4, a circuit consisting of three ICs is interconnected through combinational logic islands. During normal operation, the ICs transfer data from their DOUTs to a neighboring IC's DINs via the combinational logic and wiring interconnect. While this illustration exaggerates the amount of logic that would normally reside between major ICs in a circuit, it does show the test-time penalties paid in using a purely scan-operated boundary-scan architecture.

The 1149.1 EXTEST instruction is fully capable of testing the combinational logic between the boundaries of the ICs in Figure 4. The time required to accomplish the test is very long compared to a BIST approach. For example, consider the number of TCK inputs required to shift the boundary-scan paths of the ICs to apply one test pattern is equal to (M), the TCK period is equal to (T), and the combinational logic island being tested has (n) inputs. The total boundary-scan test time to apply an exhaustive test can be approximated by Equation 1. For a 10-MHz TCK, a 200-TCK scan operation, and an 8-bit-wide combinational logic island, the test time is equal to around 5 milliseconds.

$$\frac{Boundary\ Scan}{Test\ Time} = (T\ M\ 2^n) \quad \textbf{(1)}$$

By eliminating the need to traverse the boundary-scan paths of the ICs each time a new test pattern is to be applied, the M variable drops out of Equation 1 to produce the boundary BIST time in Equation 2. Using Equation 2, the time to test the same combinational logic island at the same TCK rate is equal to around 25 microseconds.

$$\frac{Boundary\ BIST}{Test\ Time} = (T\ 2^n) \quad \textbf{(2)}$$

Comparing the 5-millisecond, scan-operated test time against the 25-microsecond BIST-operated test time results in a 99.5-percent reduction in test time using the BIST approach. That is why a boundary BIST capability is included in the SCOPE architecture.

To support a boundary BIST capability, the SCOPE cell library includes cells that can be used to construct boundary registers with pattern-generation and data-compression capabilities. The pattern-generation test cells can produce either pseudorandom or binary output test patterns. The data-compression test cells operate together as a parallel signature analysis (PSA) register. The cells also include programmable polynomial taps to allow modifying the feedback connections. This optimizes the operation of the pattern-generation and data-compression register for a particular external logic configuration.

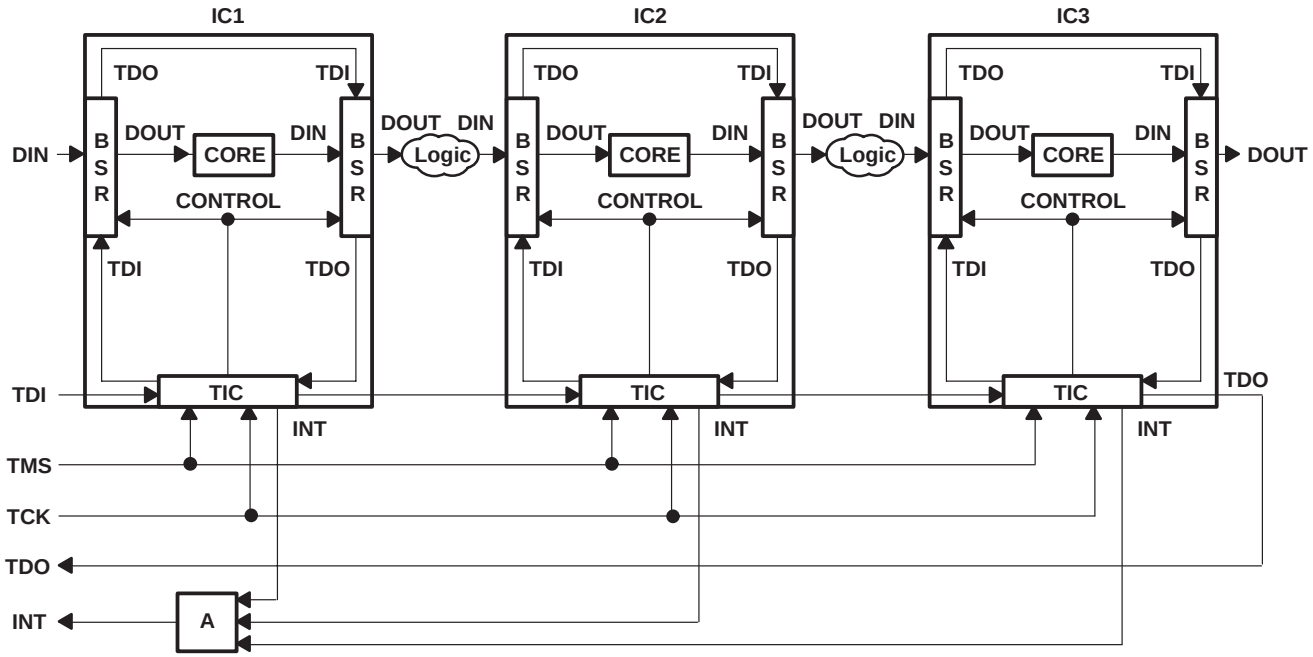

Figure 4. Testing Combinational Logic With IEEE 1149.1/BIST

When the boundary scan paths of the ICs in Figure 4 are designed using these advanced test cells, the combinational logic islands are tested much more easily and quickly. The boundary BIST test is set up by scanning seed values into the input and output boundary register sections that border the combination logic islands. After the boundary registers are set up, a run test instruction is shifted into the instruction register, and the test begins when the TAP controller enters its RT/IDLE state. During the test, the output patterns are applied from an IC's output boundary register on the falling edge of TCK to drive the combinational logic. The output response from the combinational logic is input to the IC's input boundary register, where it is sampled into the PSA register on the rising edge of TCK. When the test is complete, the TAP controller transitions from the RT/IDLE state and shifts a boundary read instruction into the instruction register. The boundary read instruction selects the boundary register to allow the signatures collected to be shifted out for inspection.

Summary

The 1149.1 standard provides a basic framework for boundary testing. A user may take this basic framework and use it as it is or build on top of it the types of test structures and operations required to satisfy particular testing needs. This paper illustrates how an existing architecture can be modified to conform to the 1149.1 architecture. Also, adapting to the new architecture does not require giving up any pre-existing test capabilities. In addition, a boundary BIST approach was described and compared to a purely scan-operated boundary test approach. This comparison shows the benefits of a boundary BIST approach to be a significant reduction in the time to test combinational logic residing between the boundaries of ICs in a circuit.

Acknowledgment

The author of this document is Lee Whetsel.

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