Application Report
SCYA007 - October 1999

Comparison of Electrical and Thermal Parameters of Widebus™ SMD SSOP, TSSOP, TVSOP, and LFBGA Packages

Johannes Huchzermeier *Standard Linear and Logic*

ABSTRACT

The trend toward 16- and 32-bit-wide bus systems, in conjunction with continuing advances in surface-mount technology during the 1980s and 1990s, led to the development of ever-smaller packages combined with increased integrated-circuit performance. The improvement in the electrical characteristics of the packages also made possible development of smaller-footprint packages for Widebus™ circuits. In the mid-1980s, Texas Instruments produced Widebus™ devices with improved electrical characteristics and expanded data width, supporting up to 20 bits in a single package.

Now, Texas Instruments is launching the low-profile, fine-pitch, ball grid array (LFBGA). The LFBGA is the first ball grid array package (BGA) for logic components, featuring improved signal characteristics, as well as increased integration.

With new designs that support up to 36 bits in a single package, doubling of component density on the printed circuit board using Widebus packages has been achieved.

The purpose of this report is to familiarize designers with the advantages of this package option by comparing the mechanical data, electrical characteristics, and thermal parameters of four packages: 48-pin SSOP (Shrink Small-Outline Package), 48-pin TSSOP (Thin Shrink Small-Outline Package), 48-pin TVSOP (Thin Very Small-Outline Package), and 96-pin LFBGA (Low-profile Fine-pitch Ball Grid Array), using the 244-function (unidirectional) buffer/driver of the LVC logic family.

Widebus is a trademark of Texas Instruments Incorporated

Contents

Introduction 4
Package Parameters 5
Packages and Package Parameters Investigated 6
Electrical Characteristics 13
Simultaneous-Switching Behavior 15
Increase in Propagation Delay Time 27
Thermal Properties 30
Package Dimensions and Size Comparison 36
Summary 41
Acknowlegment 41
Glossary 42
Bibliography 44

List of Figures

1. 16-Bit Widebus Package for 48-Pin SSOP, TSSOP, and TVSOP Packages 6
2. 32-Bit Package for 96-Ball Low-Profile Fine-Pitch Ball Grid Arrays 7
3. Influence of Slew Rate on Propagation Delay Time and the Principle Behind OEC 14
4. Basic Structure of the OEC Output Stage 14
5. Simultaneous-Switching Measurement Setup 16
6. Simultaneous Switching Parameter 18
7. Measured Simultaneous-Switching Ground Bounce, SSOP 48-Pin Package 18
8. Measured Simultaneous-Switching Ground Bounce, TSSOP 48-Pin Package 19
9. Measured Simultaneous-Switching Ground Bounce, TVSOP 48-Pin Package 19
10. Measured Simultaneous-Switching Ground Bounce, LFBGA 96 Ball 20
11. Measured Simultaneous-Switching High Bounce, SSOP 48-Pin Package 20
12. Measured Simultaneous-Switching High Bounce, TSSOP 48-Pin Package 21
13. Measured Simultaneous-Switching High Bounce, TVSOP 48-Pin Package 21
14. Measured Simultaneous-Switching High Bounce, LFBGA 96 Ball 22
15. Simultaneous-Switching Ground Bounce, SSOP 48 Pin (top), TSSOP 48 Pin (bottom) 23
16. Simultaneous-Switching Ground Bounce, TVSOP 48 Pin (top), LFBGA 96 Ball (bottom) 24
17. Simultaneous-Switching Ground Bounce, SSOP 48 Pin (top), TSSOP 48 Pin (bottom) 25
18. Simultaneous-Switching High Bounce, TVSOP 48-Pin (top), LFBGA 96 Ball (bottom) 26
19. Rising-Edge Propagation Delay Time Relative to the Number of Simultaneously Switching Outputs for the SSOP, TSSOP, TVSOP, and LFBGA Packages 28
20. Falling-Edge Propagation Delay Time Relative to the Number of Simultaneously Switching Outputs for the SSOP, TSSOP, TVSOP, and LFBGA Packages 28
21. Maximum Power Consumption Relative to Ambient Temperature, T_J = 150°C, SSOP 48-Pin Package 34
22. Maximum Power Consumption Relative to Ambient Temperature, T_J = 150°C, TSSOP 48-Pin Package 34
23. Maximum Power Consumption Relative to Ambient Temperature, T_J = 150°C, TVSOP 48-Pin Package 35
24. Maximum Power Consumption Relative to Ambient Temperature, T_J = 150°C, LFBGA 96 Ball 35
25. Dimensions of the SSOP 28-, 48-, and 56-Pin Packages 36

List of Figures (continued)

26. Dimensions of the TSSOP 48-, 56-, and 64-Pin Packages 37
27. Dimensions of the TVSOP 48-, 56-, and 64-Pin Packages 38
28. Dimensions of the LFBGA 96-Ball Package 39
29. Space Needed for a 32-Bit Interface Using Various Packages Options 40

List of Tables

1. SSOP 48-Pin Capacitance, Inductance, and Coupling-Factor (k) Package Parameters 8
2. TSSOP 48-Pin Capacitance, Inductance, and Coupling-Factor (k) Package Parameters 9
3. TVSOP 48-Pin Capacitance, Inductance, and Coupling-Factor (k) Package Parameters 10
4. LFBGA 96-Ball Package Parameters (Balls 1 – 48) (Balls 49 – 96 Analog) 11
5. Comparison of Capacitance, Inductance, and Coupling-Factor (k) Package Parameters 12
6. Comparison of the Thermal Resistance ($R_{\theta JA}$) of Different Packages 29

Introduction

The introduction of surface-mount technology at the beginning of the 1980s led to a major reduction in the component space needed on the circuit board. Users exploited this advantage either by reducing the space needed for a given system or by increasing system performance, while using the same amount of space. The steadily increasing integration of electrical circuitry also created pressure for advances in the miniaturization of packages. Standard components, such as bus drivers, also were produced in ever-smaller space-saving packages.

During the same period, the transition from 8-bit processors to 16- and 32-bit processors occurred. The associated enlargement of data and address buses tended to counteract the space advantage that had been gained because two or four modules now had to be used in place of a single bus driver.

In order to satisfy the user's need for more compact equipment, Texas Instruments (TI™) developed new packages suitable for surface-mount technology:

- SSOP (Shrink Small-Outline Package) doubles the number of bits within one package, while requiring no more space than the usual 8-bit SOP (Small Outline Package) modules
- TSSOP (Thin Shrink Small-Outline Package) represents a significant space saving over the SSOP package, and also is suitable for use in PCMCIA plug-in boards due its reduced package height
- TVSOP (Thin Very Small-Outline Package) permits a further space saving of up to 38% compared to the TSSOP package

Also, emphasis was placed on important factors, such as the speed of the new functions, while striving to keep interference voltages as low as possible.

However, miniaturization of package types to 0.4 mm pin-to-pin distance, reached the limit for reliable manufacturing processes, and led to the development of ball grid arrays.

The LFBGA (Low-profile Fine-pitch Ball Grid Array) package represents the ideal solution because it combines minimal space requirements with low package parasitics and a high level of functional density.

This report compares the dimensions, electrical characteristics, and thermal parameters of four packages:

SSOP	(Shrink Small-Outline Package) for Widebus	48-pin DL
TSSOP	(Thin Shrink Small-Outline Package) for Widebus	48-pin DGG
TVSOP	(Thin Very Small-Outline Package) for Widebus	48-pin DGV
LFBGA	(Low-profile Fine-pitch Ball Grid Array)	96-ball GKE

In addition to package names and the number of external connections, each package type is designated by a clearly defined abbreviation (e.g., DL, DGG, DGV, and GKE), which is used when ordering a component.

The influence of package type on electrical characteristics is investigated in this application report, using measurements on the unidirectional buffer components SN74LVH16244A and SN74LVCH32244A.

TI is a trademark of Texas Instruments Incorporated

Package Parameters

The increasing speed of integrated circuits makes the electrical characteristics of the package even more important.

In addition to the inevitable parasitic capacitances of the leads within a package, their inductance is the major factor determining the behavior of fast digital circuits, limiting ranges of applications in some cases.

Furthermore, with reduced distances between pins, the pins' coupling factors are increasingly important.

Supply-voltage connections should have low inductance values. For all signal lines a good package should show the lowest possible values for the following electrical variables:

- Capacitance of a pin against ground
- Inductance of the pins
- The pins' mutual-coupling factors.

The pins' mutual-coupling factors can be determined, using the general-transformer equation.

$$k = \frac{M}{\sqrt{L_1 \times L_2}} \quad (1)$$

Where:

M	= coupling inductance
L_1 and L_2	= respective self-inductance of the pin connections
k	= the inductive coupling factor

The three electrical variables of a package are determined by:

- Line length of the pins in the package
- Distance between the lines
- Length of the bonding wires.

For purposes of comparison, note that large dual in-line packages, PDIPs (plastic dual in-line packages), for example, have significantly longer leads than SSOP, TSSOP, TVSOP, or LFBGA packages.

A long lead produces high inductance and high coupling factors. Also, the large surfaces resulting from the long line result in higher capacitance. With small package types, such as the TSSOP, the inductance and capacitance of the leads is significantly less. However, the coupling-factor advantage gained by the short leads is partially offset by the minimal distance between the leads, thereby increasing the coupling factor.

To a lesser extent, the size of the chips and the lead frame used for the chip also have an influence on the electrical characteristics. Accordingly, the measurement results given in this chapter should be regarded as typical values that relate only to the component tested in each package. However, typical dependencies for each package type may be inferred from the measurements obtained.

Packages and Package Parameters Investigated

Figures 1 and 2 show the pin and ball layout, respectively, of the Widebus and the LFBGA packages. Tables 1 through 4 show the capacitance and inductance of the individual pins of the 48-pin SSOP, TSSOP, and TVSOP, and the 96-pin low-profile fine-pitch ball grid array packages. Additionally, the tables give the coupling factors between neighboring pins. As a basis for this comparison, the respective SPICE package models have been used. Minor deviations are possibly due to the use of different lead frames, i.e., the metal masks to which the chip is attached inside the package.

Tables 1 through 4 give capacitance, inductance, and coupling-factor parameters for each of the packages discussed in this report.

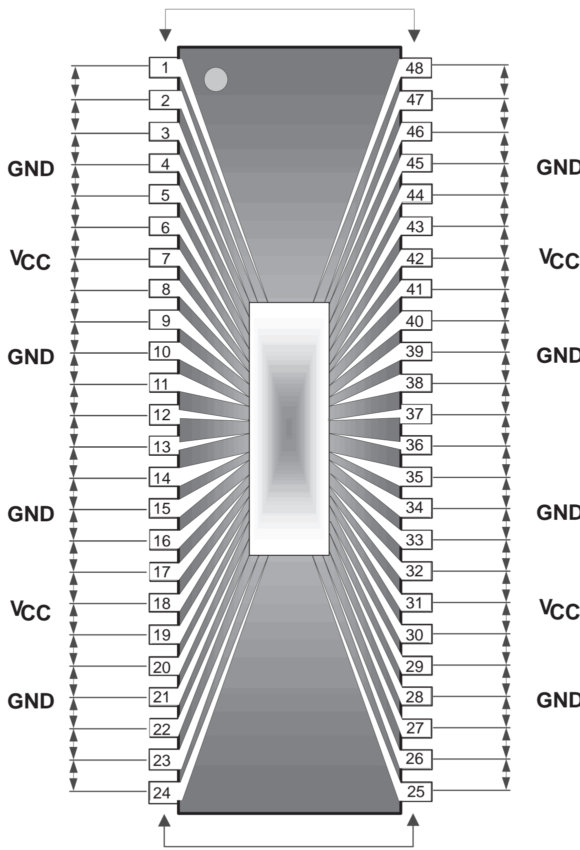


Figure 1. 16-Bit Widebus Package for 48-Pin SSOP, TSSOP, and TVSOP Packages

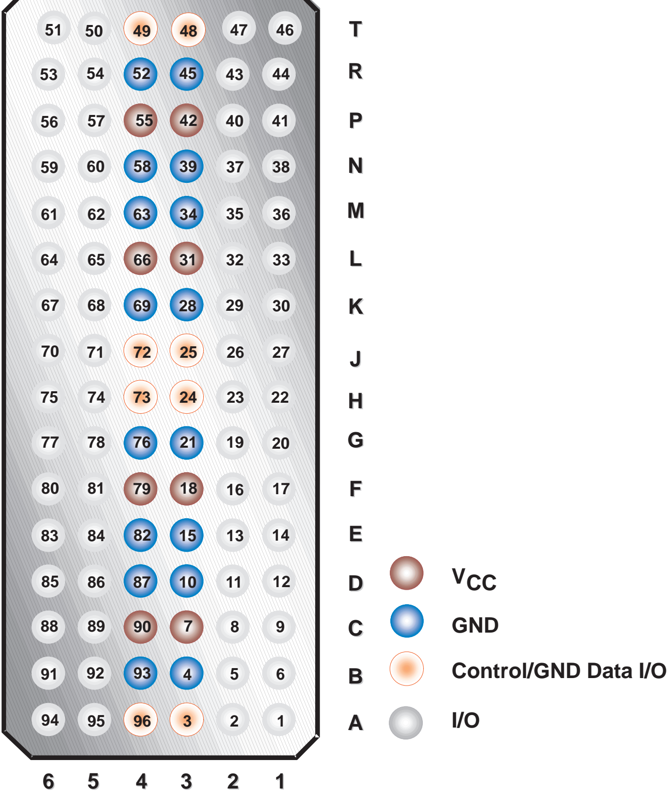


Figure 2. 32-Bit Package for 96-Ball Low-Profile Fine-Pitch Ball Grid Arrays

Table 1. SSOP 48-Pin Capacitance, Inductance, and Coupling-Factor (k) Package Parameters

Pin	Capacitance Pin to GND (pF)	Inductance Die to Pin (nH)	Coupling Factor (k)			Pin	Capacitance Pin to GND (pF)	Inductance Die to Pin (nH)	Coupling Factor (k)		
			Pin	Pin	Factor				Pin	Pin	Factor
1	0.44	7.97	1	2	0.48	48	0.44	7.97	48	1	0.06
2	0.24	7.30	2	3	0.49	47	0.24	7.30	47	48	0.48
3	0.20	6.76	3	4	0.49	46	0.20	6.76	46	47	0.49
4	0.18	6.27	4	5	0.48	45	0.18	6.27	45	46	0.49
5	0.16	5.86	5	6	0.46	44	0.16	5.86	44	45	0.48
6	0.16	5.80	6	7	0.46	43	0.16	5.80	43	44	0.46
7	0.18	5.66	7	8	0.47	42	0.18	5.66	42	43	0.46
8	0.12	5.50	8	9	0.47	41	0.12	5.50	41	42	0.47
9	0.10	5.30	9	10	0.48	40	0.10	5.30	40	41	0.47
10	0.08	5.19	10	11	0.48	39	0.08	5.19	39	40	0.48
11	0.07	5.08	11	12	0.44	38	0.07	5.08	38	39	0.48
12	0.21	5.86	12	13	0.54	37	0.21	5.86	37	38	0.44
13	0.21	5.86	13	14	0.44	36	0.21	5.86	36	37	0.54
14	0.07	5.08	14	15	0.48	35	0.07	5.08	35	36	0.44
15	0.08	5.19	15	16	0.48	34	0.08	5.19	34	35	0.48
16	0.10	5.30	16	17	0.47	33	0.10	5.30	33	34	0.48
17	0.12	5.50	17	18	0.47	32	0.12	5.50	32	33	0.47
18	0.18	5.66	18	19	0.46	31	0.18	5.66	31	32	0.47
19	0.16	5.80	19	20	0.46	30	0.16	5.80	30	31	0.46
20	0.16	5.86	20	21	0.48	29	0.16	5.86	29	30	0.46
21	0.18	6.27	21	22	0.49	28	0.18	6.27	28	29	0.48
22	0.20	6.76	22	23	0.49	27	0.20	6.76	27	28	0.49
23	0.24	7.30	23	24	0.48	26	0.24	7.30	26	27	0.49
24	0.44	7.97	24	25	0.06	25	0.44	7.97	25	26	0.48

Table 2. TSSOP 48-Pin Capacitance, Inductance, and Coupling-Factor (k) Package Parameters

Pin	Capacitance Pin to GND (pF)	Inductance Die to Pin (nH)	Coupling Factor (k)			Pin	Capacitance Pin to GND (pF)	Inductance Die to Pin (nH)	Coupling Factor (k)		
			Pin	Pin	Factor				Pin	Pin	Factor
1	0.41	3.92	1	2	0.39	48	0.40	3.99	48	1	0.03
2	0.22	3.63	2	3	0.38	47	0.22	3.63	47	48	0.4
3	0.19	3.37	3	4	0.36	46	0.19	3.31	46	47	0.39
4	0.18	3.02	4	5	0.35	45	0.17	3.06	45	46	0.37
5	0.19	2.99	5	6	0.34	44	0.17	2.91	44	45	0.35
6	0.20	2.81	6	7	0.31	43	0.18	2.80	43	44	0.34
7	0.12	2.71	7	8	0.32	42	0.16	2.69	42	43	0.34
8	0.12	2.70	8	9	0.33	41	0.11	2.58	41	42	0.33
9	0.10	2.59	9	10	0.35	40	0.10	2.52	40	41	0.34
10	0.09	2.54	10	11	0.35	39	0.09	2.45	39	40	0.35
11	0.08	2.46	11	12	0.36	38	0.08	2.37	38	39	0.34
12	0.08	2.43	12	13	0.35	37	0.08	2.37	37	38	0.36
13	0.08	2.42	13	14	0.35	36	0.08	2.37	36	37	0.35
14	0.08	2.45	14	15	0.35	35	0.08	2.38	35	36	0.36
15	0.09	2.50	15	16	0.35	34	0.09	2.44	34	35	0.36
16	0.10	2.55	16	17	0.34	33	0.10	2.51	33	34	0.34
17	0.11	2.62	17	18	0.33	32	0.11	2.57	32	33	0.34
18	0.15	2.69	18	19	0.33	31	0.16	2.69	31	32	0.33
19	0.18	2.83	19	20	0.34	30	0.18	2.78	30	31	0.33
20	0.17	2.98	20	21	0.35	29	0.17	2.87	29	30	0.33
21	0.17	3.06	21	22	0.37	28	0.17	2.98	28	29	0.35
22	0.19	3.34	22	23	0.39	27	0.19	3.26	27	28	0.37
23	0.22	3.66	23	24	0.39	26	0.22	3.55	26	27	0.39
24	0.40	3.96	24	25	0.03	25	0.40	3.89	25	26	0.4

Table 3. TVSOP 48-Pin Capacitance, Inductance, and Coupling-Factor (k) Package Parameters

Pin	Capacitance Pin to GND (pF)	Inductance Die to Pin (nH)	Coupling Factor (k)			Pin	Capacitance Pin to GND (pF)	Inductance Die to Pin (nH)	Coupling Factor (k)		
			Pin	Pin	Factor				Pin	Pin	Factor
1	0.30	4.02	1	2	0.38	48	0.30	4.01	48	1	0.13
2	0.18	3.72	2	3	0.39	47	0.18	3.72	47	48	0.38
3	0.14	3.46	3	4	0.39	46	0.14	3.44	46	47	0.39
4	0.12	3.21	4	5	0.4	45	0.12	3.20	45	46	0.39
5	0.12	2.93	5	6	0.42	44	0.12	2.93	44	45	0.4
6	0.12	2.80	6	7	0.38	43	0.12	2.80	43	44	0.42
7	0.08	2.68	7	8	0.4	42	0.08	2.67	42	43	0.37
8	0.07	2.58	8	9	0.4	41	0.07	2.56	41	42	0.39
9	0.06	2.51	9	10	0.41	40	0.06	2.47	40	41	0.39
10	0.06	2.40	10	11	0.42	39	0.06	2.43	39	40	0.41
11	0.05	2.40	11	12	0.41	38	0.05	2.39	38	39	0.41
12	0.05	2.40	12	13	0.42	37	0.05	2.38	37	38	0.41
13	0.05	2.43	13	14	0.42	36	0.05	2.42	36	37	0.42
14	0.05	2.46	14	15	0.42	35	0.05	2.47	35	36	0.42
15	0.06	2.59	15	16	0.41	34	0.06	2.55	34	35	0.41
16	0.06	2.65	16	17	0.4	33	0.06	2.64	33	34	0.4
17	0.07	2.79	17	18	0.39	32	0.07	2.78	32	33	0.4
18	0.08	2.96	18	19	0.39	31	0.08	2.88	31	32	0.39
19	0.12	3.21	19	20	0.41	30	0.11	3.23	30	31	0.37
20	0.12	3.49	20	21	0.39	29	0.12	3.52	29	30	0.42
21	0.12	3.49	21	22	0.39	28	0.12	3.52	28	29	0.4
22	0.14	3.74	22	23	0.38	27	0.14	3.70	27	28	0.38
23	0.18	3.99	23	24	0.38	26	0.18	3.93	26	27	0.39
24	0.30	4.31	24	25	0.12	25	0.30	4.29	25	26	0.38

Table 4. LFBGA 96-Ball Package Parameters (Balls 1 – 48) (Balls 49 – 96 Analog)

Ball	Capacitance Ball to GND (pF)	Inductance Ball to Die (nH)	Ball Number and Coupling															
1	0.14	2.87							2	0.25	5	0.08	6	0.06				
2	0.06	1.65							3	0.29	4	0.17	5	0.17	6	0.09	1	0.25
3	0.07	1.76							96		93		4	0.25	5	0.19	2	0.29
4	0.12	2.83	2	0.17	3	0.25	96		93		90		7	0.15	8	0.08	5	0.25
5	0.05	1.74	1	0.08	2	0.17	3	0.19	4	0.25	7	0.16	8	0.16	9	0.09	6	0.29
6	0.05	1.77			1	0.06	2	0.09	5	0.29	8	0.18	9	0.17				
7	0.11	2.75	5	0.16	4	0.15	93		90		87		10	0.16	11	0.19	8	0.26
8	0.05	1.66	6	0.18	5	0.16	4	0.08	7	0.26	10	0.18	11	0.19	12	0.10	9	0.29
9	0.05	1.75			6	0.17	5	0.09	8	0.29	11	0.22	12	0.17				
10	0.12	2.66	8	0.18	7	0.16	90		87		82		15	0.08	13	0.11	11	0.29
11	0.05	1.62	9	0.22	8	0.19	7	0.19	10	0.29	15	0.07	13	0.19	14	0.11	12	0.24
12	0.05	1.70			9	0.17	8	0.10	11	0.24	13	0.29	14	0.24				
13	0.06	1.91	12	0.29	11	0.19	10	0.11	15	0.15	18	0.06	16	0.16	17	0.10	14	0.29
14	0.05	1.73			12	0.24	11	0.11	13	0.29	16	0.18	17	0.18				
15	0.11	2.63	11	0.07	10	0.08	87		82		79		18	0.15	16	0.32	13	0.15
16	0.05	1.86	14	0.18	13	0.16	15	0.32	18	0.15	21	0.06	19	0.16	20	0.09	17	0.30
17	0.05	1.70			14	0.18	13	0.10	16	0.30	19	0.16	20	0.16				
18	0.11	2.67	13	0.06	15	0.15	82		79		76		21	0.15	19	0.32	16	0.15
19	0.05	1.91	17	0.16	16	0.16	18	0.32	21	0.16	24	0.06	23	0.12	22	0.11	20	0.30
20	0.05	1.68			17	0.16	16	0.09	19	0.30	23	0.12	22	0.20				
21	0.10	2.68	16	0.06	18	0.15	79		76		73		24	0.14	23	0.17	19	0.16
22	0.05	1.72			20	0.20	19	0.11	23	0.33	26	0.06	27	0.08				
23	0.05	1.60	20	0.12	19	0.12	21	0.17	24	0.21	25	0.09	26	0.11	27	0.06	22	0.33
24	0.10	2.85	19	0.06	21	0.14	76		73		72		25	0.32	26	0.09	23	0.21
25	0.10	2.85	23	0.09	24	0.32	73		72		69		28	0.14	29	0.07	26	0.21
26	0.05	1.60	22	0.06	23	0.11	24	0.09	25	0.32	28	0.17	29	0.15	30	0.09	27	0.33
27	0.05	1.72			22	0.08	23	0.06	26	0.33	29	0.16	30	0.15				
28	0.11	2.68	26	0.17	25	0.14	72		69		66		31	0.15	32	0.07	29	0.21
29	0.05	1.74	27	0.16	26	0.15	25	0.07	28	0.21	31	0.19	32	0.16	33	0.10	30	0.32
30	0.05	1.70			27	0.15	26	0.09	29	0.32	32	0.17	33	0.16				
31	0.10	2.68	29	0.19	28	0.15	69		66		63		34	0.15	35	0.08	32	0.21
32	0.05	1.76	30	0.17	29	0.16	28	0.07	31	0.21	34	0.19	35	0.17	36	0.10	33	0.31
33	0.05	1.70			30	0.16	29	0.10	32	0.31	35	0.19	36	0.17				
34	0.10	2.63	32	0.19	31	0.15	66		63		58		39	0.05	37	0.10	35	0.22
35	0.05	1.79	33	0.19	32	0.17	31	0.08	34	0.22	39	0.09	37	0.23	38	0.10	36	0.30
36	0.05	1.75			33	0.17	32	0.10	35	0.17	37	0.30	38	0.13				
37	0.05	1.76	36	0.30	35	0.17	34	0.10	39	0.18	42	0.06	40	0.17	41	0.10	38	0.21
38	0.11	2.60			36	0.13	35	0.10	37	0.21	40	0.19	41	0.12				
39	0.05	1.68	35	0.09	34	0. 05	63		58		55		42	0.11	40	0.33	37	0.18

Table 4. LFBGA 96-Ball Package Parameters (Balls 1 – 48) (Balls 49 – 96 Analog) (Continued)

Ball	Capacitance Ball to GND (pF)	Inductance Ball to Die (nH)	Ball Number and Coupling															
40	0.05	1.81	38	0.19	37	0.17	39	0.33	42	0.17	45	0.06	43	0.17	44	0.09	41	0.28
41	0.05	1.66			38	0.12	37	0.10	40	0.28	43	0. 18	44	0.15				
42	0.11	2.75	37	0.06	39	0.11	58		55		52		45	0.15	43	0.25	40	0.17
43	0.05	1.84	41	0.18	40	0.17	42	0.25	45	0.17	48	0.06	47	0.13	46	0.13	44	0.28
44	0.06	1.85			41	0.15	40	0.09	43	0.28	47	0.13	46	0.25				
45	0.11	2.83	40	0.06	42	0.15	55		52		49		48	0.16	47	0.16	43	0.17
46	0.06	1.75			44	0.25	43	0.13	47	0.28								
47	0.06	1.66	44	0.13	43	0.13	45	0.16	48	0.25							46	0.28
48	0.14	2.87	43	0.06	45	0.16	52		49									

Table 5 gives the maximum and minimum values of capacitance and inductance and the maximum value for the mutual coupling of two pins from Tables 1 through 4.

Table 5. Comparison of Capacitance, Inductance, and Coupling-Factor (k) Package Parameters

	Capacitance Pin to GND (pF)		Inductance Die to Pin (nH)	Coupling Factor (k) Pin to Pin (nH)
SSOP 48 pin	MAX	0.443	7.970	0.54
	MIN	0.074	5.080	
	DELTA	0.369	2.890	
TSSOP 48 pin	MAX	0.410	3.990	0.40
	MIN	0.077	2.370	
	DELTA	0.333	1.620	
TVSOP 48 pin	MAX	0.296	4.310	0.42
	MIN	0.048	2.380	
	DELTA	0.248	1.930	
LFBGA 96 ball	MAX	0.145	2.866	0.42
	MIN	0.046	1.597	
	DELTA	0.099	1.269	

The lower the parasitic parameters for a package are, the better the electrical quality of the package. In this comparison, the SSOP package showed the highest values for all parameters and the largest difference between maximum and minimum values. The SSOP maximum value is 180% higher than the value for the LFBGA 96-ball packages, and the difference between its maximum and minimum values is more than twice as great as for the LFBGA 96-ball package.

A comparison of the LFBGA 96-ball package with the dual in-line Widebus package types also demonstrates the superiority of the ball grid array package over the dual in-line Widebus package. The effects of lead inductance are examined in greater detail in the *Electrical Characteristics* section.

Electrical Characteristics

If one or more outputs switch, current flowing through the output lines leads to voltage drops, particularly to the inductance (L_P) of the lines of the supply voltage (V_{CC}) and GND. This voltage drop (U_{LP}) can be calculated using equation 2:

$$U_{Lp} = -Lp \frac{\Delta i}{\Delta t} \qquad (2)$$

U_{Lp} is superimposed within the circuit on the supply-voltage pins and ground pins and also is directly superimposed on the potential of the outputs, which do not switch. Because the amplitude of the interference is dependent on the current, it increases with increasing numbers of simultaneously switching outputs. Simultaneous switching interference is interference caused by the simultaneous switching of several outputs. There are various methods of reducing the amplitude of the interference.

First, the output current [Δi in equation (2)], i.e., the current drive capability, which influences the amplitude of the interference, can be limited. However, this solution is not applicable in many packages because a large current is needed to drive low-impedance lines.

The second option is to reduce the slew rate at the start of switching, or, in other words, to increase the switching duration (Δt) in equation 2.

However, because the propagation delay time is measured at the threshold voltage, which is one-half the supply voltage with CMOS or 1.5 V with bipolar technology, the propagation delay time increases proportionately with a steeper output signal edge. Therefore, this solution also is of very limited use.

To reduce signal slew-rate (see Figure 3), TI uses a switching technique known as Output Edge Control (OEC™) in the output stages of modern logic circuits (see Figure 4).

OEC is a trademark of Texas Instruments Incorporated.

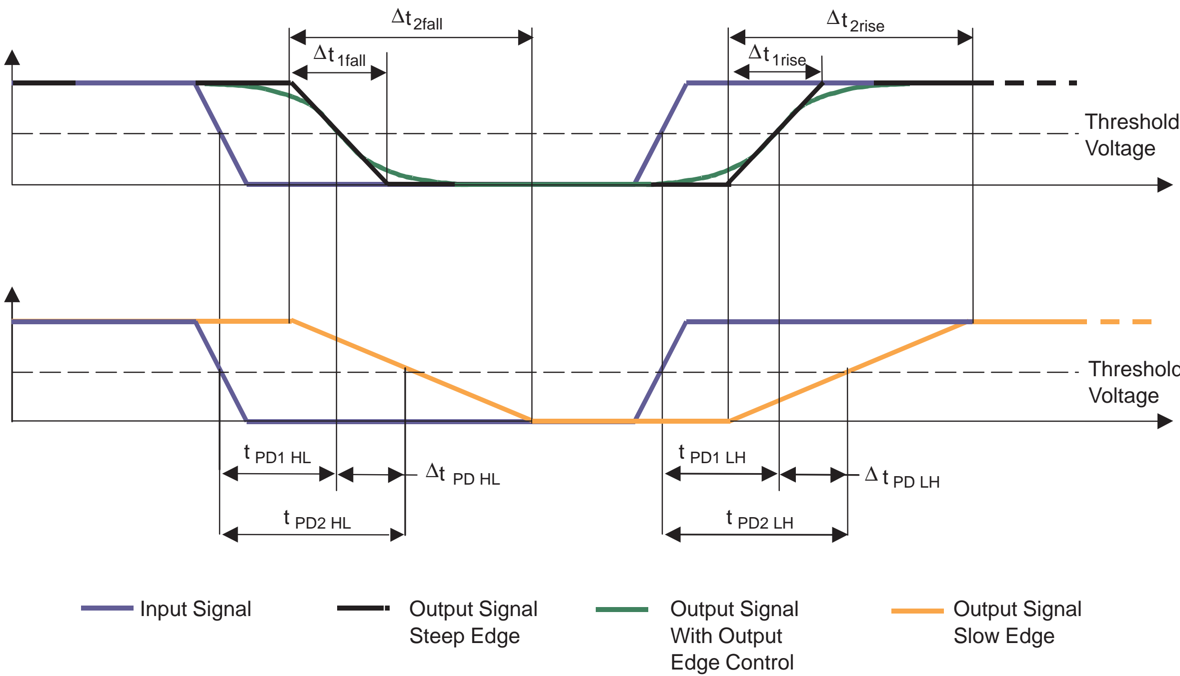


Figure 3. Influence of Slew Rate on Propagation Delay Time and the Principle Behind OEC

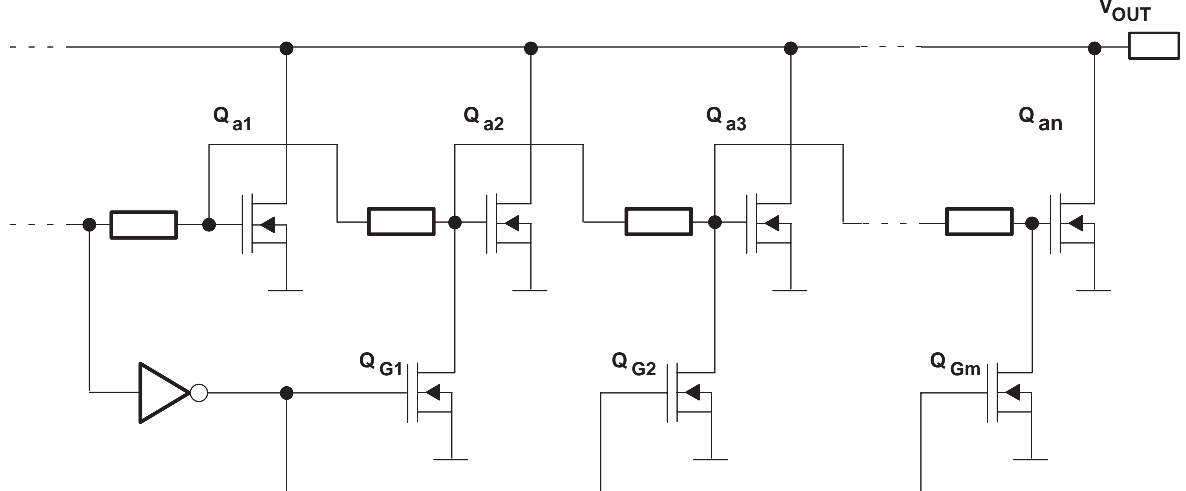


Figure 4. Basic Structure of the OEC Output Stage

The output stage, as a whole, is divided into several mini-output stages whose drain and source connections are each switched in parallel. The gates of these transistors are triggered in a delayed fashion. The resistance of these transistors before the gates, together with the input capacitance of the transistors (Miller capacitance), creates a signal delay line. When a signal is applied to this arrangement, the whole transistor does not switch on at once, rather the individual part transistors conduct one after the other. Thus, the closing of the circuit is delayed so that, on output, there is a transition rise time or fall time of about 2 ns. When switching off, the gates of the output transistors are switched off without delay via transistors Q_{G1} to Q_{Gm} to limit the current spikes occurring when switching from push-pull output stages. However, any further delaying of edges by this method is not possible.

The measures cited thus far are not sufficient to adequately damp the interference mentioned above. Accordingly, the inductance of the supply-voltage lead (L_P) must be reduced. The distance of the silicon from the pin connections and, therefore, the inductance, is determined decisively by the length of the lead. Therefore, the best solution is to reduce the size of the package as much as possible. In the case of modern logic circuits, with a propagation delay time of less than 6 ns, a reduction of the inductance in the supply leads results in an increase in speed because the braking effect of lead inductance is reduced.

In Widebus packages, additional grounding and supply connections are inserted along the whole width of the circuit, an arrangement known as staggered pinout. This does increase the number of pins, but the main advantage is that the interference voltages that can arise due to crosstalk between two neighboring connections are significantly reduced. Additionally, this distribution of supply connections results in a significant reduction in lead inductance.

Simultaneous-Switching Behavior

Figure 5 shows the simultaneous-switching measurement setup and the position of the outputs examined.

Figure 5. Simultaneous-Switching Measurement Setup

For this measurement procedure, one input is connected to a fixed low (L) state, or high (H) state, while all other inputs are switched simultaneously. The outputs of the connecting driver react to the changes in the various inputs with a certain delay, while the nonswitched output should maintain a constant low state (or high state).

However, three factors lead to a reaction by the nonconnected input:

- Crosstalk between neighboring pins
- A brief notch in the supply voltage, not measurable from outside, caused by the inductance of the V_{CC} lead
- A brief increase in the grounding level, not measurable from outside, caused by the ground lead

The worst case possible for the measurement procedure is when the distance to the GND and supply pins is greatest. Accordingly, for the Widebus package, measurements are made at pin 37 (2A2) and for the LFBGA at ball 23 (4A4).

Figure 6 sets out the parameters and definitions of significance for this measurement procedure. Points on the curves are defined as:

V_{OHP} (voltage output high peak): High bounce: peak output-voltage value during a static high at the nonswitched output

V_{OHV} (voltage output high valley): High bounce: minimum output-voltage value during a static high at the nonswitched output

V_{OLP} (voltage output low peak): Ground bounce: peak output-voltage value during a static low at the nonswitched output

V_{OLV} (voltage output low valley): Ground bounce: minimum output-voltage value during a static low at the nonswitched output

The critical parameters are V_{OLP} and V_{OHV} because, in the worst case, they could exceed the switching thresholds V_{IH} and V_{IL}.

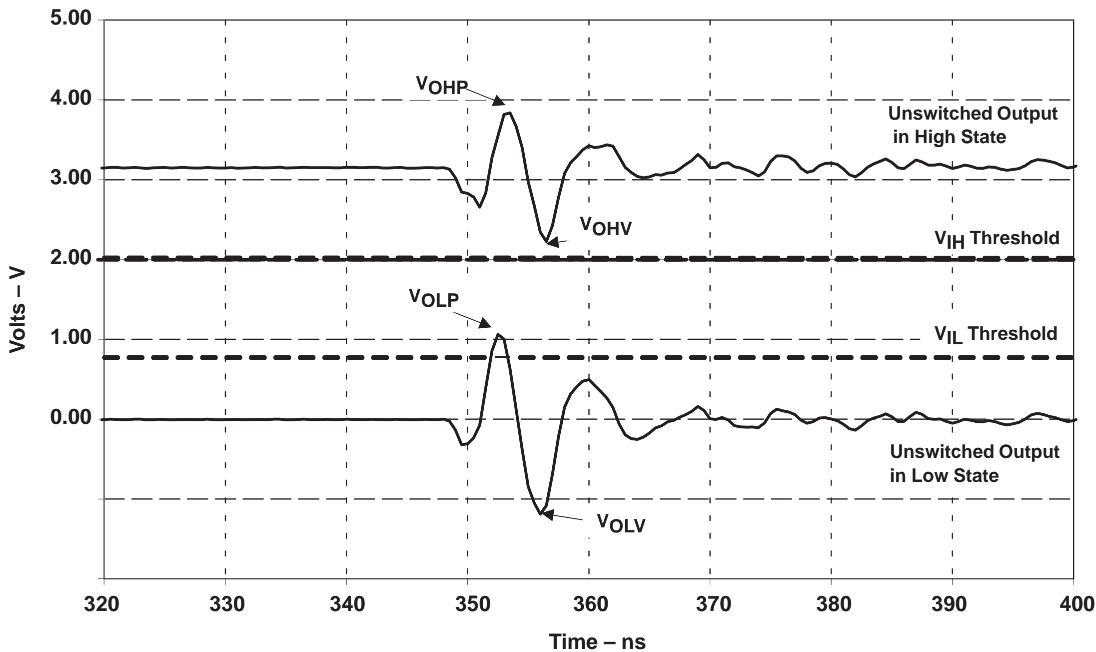


Figure 6. Simultaneous-Switching Parameter

The ground- and high-bounce measurements for the simultaneous switching of several outputs are given in Figures 7 through 14 for the package types investigated in this report.

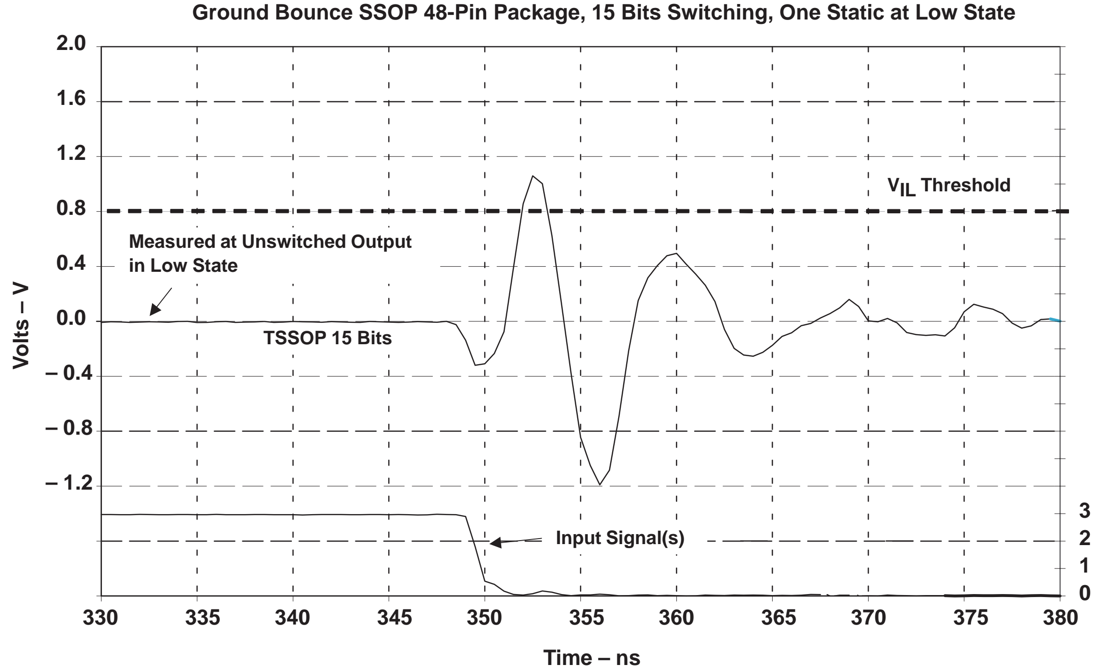


Figure 7. Measured Simultaneous-Switching Ground Bounce, SSOP 48-Pin Package

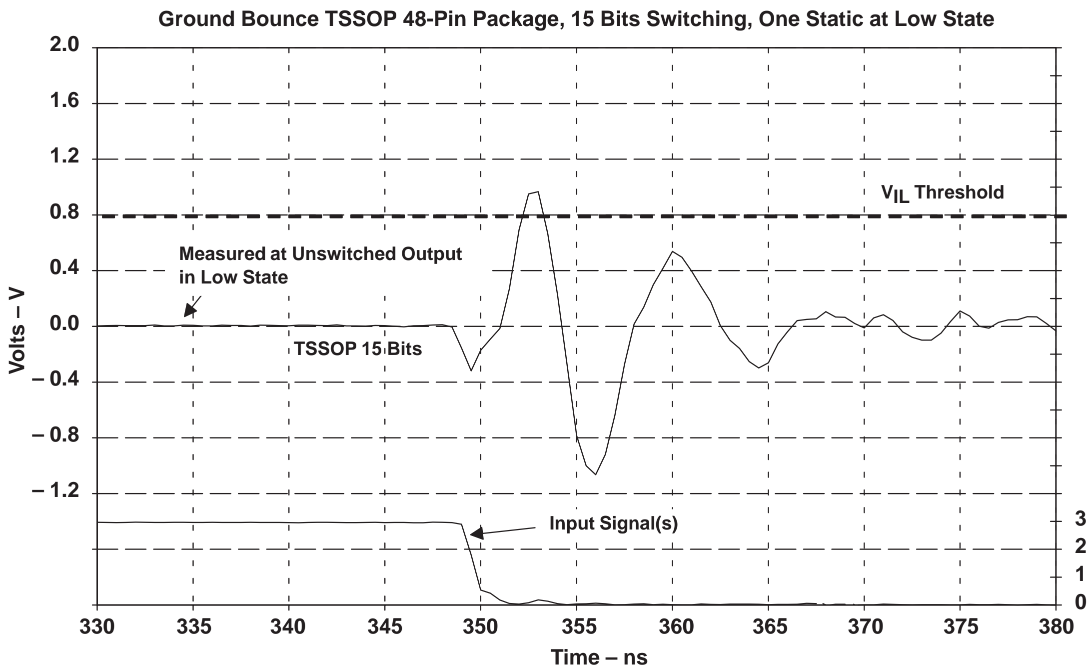


Figure 8. Measured Simultaneous-Switching Ground Bounce, TSSOP 48-Pin Package

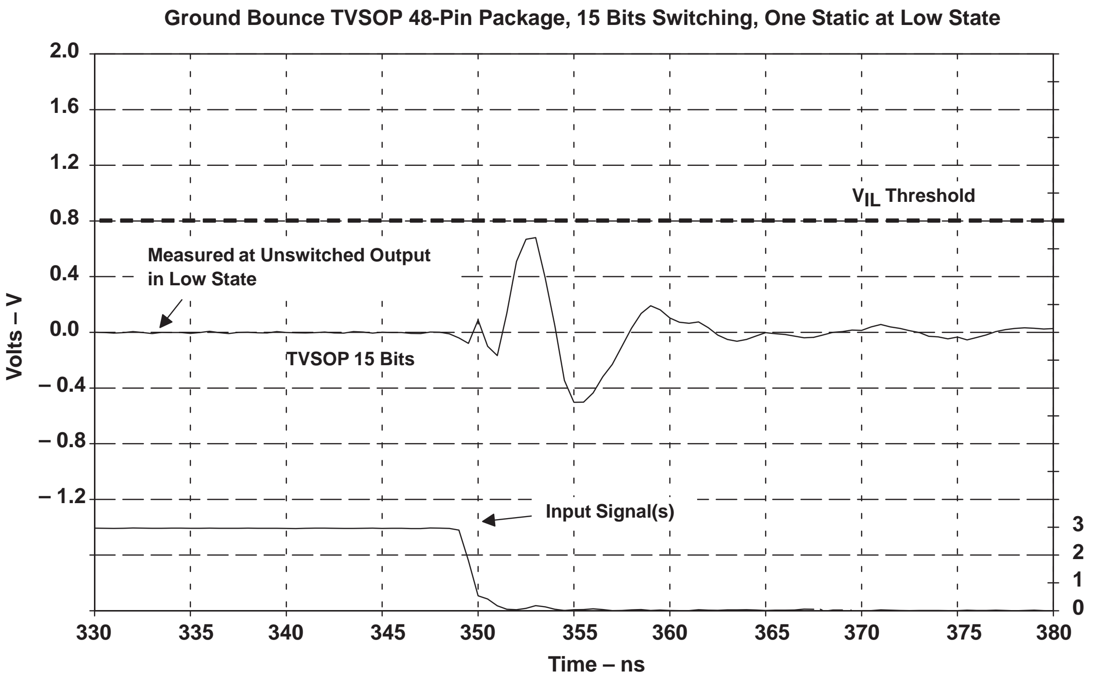


Figure 9. Measured Simultaneous-Switching Ground Bounce, TVSOP 48-Pin Package

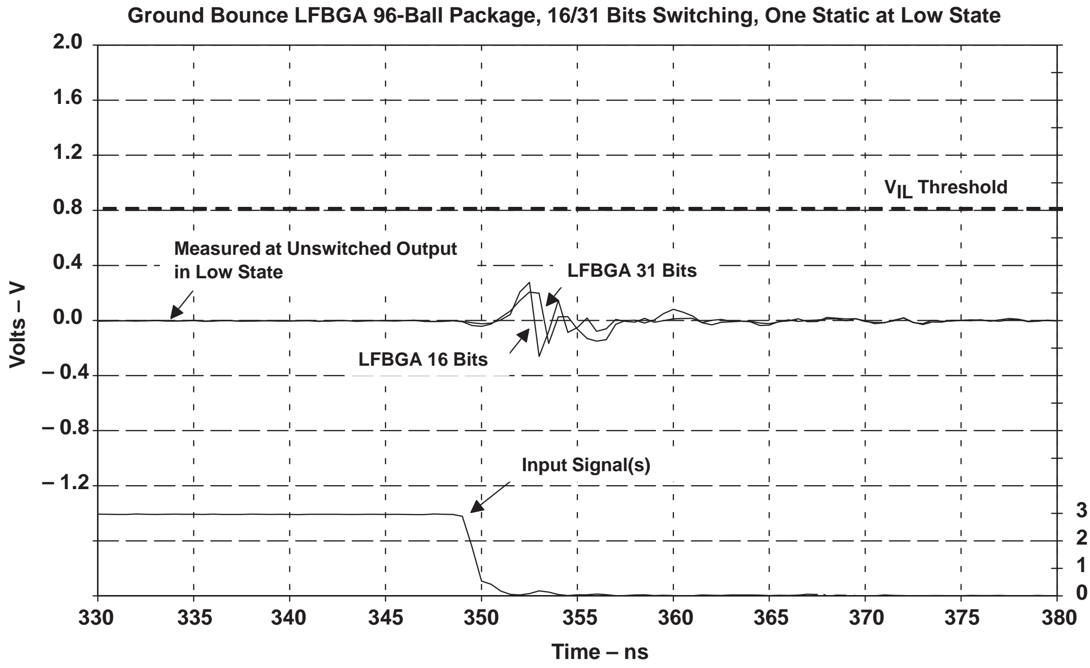


Figure 10. Measured Simultaneous-Switching Ground Bounce, LFBGA 96 Ball

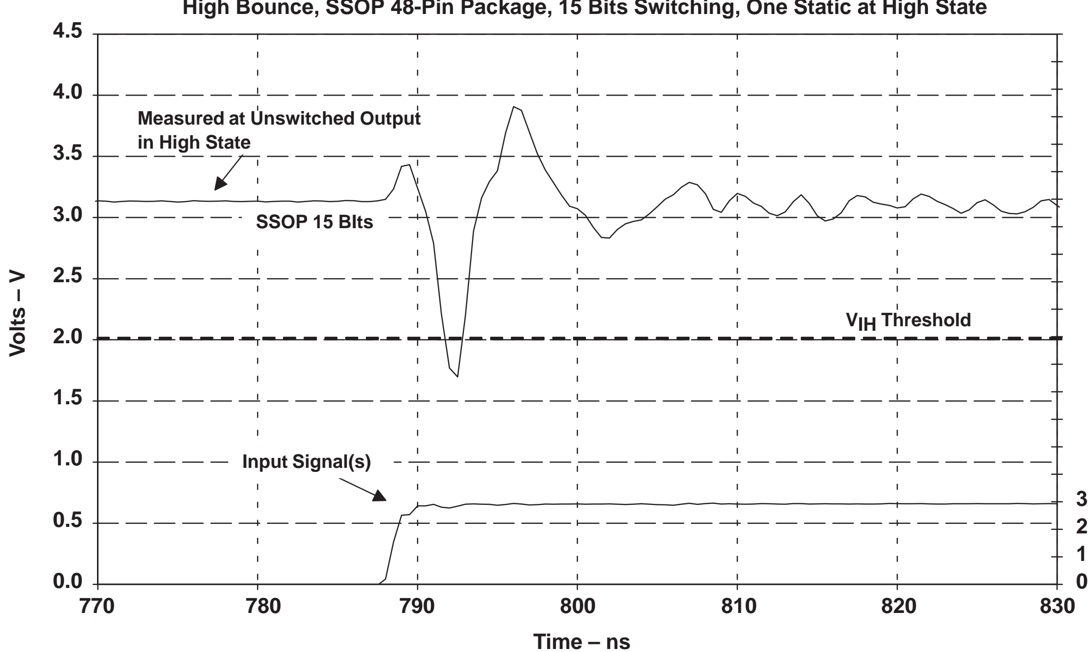


Figure 11. Measured Simultaneous-Switching High Bounce, SSOP 48-Pin Package

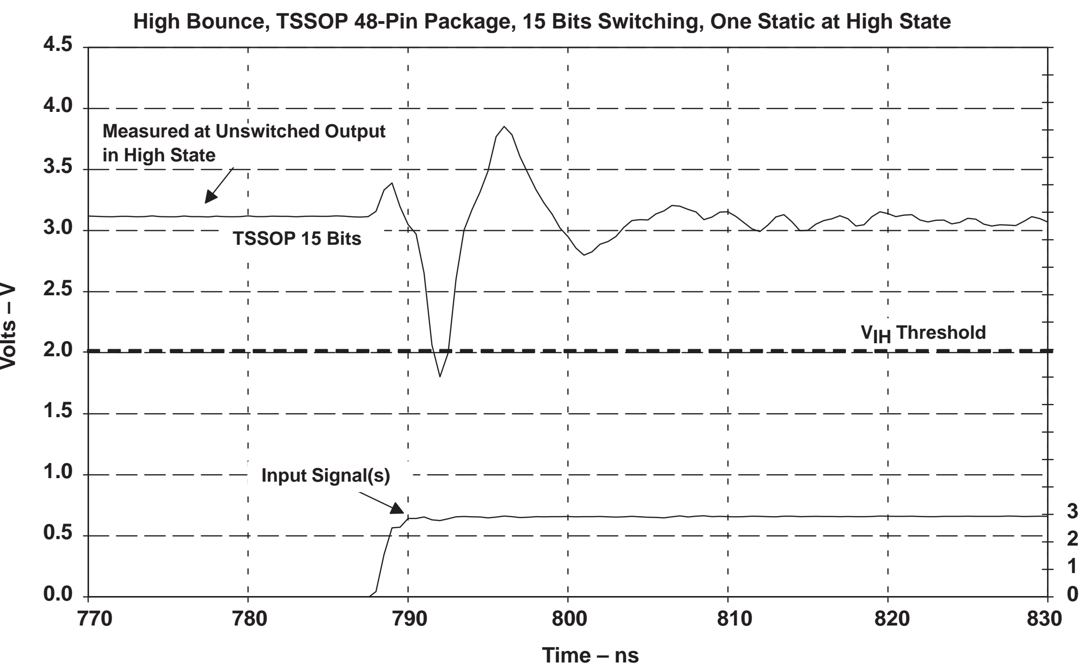


Figure 12. Measured Simultaneous-Switching High Bounce, TSSOP 48-Pin Package

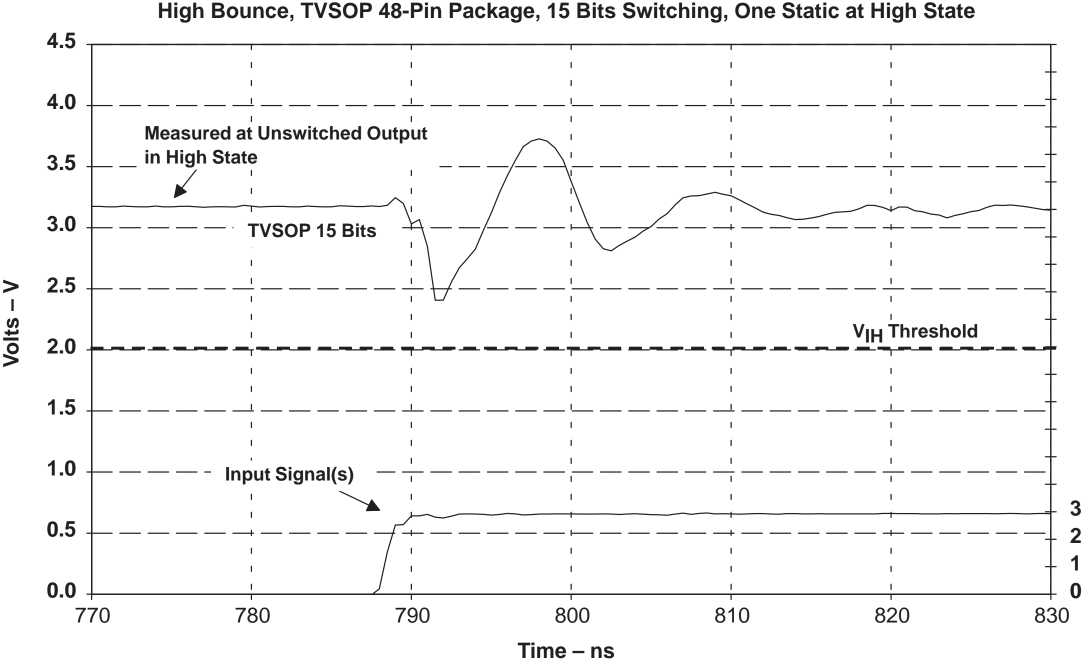


Figure 13. Measured Simultaneous-Switching High Bounce, TVSOP 48-Pin Package

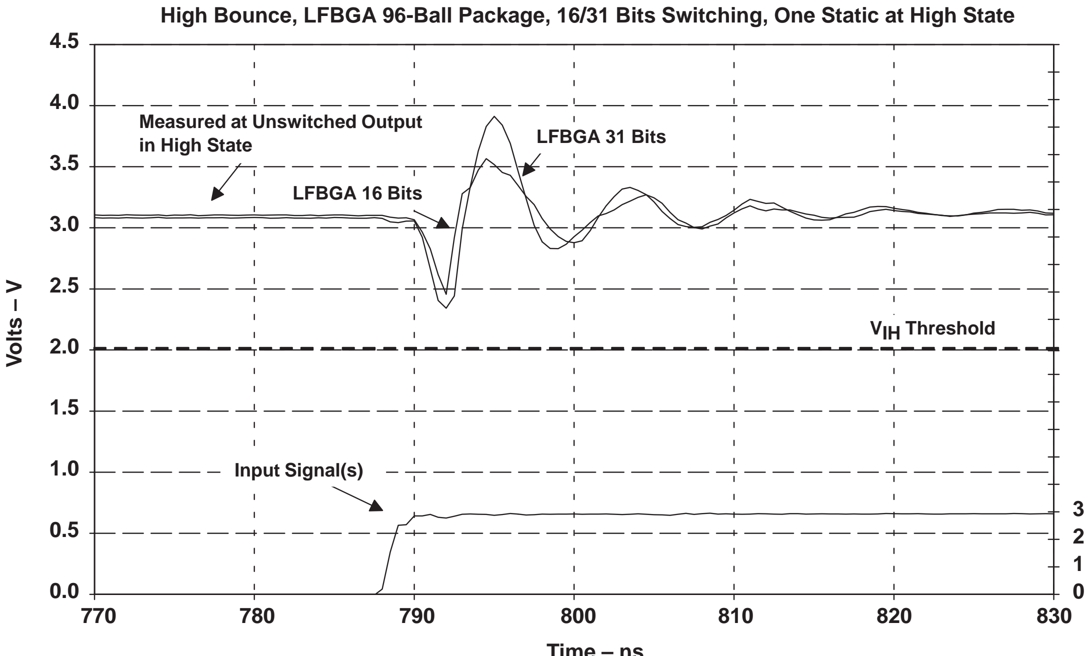
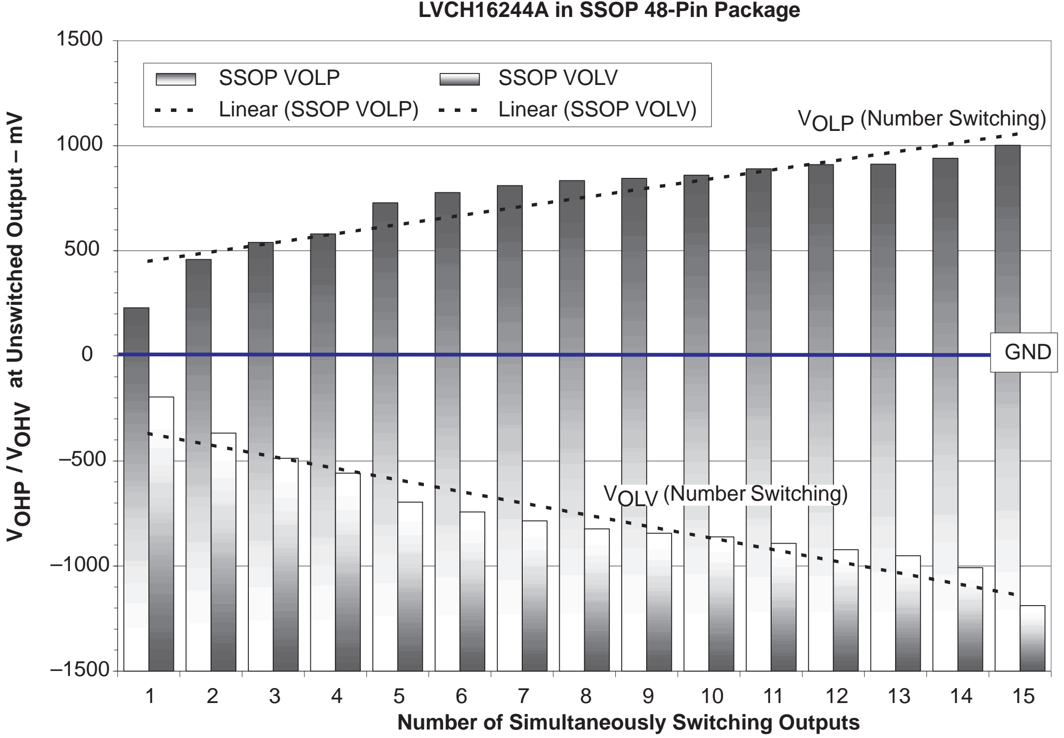


Figure 14. Measured Simultaneous-Switching High Bounce, LFBGA 96 Ball

The results shown in Figures 7 through 14 examine only the case in which all outputs but one are connected. It is also of interest to know the relationship between the number of simultaneously switching outputs and the level of interference. These results are shown in Figures 15 through 18. The dotted lines show the linearized increase in the ground/high bounce relative to the number of connected outputs.



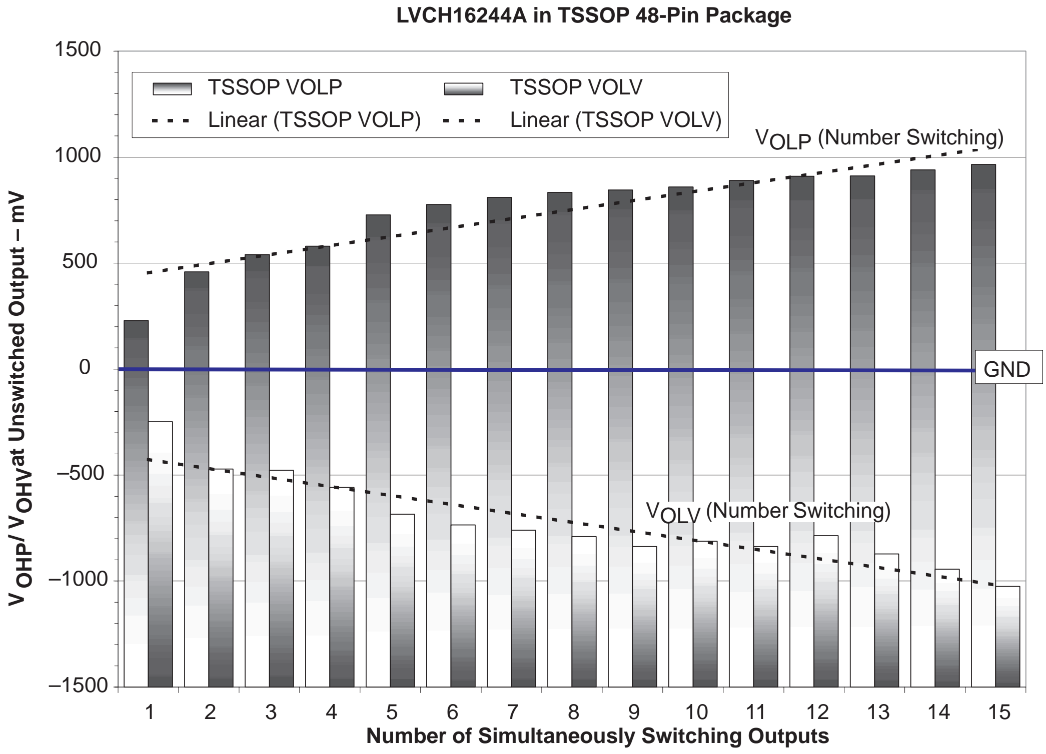
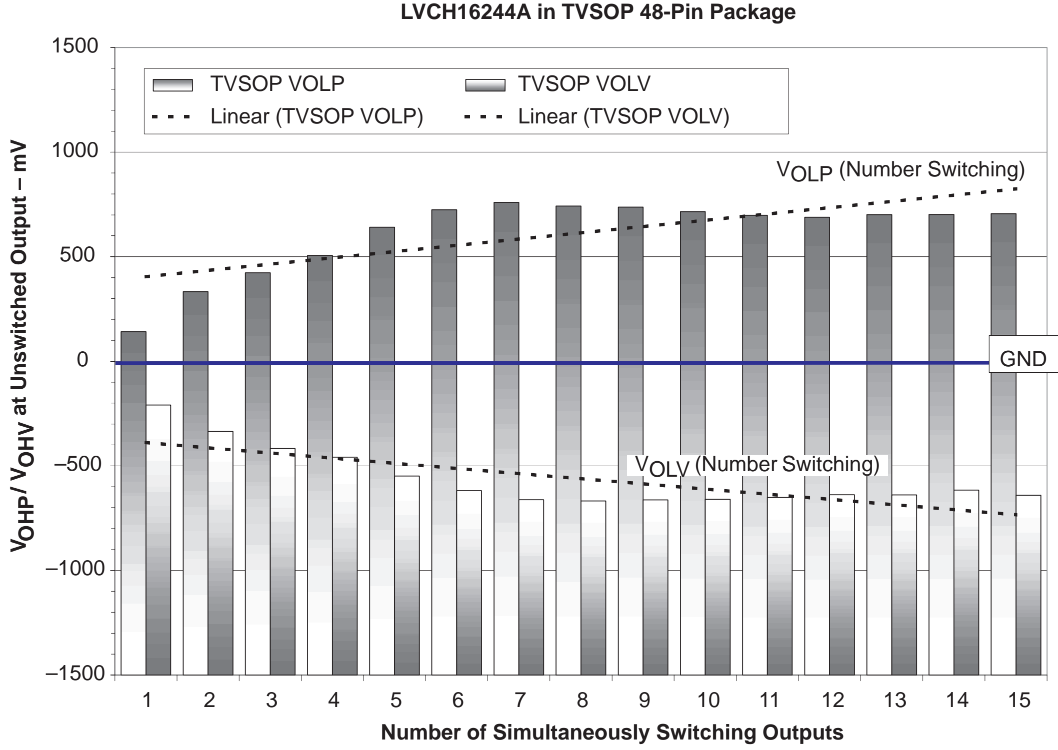


Figure 15. Simultaneous-Switching Ground Bounce, SSOP 48 Pin (top), TSSOP 48 Pin (bottom)



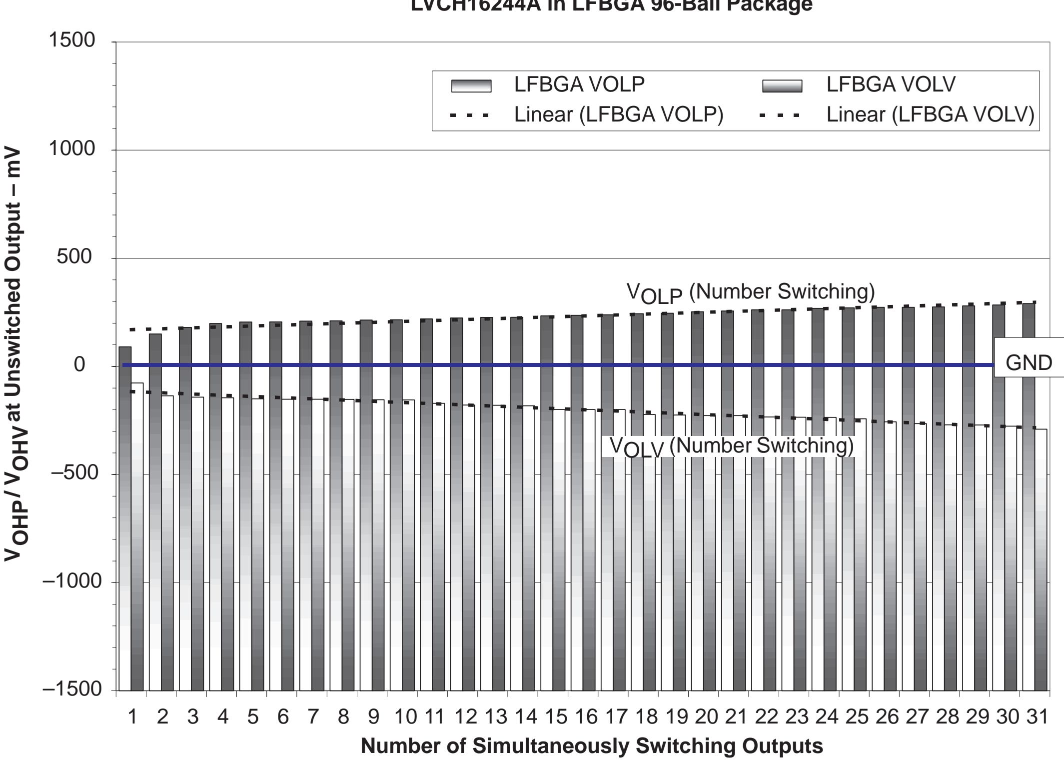
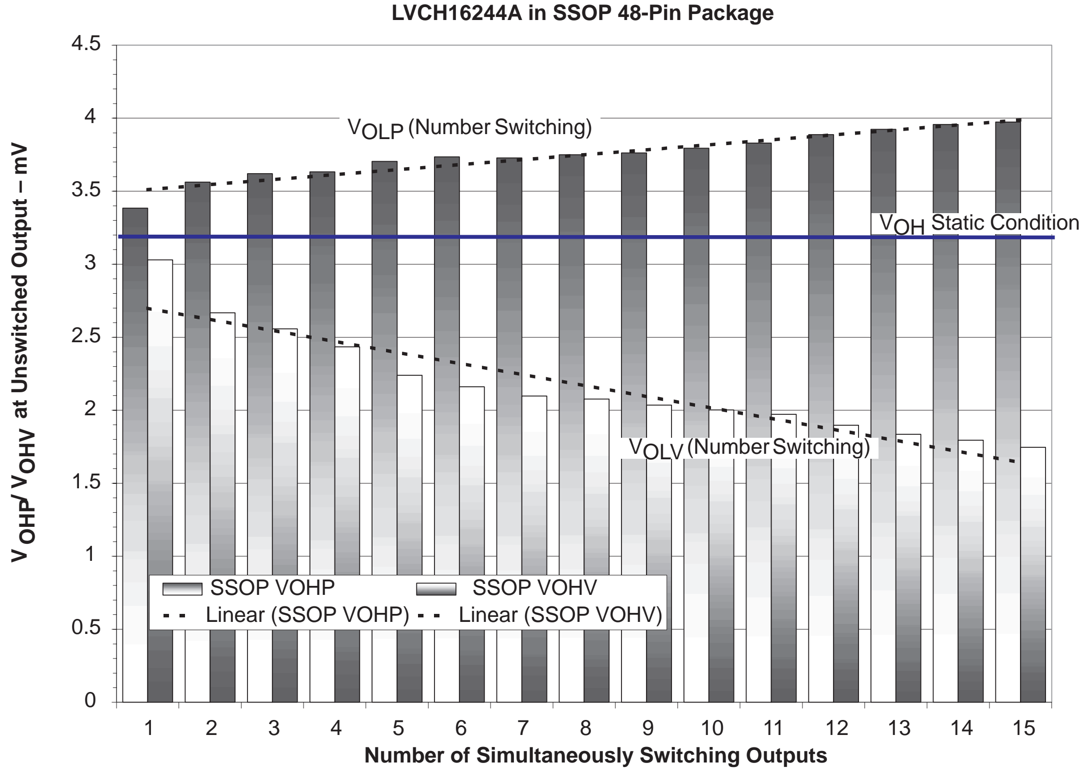


Figure 16. Simultaneous-Switching Ground Bounce, TVSOP 48 Pin (top), LFBGA 96 Ball (bottom)



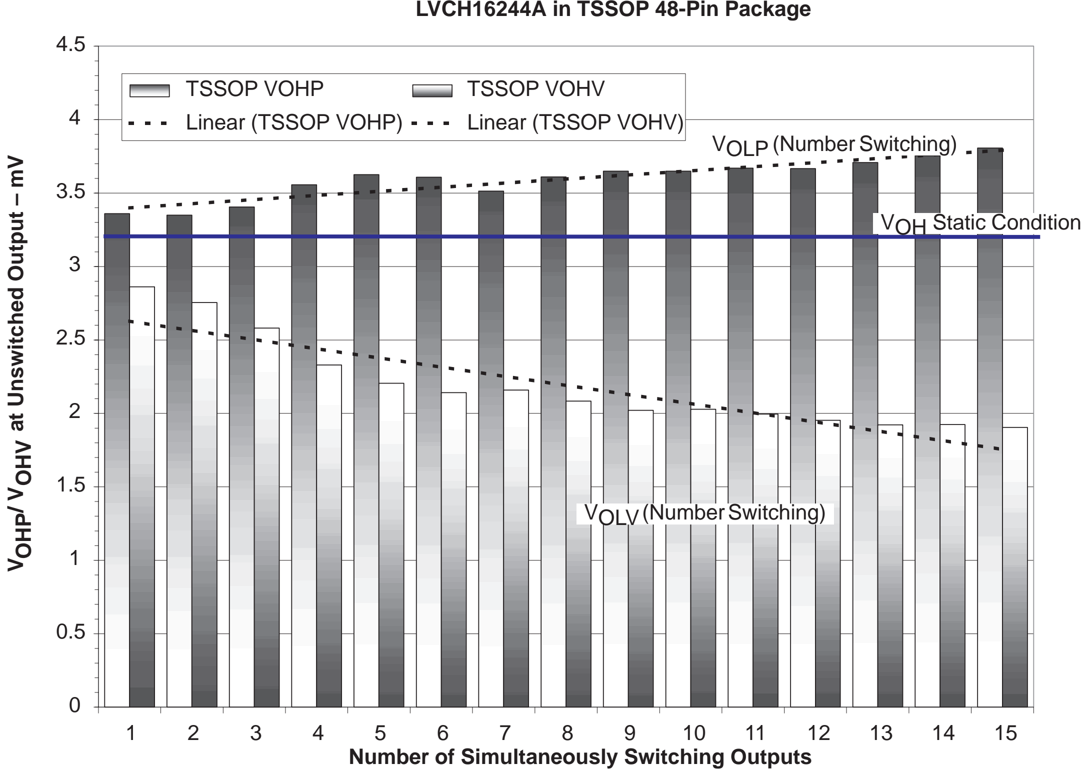
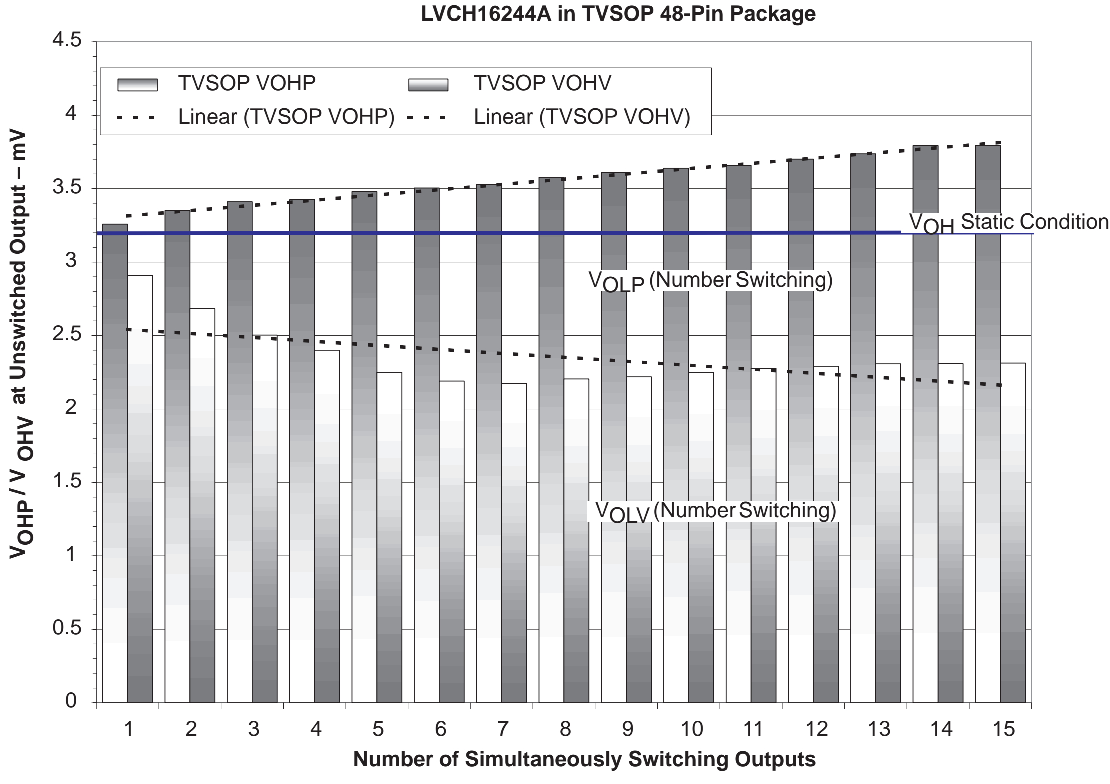


Figure 17. Simultaneous-Switching Ground Bounce, SSOP 48 Pin (top), TSSOP 48 Pin (bottom)



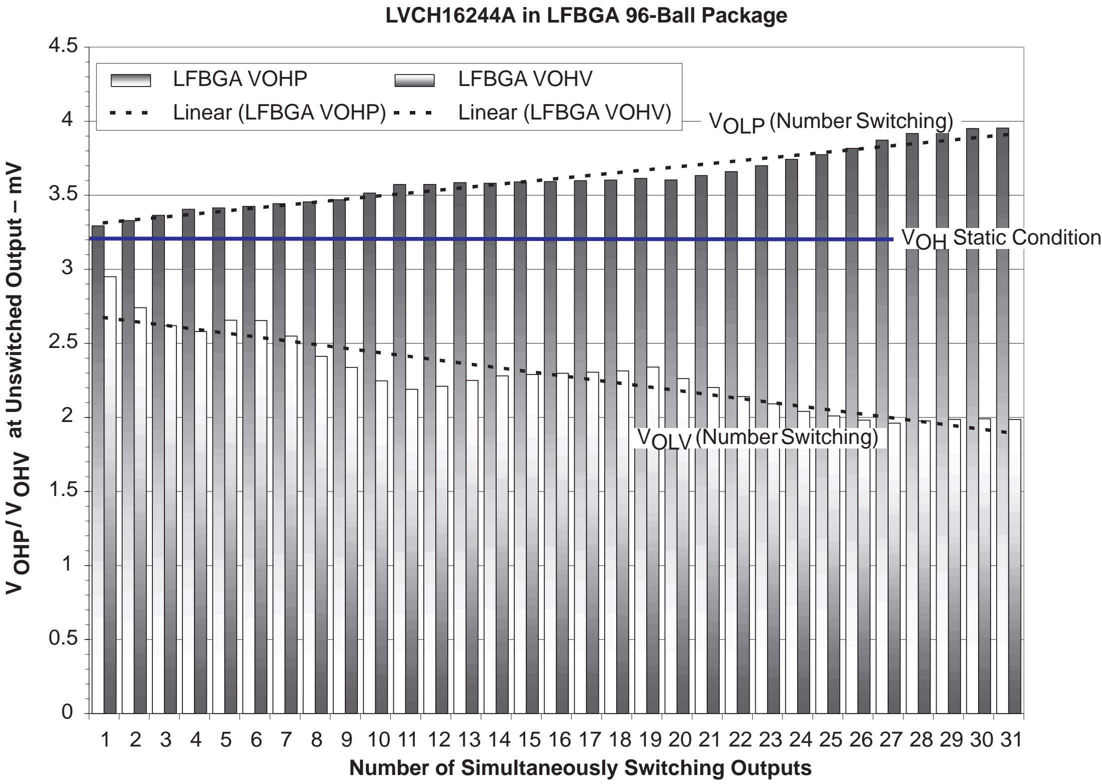


Figure 18. Simultaneous-Switching High Bounce, TVSOP 48-Pin (top), LFBGA 96 Ball (bottom)

The ground- and high-bounce interference voltages produced by simultaneous switching must not exceed the threshold voltage range for the subsequent input stage (1.4 V to 1.5 V). All the package types investigated meet this requirement for the investigated logic functions SN74LVCH16244A and SN74LVCH32244A. Although the components in the SSOP and TSSOP packages slightly exceed the input voltage threshold for the relevant logic states, switching of the subsequent stage is not expected because the typical threshold voltage of 1.5 V is not reached under any circumstances.

The best result obtained in this investigation was for the ball grid array package. The positive effect of the favorable ball arrangement with additional GND balls is evident.

A small part of the differences measured could be due to component spread rather than being exclusively the result of the package being measured.

The process technology involved also has a decisive effect on the interference level. However, the results here give an idea of the general tendencies that apply to other logic families as well.

Increase in Propagation Delay Time

The package type also influences the increase in propagation delay that occurs when several outputs switch simultaneously. The inductance of the supply and ground leads is the decisive factor. To measure this behavior for various packages, the relation between propagation delay and the number of outputs switching was measured. (see Figures 19 and 20). In all cases, the devices measured were from the LVC family operated at a supply voltage of 3.3 V and whose outputs were, in accordance with the data sheet, loaded with 30 pF and 500 Ω: SN74LVCH16244A for the Widebus package and SN74LVCH32244A for the LFBGA 96-pin package.

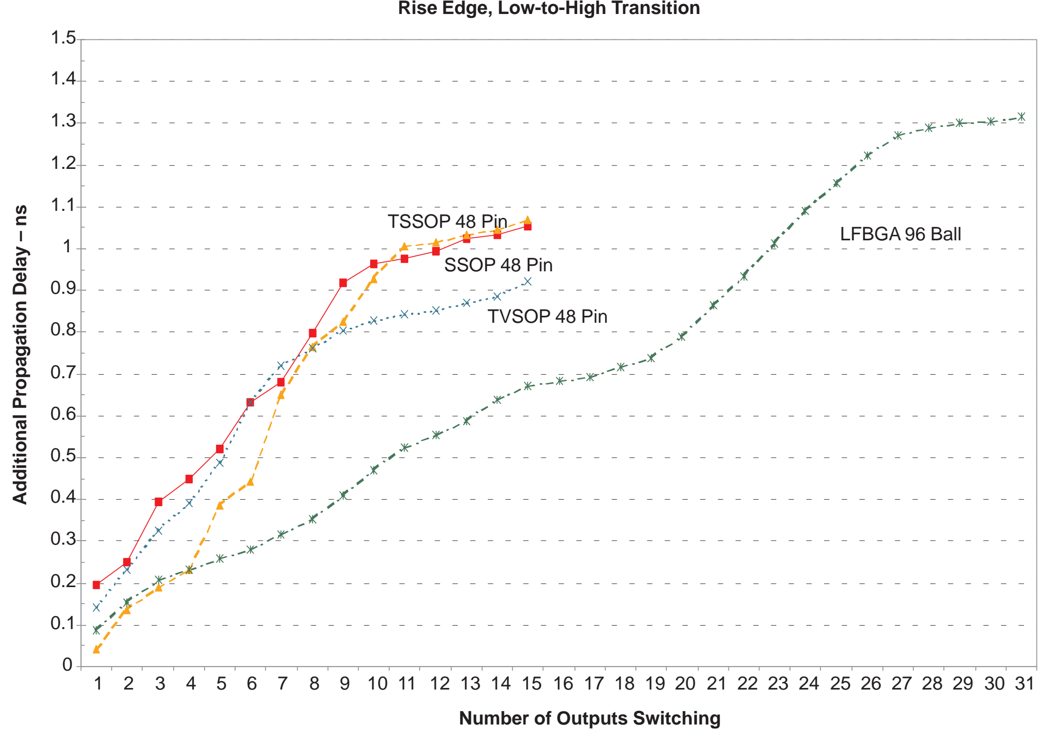


Figure 19. Rising-Edge Propagation Delay Time Relative to the Number of Simultaneously Switching Outputs for the SSOP, TSSOP, TVSOP, and LFBGA Packages

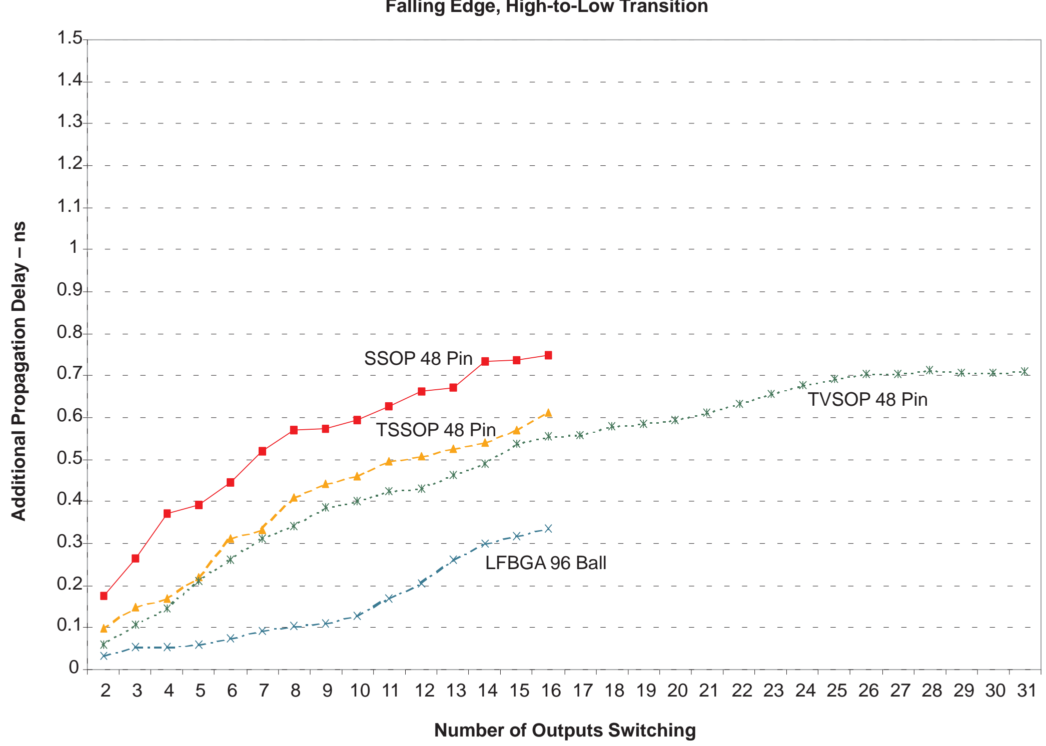


Figure 20. Falling-Edge Propagation Delay Time Relative to the Number of Simultaneously Switching Outputs for the SSOP, TSSOP, TVSOP, and LFBGA Packages

In Figures 19 and 20, the Y-axis shows the increase in propagation delay time and the X-axis shows the number of outputs switching. The representation of the increase in propagation delay time was selected in order to eliminate fluctuations in absolute switching speed that occur as a result of variations in component tolerances. Because the absolute increase in propagation delay time for the rising edges is 0.3 ns to 0.8 ns (for the falling edge, 0.9 ns to 1.3 ns), the measurements are at the upper limits of achievable measurement accuracy, the given measurement setup, and the measuring instruments used. This is the reason for the nonlinearities of the data curves.

The SSOP package produced the worst results for all tests, while the TVSOP 48-pin gave the best values for a Widebus package.

Again, the LFBGA package performed well.

Thermal Properties

When developing a digital system, the thermal behavior of the package must be taken into account.

The small size of surface-mounted devices means that the dissipation of the heat arising from power loss becomes increasingly critical as components become smaller.

The thermal resistance of packages relative to airflow is given in Table 6. The maximum power consumption curves in relation to the ambient temperature for the package types investigated in this report are given in Figures 21 through 24.

Table 6. Comparison of the Thermal Resistance ($R_{\theta JA}$) of Different Packages

Package	Thermal Resistance at Various Airflows			
	0 m/s	0.83 m/s	1.38 m/s	2.78 m/s
SSOP 48 pin	93.5	69.9	63.8	57.1
TSSOP 48 pin	89.1	78.5	75.1	69.4
TVSOP 48 pin	92.9	80.9	77.1	71
LFBGA 96 ball	40	37.5	37	35.7

In equation 3, the chip temperature is derived from the thermal resistance, the component's overall power loss, and the ambient temperature.

$$T_J = R_{QJA} \times P_{TOT} + T_A \quad (3)$$

Where:

T_J = chip temperature (J = junction)
R_{QJA} = thermal resistance of the chip (junction) at the ambient air temperature
P_{TOT} = component's overall power loss
T_A = ambient temperature

The total power consumption (P_{TOT}) of a circuit is determined mainly by:

- Circuit standby power consumption (P_{Stat})
- Power consumption (P_S) caused by the current spike that occurs when switching an output
- Power consumption (P_L) necessary for the transition from one logic state to the other of the capacitive load connected at the output.

The equation for calculating P_{TOT} is:

$$P_{TOT} = P_{Stat} + P_S + P_L \quad (4)$$

Where:

P_{Stat} = static power consumption
P_S = dynamic power consumption caused by current spikes
P_L = dynamic power consumption caused by capacitance load

The static share (P_{Stat}) of the power consumption, which is caused by the component itself, can be calculated from the parameters I_{CCL}, I_{CCH}, and I_{CCZ}, given in the specification sheet, the supply voltage, and the relationship of active high, low, and high impedance. Equation 6 gives the amount of static power consumption. However, this power consumption does not depend on the number of switched outputs, but on the share of the signal.

The dynamic share of the power consumption depends on the factor’s line impedance and length; the output load of the input and output rates; the duty cycle from active high, low, and high impedance; and the amplitude and duration of current peaks at the moment of switching. The definition of share is given in equation 5:

$$share_{high(low;\ Z)} = \frac{T_{high(low;\ Z)}}{T_{high} + T_{low} + T_{Z}} \tag{5}$$

Where:

$T_{high,low,Z}$ = average amount of time within a signal period

$$P_{Stat} = \sum_{k=1}^{n} \frac{V_{CC(share(k)high} \times I_{CCH} + share_{low}(k) \times I_{CCL} + share_{Z}(k) \times I_{CCZ})}{n} \tag{6}$$

Where:

V_{CC}	=	supply voltage
I_{CCL}, $share_{low}(k)$	=	current consumption for static low at output, average percentage share of the kth output
I_{CCH}, $share_{high}(k)$	=	current consumption for static high at output, average percentage share of the kth output
I_{CCZ}, $share_{Z}(k)$	=	current consumption for high-impedance state at output, average percentage share of the kth output
k	=	number of the switched output of the circuit
n	=	number of inputs in the circuit

The power consumption caused by the current spikes can be calculated using equation 7:

$$P_{S} = \sum_{k=1}^{n} V_{CC} \times I_{S} \times t_{S} \times f \times k \tag{7}$$

Where:

I_S	=	amplitude of current spikes
t_S	=	duration of current spikes
f	=	clock rate (repetition rate)
k	=	number of the switched outputs of the circuit
n	=	number of switched outputs

The technology involved is a major factor in the amplitude of current spikes. With bipolar output stages, the amplitude of current spikes is less. They are more clearly revealed by the rising signal edges.

Power consumption (P_L) is caused by external loads at the outputs of the circuit. This power is taken up by the circuit for the transition from one logic state to the other, and can be calculated by equation 8:

$$P_L = \sum_{k=1}^{n} V_{CC} \frac{V_{swing} \times C_L(k) \times f(k)}{2} \tag{8}$$

Where:

C_L (k) = capacitive load connected to the kth output
V_{swing} = signal swing $V_{OH} - V_{OL}$
f(k) = frequency applied to the kth input

In addition to the power consumption shares mentioned above, additional power consumption can result from bus conflicts. A bus conflict occurs when two drivers on a line simultaneously create different logic levels. This problem can be avoided when designing a circuit by using proper timing arrangements.

Power consumption and chip temperature can be calculated, using the LVTH16244A as an example.

The SN74LVTH16244A 16-bit driver, with V_{CC} = 3.6 V, runs at a clock speed of 33 MHz. All of the outputs are switched. The symmetrical driver output load in the static case is 1 MΩ. The overall capacitive load totals 90 pF per output. On average, each output delivers logical high, low, and high-impedance one-third of the time. The current spikes at the moment of switching reach values of 20 mA in the LVT family. The duration of the current spike is 5 ns, and there are no bus conflicts.

Because the assigned load conditions and frequency are the same for all inputs and outputs, equations 5 through 8 are simplified. The summation and the control variables n and k are eliminated from equation 6. The factor 16 is added in equations 7 and 8 to reflect 16 inputs and outputs.

On the basis of the data-sheet values for the supply current (I_{CC}) in the high, low, and high-impedance state, for the component SN74LVTH16244A:

- $I_{CCH/Z}$ = 190 µA (for V_{CC} = 3.6 V, I_O = 0, V_I = V_{CC} or GND, outputs high or high impedance)
- I_{CCL} = 5 mA (for V_{CC} = 3.6 V, I_O = 0, V_I = V_{CC} or GND, outputs low)

P_{Stat} is derived for one-third low, one-third high, and one-third high impedance of the driver as follows:

$$P_{Stat} = 3.6\ \text{V} \times \left(\frac{5\ \text{mA}}{3} + \frac{0.19\ \text{mA}}{3} + \frac{0.19\ \text{mA}}{3}\right) = 6.46\ \text{mW} \tag{9}$$

These values also give the dynamic share in accordance with equations 7 and 8, and result in equation 10.

$$P_{dyn} = 16 \times \left(P_s + P_L\right) \tag{10}$$

With the given values, equation 10 results in

$$P_{dyn} = 16 \times \left(3.6\ \text{V} \times 20\ \text{mA} \times 5\ \text{ns} \times 33\ \text{MHz} + 3.6\ \text{V}\ \frac{3.6\ \text{V} \times 90\ \text{pF} \times 33\ \text{MHz}}{2}\right) \tag{11}$$

$$= 0.19\ \text{W} + 0.308\ \text{W} = 0.498\ \text{W}$$

The overall result in this case is:

$$P_{TOT} = 6.46\ mW + 0.498\ W = \sim 0.5\ W \tag{12}$$

The temperature on the silicon can be determined from the thermal resistance (R_{QJA}) of the package, and the ambient temperature, with the aid of equation 3. R_{QJA} corresponds to the capacity to dissipate heat to the ambient environment. Four package options are available:

SSOP: R_{QJA} = 89°C/W

TSSOP: R_{QJA} = 93°C/W

TVSOP: R_{QJA} = 94°C/W

LFBGA: R_{QJA} = 40°C/W

The thermal resistance given in each case is without any additional cooling measures. For the packages investigated, the following chip temperatures (T_J) are derived at an ambient temperature of 25°C, and without additional cooling:

SSOP package: T_J = 89°C/W × 0.5 W + 25°C = 69.5°C

TSSOP package: T_J = 93°C/W × 0.5 W + 25°C = 71.5°C

TVSOP package: T_J = 94°C/W × 0.5 W + 25°C = 72.0°C

LFBGA 96 package: T_J = 40°C/W × 0.5 W + 25°C = 45.0°C

If the temperature rises further as a result of greater output loads, leading to chip temperatures in excess of 150°C, additional cooling devices or fans must be used to dissipate the excess heat.

Figures 21 through 24 show the characteristic curves for power consumption relative to ambient temperature. In all cases, an upper limit value for the chip temperature of 150°C is assumed. Airflow ranges from 0 m/s to 2.78 m/s. An airflow of 0 m/s relates to an application using no additional cooling measures, while 2.78 m/s is for a system application using a cooling fan.

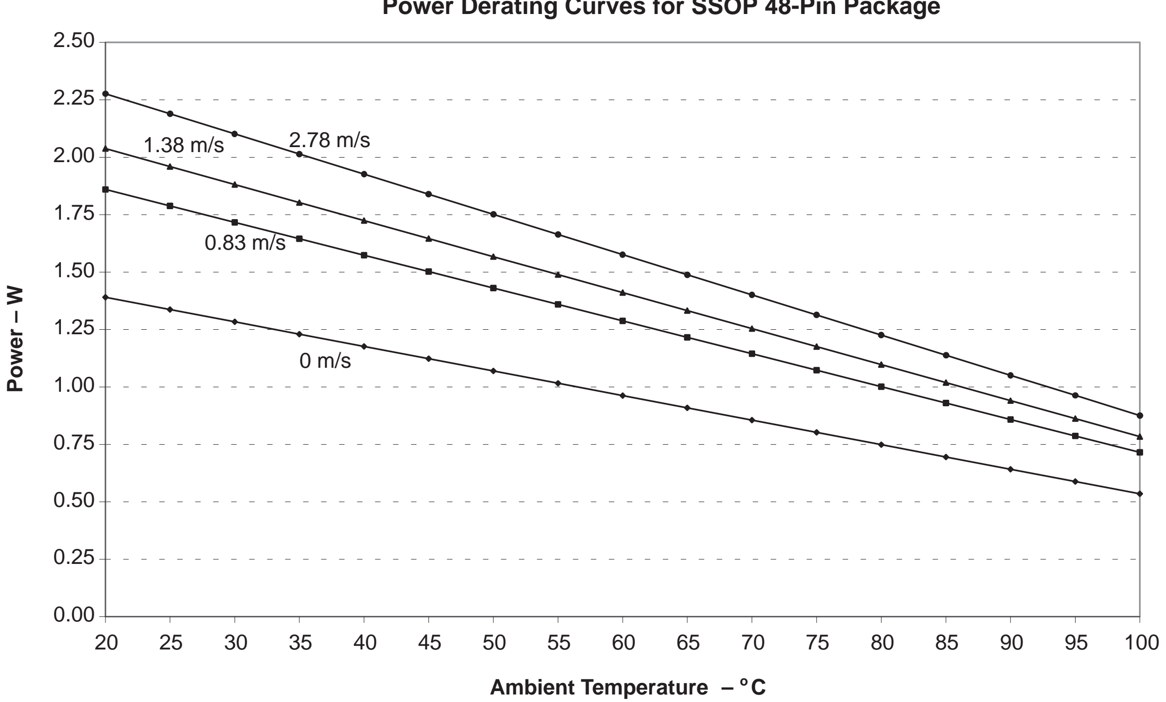


Figure 21. Maximum Power Consumption Relative to Ambient Temperature, T_J = 150°C, SSOP 48-Pin Package

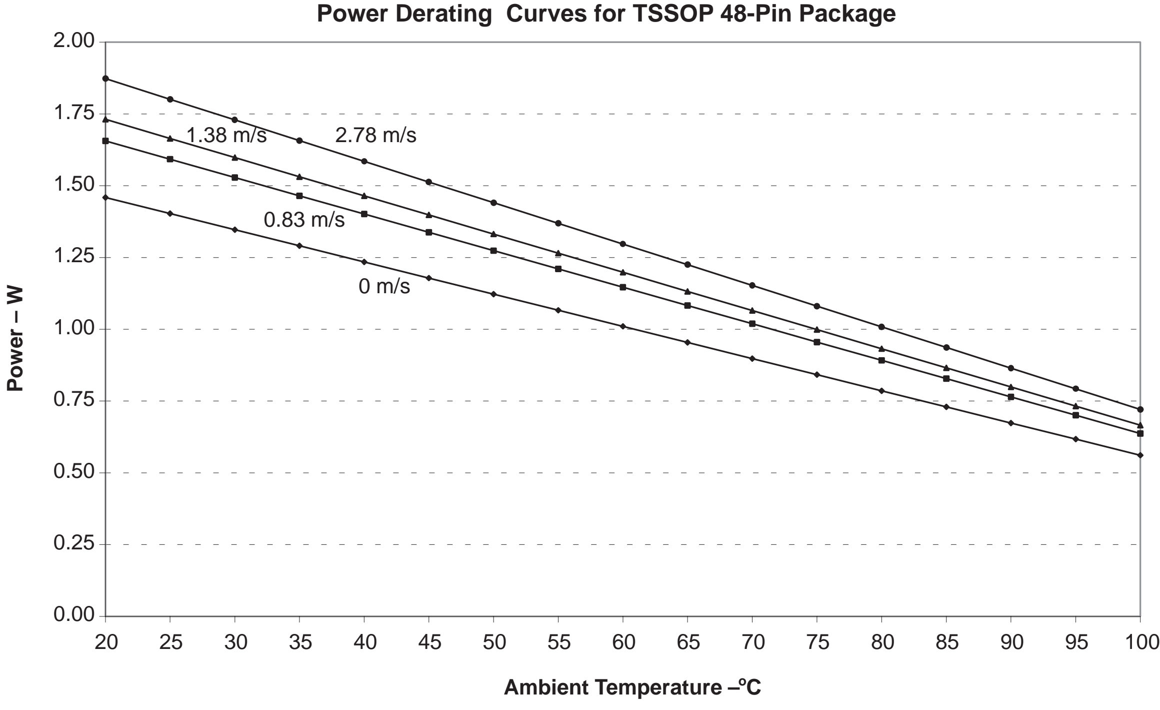


Figure 22. Maximum Power Consumption Relative to Ambient Temperature, T_J = 150°C, TSSOP 48-Pin Package

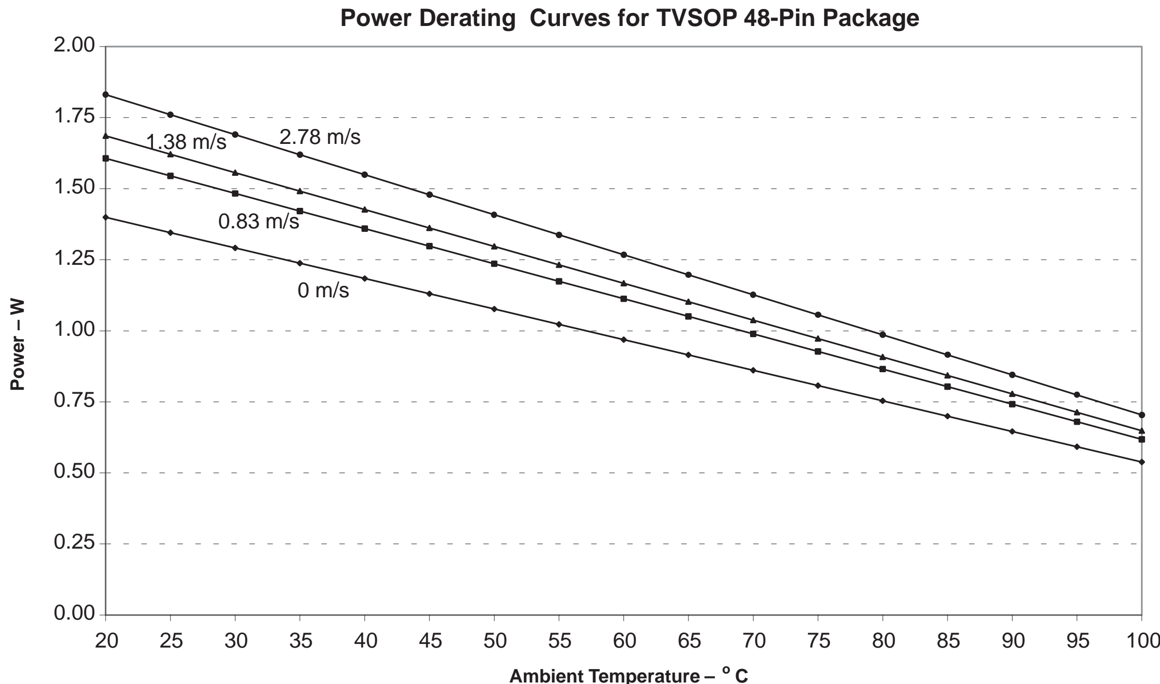


Figure 23. Maximum Power Consumption Relative to Ambient Temperature, T_J = 150°C, TVSOP 48-Pin Package

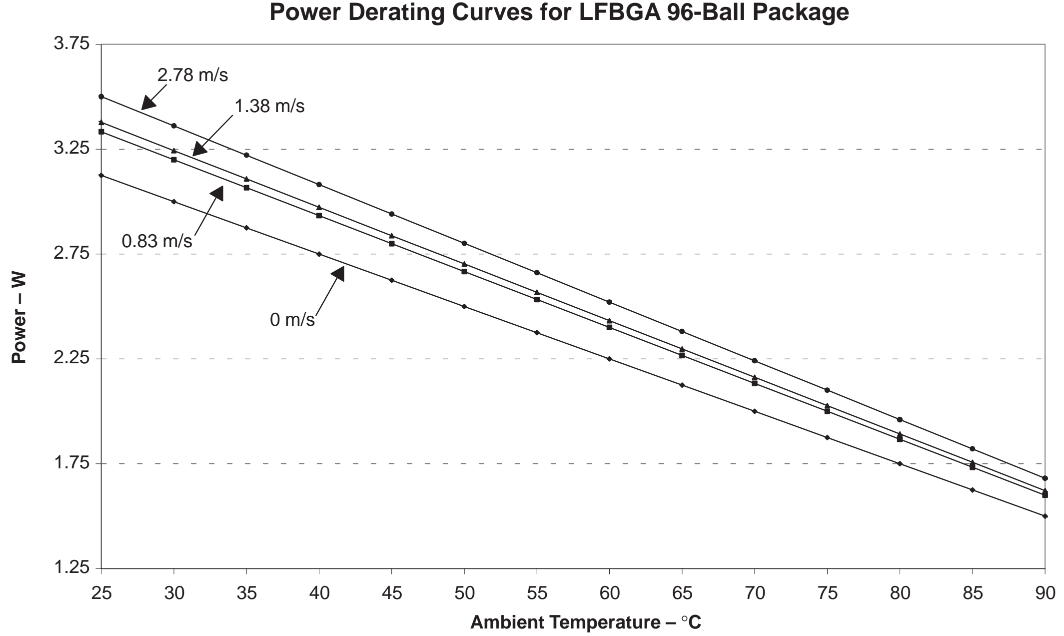


Figure 24. Maximum Power Consumption Relative to Ambient Temperature, T_J = 150°C, LFBGA 96 Ball

Although the LFBGA 96-pin package is the smallest, in this comparison it showed the lowest heat resistance. Table 6 shows that the LFBGA 96-pin package dissipates heat more effectively by a factor of more than two, compared to any of the other packages investigated. This leads to the added advantage that many systems do not require additional cooling provisions.

Package Dimensions and Size Comparison

Dimensions of the packages discussed in this report are provided in Figures 25 through 28.

DL (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN

0.025 (0,635)
0.012 (0,305)
0.008 (0,203)
0.005 (0,13) M
48
25
0.299 (7,59)
0.291 (7,39)
0.420 (10,67)
0.395 (10,03)
1
24
A
0.006 (0,15) NOM
Gage Plane
0.010 (0,25)
0°–8°
0.040 (1,02)
0.020 (0,51)
Seating Plane
0.004 (0,10)
0.110 (2,79) MAX
0.008 (0,20) MIN

DIM \ PINS **	28	48	56
A MAX	0.380 (9,65)	0.630 (16,00)	0.730 (18,54)
A MIN	0.370 (9,40)	0.620 (15,75)	0.720 (18,29)

4040048/D 08/97

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO-118

Figure 25. Dimensions of the SSOP 28-, 48-, and 56-Pin Packages

DGG (R-PDSO-G**) PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

4040078/F 12/97

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

Figure 26. Dimensions of the TSSOP 48-, 56-, and 64-Pin Packages

DGV (R-PDSO-G**) PLASTIC SMALL-OUTLINE PACKAGE

24 PINS SHOWN

PINS ** / DIM	14	16	20	24	48	56
A MAX	3,70	3,70	5,10	5,10	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	9,60	11,20

4073251/C 08/98

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

Figure 27. Dimensions of the TVSOP 48-, 56-, and 64-Pin Packages

GKE (R-PBGA-N96) PLASTIC BALL GRID ARRAY

5,60
5,40

13,60
13,40

4,00 TYP
0,80
0,40

T
R
P
N
M
L
K
J
H
G
F
E
D
C
B
A

1 2 3 4 5 6

0,80
0,40
12,00 TYP

0,95
0,85

1,40 MAX

Seating Plane

0,55
0,45

0,45
0,35

0,10

0,08 M

4188953/A 10/98

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar BGA™ configuration

Figure 28. Dimensions of the LFBGA 96-Ball Package

MicroStar BGA is a trademark of Texas Instruments Incorporated.

Figure 29 shows the amount of space needed for a 32-bit interface using the package types discussed in this report. The LFBGA 96-ball package requires the least amount of space.

Creating the interface using two SSOP packages requires 4.5 times as much space.

The low-profile, fine-pitch, 96-ball grid array package requires 2.32 mm^2 per bit, while the TVSOP package requires almost twice as much space at 4.14 mm^2 per bit. The space required using the TSSOP package is 6.65 mm^2 per bit, and for the SSOP package the space is 10.69 mm^2 per bit.

Height 2.8 mm
0.635 mm Pitch
Height 1.2 mm
0.5 mm Pitch
Height 1.2 mm
0.4 mm Pitch
Height 1.4 mm
0.8 mm Pitch
15.85 mm
48-Pin
DL
SSOP
12.5 mm
48-Pin
DGG
TSSOP
9.7 mm
48-Pin
DGV
TVSOP
15.85 mm
48-Pin
DL
SSOP
13.5 mm
96-Ball
GKE
LFBGA
9.7 mm
48-Pin
DGV
TVSOP
12.5 mm
48-Pin
DGG
TSSOP
5.5 mm
6.4 mm
8.1 mm
10.32 mm
32-Bits
74.25 mm^2
32-Bits
132.5 mm^2
32-Bits
213.0 mm^2
32-Bits
342.0 mm^2

Figure 29. Space Needed for a 32-Bit Interface Using Various Packages Options

Summary

The trend toward 32-bit, or wider, bus systems reflects the need to increase the data rate in modern computer systems, and there is a corresponding demand for bus drivers supporting wider data formats.

To meet these requirments, TI has introduced the Widebus devices and low-profile fine-pitch ball grid array package.

Optimizing the voltage supply via staggered pinning for the Widebus packages ensures extremely low interference voltages, even during simultaneous switching of several outputs (simultaneous-switching interference). Additionally, Widebus packages allow the very high speeds that can be achieved with modern semiconductor technology to be fully exploited at the system level as well.

The TVSOP package is the smallest Widebus package. It gives the best results among the Widebus dual in-line packages for the ground-bounce and simultaneous-switching parameters of several outputs. The additional delay caused by simultaneously switching outputs also was the smallest with this package. However, the TVSOP package currently is still relatively difficult to process due to its very small pin-to-pin spacing of 0.4 mm.

The LFBGA package features another improvement: terminals are in the form of balls, leading to a further reduction in parasitic inductance.

In addition to the circuit-board space advantages it affords, the LFBGA package achieves a marked improvement in signal quality for all measurements as a result of its low package parasitics and, particularly, its minimal inductance.

The LFBGA package also demonstrates good heat resistance. A θ_{JA} of 40°C/W represents at least twice the heat dissipation efficiency of any of the other Widebus packages investigated for this report.

Acknowlegment

The author of this application report is Johannes Huchzermeier.

Glossary

AC	Advanced CMOS
ABT	Advanced BiCMOS Technology
AHC	Advanced High-Speed CMOS
ALVC	Advanced Low-Voltage CMOS
ALVT	Advanced Low-Voltage Technology
ALS	Advanced Low-Power Schottky
AS	Advanced Schottky
AVC	Advanced Very-Low-Voltage CMOS
Auto3-state	Devices with Auto3-state tolerate a higher voltage level at the outputs during active-high state at the output. (also called overvoltage protection)
BCT	BiCMOS technology
BiCMOS	Combination of the bipolar and CMOS manufacturing processes, with CMOS input structure and bipolar output structure
Bonding wire	Wire connecting the chip and the pin
Bus hold	An input circuit that holds the last valid state before the onset of the undefined state on the bus until a new valid logic state ensues
Coupling factor	Reciprocal inductive coupling between two neighboring pins on the basis of the transformer equation
GND	Ground (UK = Earth)
HC	High-speed CMOS
I/O	Input/Output
Leadframe	Metal mask to which the chip is attached, with the pins leading outward.
LFBGA	Low-profile fine-pitch ball grid array
LS	Low-Power Schottky
LVC	Low-Voltage CMOS
LV	Low-Voltage CMOS, originally designed for 3.3-V V_{CC}, but also usable with a 5-V V_{CC}
LVT	Low-voltage technology

OEC™	Output Edge Control, a procedure patented by Texas Instruments that reduces the output-signal slew rate.
R_{Load}	Load resistance
S	Schottky
SPICE	Simulation Program with Integrated Circuit Emphasis
SSOP	Shrink Small-Outline Package
TSSOP	Thin Shrink Small-Outline Package
TVSOP	Thin Very Small-Outline Package
TTL	5-V Logic, Transistor-Transistor Logic
V_{CC}	Supply voltage

Bibliography (Texas Instruments Publications)

1. *AVC Logic family Technology and Applications*, 1998, literature number SCEA006A
2. *ABT Logic Advanced BiCMOS Technology*, Databook, 1998, literature number SCBD002C
3. *Advanced CMOS Logic, Databook*, 1996, literature number SCADE02
4. *Logic Selection Guide and Databook CD-ROM*, April 1998, literature number SCBC001B
5. *Cross Bar Technology & Cross Bar Technology Low Voltage (CBT & CBTLV)*, 1999, literature number SCDD001B
6. *AHC/AHCT Logic, Databook 1997*, literature number SCLD003A
7. *Design Considerations for Logic, 1997*, literature number SDYA002
8. *Digital Design Seminar – Reference Manual*, 1998, literature number SDYDE01B
9. *What a Designer Should Know,* November 1994, literature number SDZAE03
10. *Electromagnetic Emission from Logic Circuits*, March 1998, literature number SDZAE17,
11. *The Bergeron Method*, September 1985, literature number SDZAE02
12. *Bus-Interface Devices with Output-Damping Resistors or Reduced-Drive Outputs*, August 1997, literature number SCBA012A
13. *Live Insertion*, November 1995, literature number SCZAE07
14. *TVSOP Thin Very Small Outline Package*, August 1997, literature number SDZAE02
15. *Low Voltage Logic Families*, April 1997, literature number SCVAE01A
16. *Bushold Circuit*, July 1992, literature number SDZAE15
17. *PCB Design Guidelines for Reduced EMI*, Mai 1998, literature number SDYA017
18. *Input and Output - Characteristics of Digital Integrated Circuits at V_{CC} = 5 V Supply Voltage*, literature number SCYA002
19. *Input and Output - Characteristics of Digital Integrated Circuits at V_{CC} = 3.3 V Supply Voltage*, literature numberSCYA003
20. *G.Becke, E.Haseloff, Das TTL- Kochbuch (The TTL Cook Book)*, literature number SDYZG17

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.

Copyright © 1999, Texas Instruments Incorporated