Interfacing the TLC3544 or TLC3548 ADC to the MSP430F149 MCU

ABSTRACT

The TLC3544 and TLC3548 14-bit serial-output analog-to-digital converters can easily interface to the serial peripheral interface port of many popular microcontrollers. Using the serial port of the TI MSP430F149 MCU, this application report focuses on configuring, sampling, and converting analog data presented to the ADC. The assembly code developed for this application report shows how the EOC/INT pin can be used as an interrupt source to the host processor.

The associated source code is available from http://www.ti.com/lit/zip/slaa126.
Introduction

The TLC3544 and TLC3548 are 4- and 8-channel, 14-bit, serial ADCs. Each device has chip select (CS), input clock (SCLK), serial data input (SDI), and serial data output (SDO) pins that can interface directly to a microprocessor. These data converters also feature a programmable end-of-conversion or interrupt (EOC/INT) pin, which can be used to initiate an interrupt service routine on the host processor.

This application report takes advantage of the hardware built into the TLC3544/48 evaluation module. A 20-pin ribbon cable from J12 on the data converter EVM to the microprocessor board is used to carry the necessary interface signals. The EVM’s on-board signal generator provides the analog signals, and W17 allows the user to select either 3.3 V or 5.0 V as the digital I/O voltage. Because the MSP430F149 is a low-voltage device, the EVM’s I/O voltage must be set to 3.3 V before attempting to use this processor.

Ten-pin, dual-row headers were added to the microprocessor boards to accommodate the cable from the data converter EVM. Figure 1 shows the system configuration, and Table 1 shows the connector pinout used.

The sample code (see Section 6) was developed using the Texas Instruments MSP430F149 evaluation board. This simple code example demonstrates how to configure the serial port, initialize the data converter, and process an interrupt (through the EOC/INT pin) from the data converter.

2 TLC3544/48 Evaluation Module

The data converter EVM used for this application report can have either the TLC3544 or the TLC3548 installed at location U9. These are 14-bit, 200-kspss serial analog-to-digital converters with four (TLC3544) or eight (TLC3548) analog input channels.

The TLC3544 and TLC3548 devices operate from a single 5-V analog supply and a 3.3-V or 5.0-V digital supply. The EVM contains regulators that provide all the necessary voltages from a standard 12-V laboratory power supply.

The EVM features a convenient onboard signal generator as well as all the necessary hardware to provide accurate reference voltages to the data converters. Connectors J12, J13, and J14 are 10-pin dual-row headers. These headers simplify interfacing a microcontroller-based system. The shorting bars can be removed from headers J13 and J14, allowing the user to define a custom signal-interface to the EVM.

System I/O voltages, as well as the voltage on the digital portion of the ADC, can be set to either 3.3 V or 5.0 V by changing the position of W17. When W17 is in position 2-3, the I/O voltage is set to 5.0 V. Position 1-2 on W17 lowers the I/O voltage to 3.3 V, which is necessary when running the low-power MSP430™ family of microcontrollers.
Although the onboard signal generator was used as the analog source in this application report, the TLC3544/48 EVM contains a variety of input and output connectors, signal conditioning circuits, and reference voltage options, so that users can define custom analog input conditions. It is even possible to tie the EVM directly into an existing control system – see the TLC3578 Family Evaluation Module User's Guide for complete details.

### Table 1. EVM to Micro Cable Definition

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>MSP430F149 Port</th>
<th>J12 Pin Name</th>
<th>Signal Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>P3.5 - SS CS</td>
<td>HOST_CNTLa</td>
<td>Low = ADC CS; High = DAC CS</td>
</tr>
<tr>
<td>3</td>
<td>P3.3 - CLKS</td>
<td>HOST_CLKXa</td>
<td>Serial clock to EVM</td>
</tr>
<tr>
<td>5</td>
<td>Not used</td>
<td>HOST_CLKRa</td>
<td>Serial clock return to HOST</td>
</tr>
<tr>
<td>7</td>
<td>P3.1 - MOSI</td>
<td>HOST_DXa</td>
<td>Serial data to EVM</td>
</tr>
<tr>
<td>9</td>
<td>P3.2 - MISO</td>
<td>HOST_DRa</td>
<td>Serial data to host</td>
</tr>
<tr>
<td>11</td>
<td>P3.6 - GPIO</td>
<td>HOST_FSXa</td>
<td>Frame sync to EVM</td>
</tr>
<tr>
<td>13</td>
<td>Not used</td>
<td>HOST_FSRa</td>
<td>Frame sync return to host</td>
</tr>
<tr>
<td>15</td>
<td>P1.1 - EINT</td>
<td>HOST_INT*</td>
<td>ADC configured as INT</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>ADC configured as EOC</td>
</tr>
<tr>
<td>17</td>
<td>Not used</td>
<td>HOST_CLKSa</td>
<td>Clock source for host – from EVM</td>
</tr>
<tr>
<td>19</td>
<td>P3.7 - GPIO</td>
<td>HOST_CNTLb</td>
<td>CSTART to ADC</td>
</tr>
<tr>
<td>2 to 20 (even)</td>
<td>GND</td>
<td>DGND</td>
<td>Ground connections</td>
</tr>
</tbody>
</table>

## 3 Serial Interface

The following sections give specific details of the serial data communication pins of the TLC3544 and TLC3548 devices.

### 3.1 Chip Select (CS)

Chip select is an active-low input signal. When CS is high, the serial-data output (SDO) pin is in a high-impedance state. The serial-data input (SDI) is ignored, and the serial clock (SCLK) is disabled from the internal data clocking circuits. A falling edge of CS, resets the internal 4-bit counter, enables SDI, and removes SDO from its high-impedance state. CS must be held low for the entire sampling period in order to provide valid data conversions (see the TLC3544 data sheet for details).

The chip select signal is shown on the interface section of the EVM schematic as HOST_CNTLa. When HOST_CNTLa is pulled low, the TLC3544/48 ADC is selected.

### 3.2 Serial Data Input (SDI)

The serial data input to the ADC consists of a 16-bit word presented MSB first. The first 4 MSBs are decoded as a one-of-four bit command. The Configure Write command (1010b or 0xA) lets the user enable various operating modes by setting or clearing bits of the internal configuration registers. When initializing the ADC after power up, two write cycles are recommended to ensure correct programming. The first write cycle should contain the CW command, followed by zeros (0xA000h). The second write cycle can contain any valid configuration option as defined in the device datasheet. Input data is shifted into the device on the rising edge of SCLK.

During normal sample-and-convert cycles, the first 4 MSBs are responsible for channel selection and the selection of various test and FIFO read modes. The remaining 12 bits are normally zeros and are ignored by the ADC.

### 3.3 Serial Data Output Pin (SDO)

The serial data output from the ADC consists of the 14-bit result of the previous conversion cycle. The output data is presented MSB first. When using chip select as the conversion trigger, the MSB is available at the falling edge of CS. Subsequent data bits are shifted out from the SDO pin on the rising edges of SCLK. Data should be considered valid on the falling edges of SCLK.
3.4 **Serial Clock Pin (SCLK)**

The host processor provides the serial clock input. SCLK clocks the configuration data into, and conversion data out of, the ADC. When the ADC is appropriately programmed, the serial clock can also be used as the conversion clock. No special configuration is required to run the SCLK in burst mode.

4 **Control and I/O Pins**

4.1 **Conversion Start (CSTART)**

CSTART is an active low-external sampling trigger. Pulling this line low initiates the sampling period on the selected (through SDI) analog input. A low-to-high transition starts the conversion process. CSTART should be pulled to DVDD when not in use. For the purpose of this application report, a general-purpose I/O pin from the microprocessor was used to hold the CSTART pin high.

4.2 **Frame Sync (FS)**

The FS input signal is normally used in DSP based systems to indicate the start of a serial data frame. If FS is low at the falling edge of CS, the rising edge of the frame sync pulse initiates the sample-and-convert cycle. FS should be pulled to DVDD when not in use.

The TLC3544/48 evaluation module uses a common frame-sync line for both the ADC and DAC. The Xilinx PLD located at U15, acts as a gatekeeper by determining which device (ADC or DAC) should receive the incoming signal. When the HOST_CNTLa line is low (ADC is selected), the PLD routes the incoming FS to the ADC. When HOST_CNTLa is high, the FS signal is applied to the DAC.

4.3 **End of Conversion/Interrupt (EOC/INT)**

The EOC/INT pin is a programmable output, which indicates the end of conversion (EOC) or acts as an interrupt (INT) to host processor. When programmed as EOC, the output goes from a high-to-low state at the end of the sampling period and returns to a high state when the conversion process is complete. In other words, EOC indicates that the ADC is busy doing a conversion.

When programmed as INT, the pin goes low after the conversion is complete, and stays low until reset by the falling edge of CS or CSTART. A rising edge on the FS input can also clear INT.

The assembly code for this application report uses the EOC/INT pin to signal the processor that the conversion process has completed. The configuration/channel selection information is transmitted to the ADC as two bytes. The processor then enters a loop that transmits zeros or dummy data until it receives an interrupt from the ADC.

4.4 **Device Pinout**

Table 2 shows the complete device pin assignments for both the TLC3544 and TLC3548 devices.

<table>
<thead>
<tr>
<th>3544</th>
<th>3548</th>
<th>Pin Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>SCLK</td>
<td>Serial input clock</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>FS</td>
<td>Frame sync: DSP frame synchronization input, tied to Vcc when not used</td>
</tr>
<tr>
<td>3</td>
<td>3</td>
<td>SDI</td>
<td>Serial data Input: the 4 most significant bits select test modes, mux channel, and conversion speed</td>
</tr>
<tr>
<td>4</td>
<td>4</td>
<td>EOC/INT</td>
<td>End of conversion/interrupt: used to indicate the converter is busy, or as an external interrupt source to the host processor</td>
</tr>
<tr>
<td>5</td>
<td>5</td>
<td>SDO</td>
<td>3-State serial output of conversion result</td>
</tr>
<tr>
<td>6</td>
<td>6</td>
<td>DGND</td>
<td>Digital ground reference</td>
</tr>
<tr>
<td>7</td>
<td>7</td>
<td>DVDD</td>
<td>Digital supply voltage: 2.7 to 5.5 V dc</td>
</tr>
<tr>
<td>8</td>
<td>8</td>
<td>CS</td>
<td>Chip select: active low</td>
</tr>
<tr>
<td>9-12</td>
<td></td>
<td>A0 – A4</td>
<td>Analog inputs of the TLC3544</td>
</tr>
<tr>
<td>9-16</td>
<td></td>
<td>A0 – A8</td>
<td>Analog inputs of the TLC3548</td>
</tr>
</tbody>
</table>
Table 2. I/O Pins of the TLC3544/48 (continued)

<table>
<thead>
<tr>
<th>3544</th>
<th>3548</th>
<th>Pin Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>13</td>
<td>17</td>
<td>AVDD</td>
<td>Analog supply voltage</td>
</tr>
<tr>
<td>14</td>
<td>18</td>
<td>AGND</td>
<td>Analog ground reference</td>
</tr>
<tr>
<td>15</td>
<td>19</td>
<td>REFP</td>
<td>Upper reference voltage: 5.0 V maximum</td>
</tr>
<tr>
<td>16</td>
<td>20</td>
<td>REMF</td>
<td>Lower reference voltage: nominally ground</td>
</tr>
<tr>
<td>17</td>
<td>21</td>
<td>BGAP</td>
<td>Internal band gap compensation: see data sheet for requirements</td>
</tr>
<tr>
<td>18</td>
<td>22</td>
<td>AGND</td>
<td>Analog ground reference</td>
</tr>
<tr>
<td>19</td>
<td>23</td>
<td>AVDD</td>
<td>Analog supply voltage</td>
</tr>
<tr>
<td>20</td>
<td>24</td>
<td>CSTART</td>
<td>External start of conversion trigger: used for extended sampling mode</td>
</tr>
</tbody>
</table>

5 ADC Initialization and Operation

5.1 Initializing the ADC

Initializing the ADC is a relatively straightforward task. After power up, EOC/INT is high and the data registers are set to zero. The user has the option of setting a default hardware mode, or programmed mode. Each mode requires two 16-bit initialization cycles. Data output from the power up initialization phase should be ignored. For the purpose of this application report, the initialization cycle consists of chip select being held low through two 8-bit SCLK cycles.

Hardware mode is defined by the status of the SDI pin. After power up, two consecutive initialization cycles put the device into hardware mode if the SDI pin is tied to DVDD. This loads the ADC’s configuration register with 0x0800h.

To enter the programmed mode, the host processor must write 0xA000h (WRITE CFR + 000h) to the SDI pin during the first initialization cycle, followed by a WRITE CFR + DATA command during the second.

![Figure 2. ADC Initialization Cycle](image)

5.2 Operating the ADC

This application report is based on the one-shot operating mode (mode 00) using chip select (CS) as a conversion trigger. In this mode, each cycle performs one sample and one conversion on the selected analog input channel. Operation begins by bringing chip select low.

Channel selection is accomplished by writing 0000h through 0700h to the SDI pin of the ADC. The microprocessor presented in this application report uses 8-bit data packets when writing to the serial port. The upper and lower bytes are transmitted to the ADC by writing to the micro’s data buffer twice, while holding the CS pin low. The first byte [D15:D8] contains the channel selection information, and the second byte [D7:D0] consists of zeros, or a dummy value transfer.

The TLC3544 and TLC3548 also feature three test modes that can be accessed by writing 0xB000h, 0xC000h or 0xD000h to the SDI pin. Test mode 1 (0xB000h) presents a digital code on SDO equivalent to (REFP + REMF) / 2. Test mode 2 and 3 present a digital code equal to REMF or REFP respectively.
ADC Initialization and Operation

5.3 EOC or INT

Figure 4 shows the relationship of the EOC and INT signals more clearly. The EOC signal is active low while the ADC is converting the sampled data. It returns to a high state when the conversion is complete.

INT is active low after the (sample plus conversion) period has finished. INT is cleared when a new sample-and-conversion cycle is initiated by either a falling edge of CS (see Figure 4) or rising edge of FS.

Figure 3. Sample-and-Convert Cycle

Figure 4. EOC/INT Timing
6 MSPF149 Code Example

The following code example can be downloaded from http://www.ti.com/lit/zip/slaa126.

;;; MSP430F149 Demo - SPI Communication with TLC3544/48 or TLC3574/78 EVM
;;; Program implements a digital filter - takes the average of 4 samples
;;; from CH0 of the ADC and returns them to the TLV5636 DAC

TLC3544/48 MSP430F149
--------------------
| SDI | CH0~> | IN+ | SCLK | /CS | FS | CSTART | INT | |-----|----|----|-----|----|----|--------|----|-------------------
|     |     |----|----|----|----|---------|----|-------------------
|     |     | SDI |     |     | SDO |        |     |-------------------
| 3.1 |     |     |     | P3.2|     |        |     |-------------------
|     | 3.3 |     |     | P3.6|     |        |     |-------------------
|     |     |     |     | P3.7|     |        |     |-------------------
|     |     |     |     |     |     | P3.5   |     |-------------------
|     |     |     |     |     |     |        |     |-------------------
|     |     |     |     |     |     | P3.1   |     |-------------------
|     |     |     |     |     |     |        |     |-------------------
|     |     |     |     |     |     |        |     |-------------------

Assembled with IAR Embedded Workshop for MSP430 Kickstart

Texas Instruments, Inc.
Tom Hendrick
Data Acquisition Applications - Dallas
Dec. 2000

#include "msp430x14x.h" // Standard Equations
#include "TLC357X.h" // ADC Equations

Constants

CS equ 020h ; Assign p3.5 to CS
FS equ 040h ; Assign p3.6 to FS
CSTART equ 080h ; Assign p3.7 to CSTART
Samples equ 004h ; Number of Sample for Filter

Setup RAM

RSEG UDATA0
ADC_Data DS 0 ; Storage for ADC Samples

Setup Stack

RSEG CSTACK
DS 0

Program Code

RSEG CODE
RESET_ISR
mov #SFE(CSTACK),SP ; define stackpointer
call #Init_Sys ; Initialize the MSP430
call #SETUP_ADC ; Initialize the ADC
call #Mainloop ; Run the Main Program

Mainloop
mov.b #Samples, R10 ; Move the # of samples required to R10
mov #00, R8 ; Clear R8

SampleLoop
bic.b #CS,&P3OUT ; Enable TLC3544/48
bis.b #01h,&P1OUT ; Set a test bit - Bit is cleared in ISR

Read_ADC
mov.b #CH0,&U0TXBUF ; Dummy write to SPI (generates SCLK)
call #CLEAR
mov.b &U0RXBUF,ADC_Data(R8) ; Store Upper Byte
inc R8 ; Increment data storage pointer
mov.b #DUMMY,&U0TXBUF ; Dummy write to SPI (generates SCLK)
call #CLEAR
mov.b &U0RXBUF,ADC_Data(R8) ; Store Lower Byte
inc R8 ; Increment data storage pointer

TEST:
mov.b #DUMMY,&U0TXBUF ; Dummy write to SPI
call #CLEAR
bit.b #01h, &P1OUT ; Test bit - keep writing 0’s to port
jnz TEST ; until an interrupt occurs
dec R10
cmp #00,R10 ; Finished taking sample?
jnz SampleLoop ; Repeat till R10 = 0
;jmp Mainloop ; Repeat

; Remove remark from above line to skip transmit back to DAC

Write_DAC
mov #0x0000, R13
mov #Samples, R10
mov #0x0000, R8

next
mov ADC_Data(R8), R12
swpb R12 ; Swap Bytes
and.w #0xFFF0, R12 ; Strip trailing bits
rrc.w R12 ; Shift data 4 places
rrc.w R12 ; to conform to
rrc.w R12 ; DAC input format
rrc.w R12 ; Data is shifted!
and.w #0xOFFF, R12 ; Strip any carries
add.w R12, R13
incd R8
dec R10
cmp #00, R10
jnz next
rrc.w R13 ; Divide by 2
rrc.w R13 ; Divide by 2 again
and.w #0xOFFF, R13 ; Strip any carries
add.w #0x4000, R13 ; Set DAC Fast Mode, 0x4000
bic.b #FS,&P3OUT ; toggle Frame Sync
bic.b #FS,&P3OUT ; toggle Frame Sync
bic.b #FS,&P3OUT ; to DAC
swpb R13 ; Align MSB First
mov.b R13,&U0TXBUF ; Transmit upper Data Byte to DAC
call #CLEAR
swpb R13 ; Prepare Lower Byte
mov.b R13,&U0TXBUF ; Transmit lower Data Byte to DAC
call #CLEAR
bis.b #FS,&P3OUT ; Set Frame Sync
jmp Mainloop ; Repeat

; Clear TX Flag
CLEAR

bit.b #UTXIFG0,&IFG1 ; Thank You Eric! TXBUF ready?
jnc CLEAR ; 1 = ready
bic.b #UTXIFG0,&IFG1
ret

Init_Sys; Modules and Controls Registers set-up subroutine

StopWDT mov #WDTPW+WDTHOLD,&WDTCTL ; Stop Watchdog Timer

SetupClock
bic.b #XTOFF, &BCSCTL1
bic.b #SEL1+SELS, &BCSCTL2

HF_WAIT ; 8MHz Crystal used - wait for stabilization
bic.b #OFIFG, &IFG1
bit.b #OFIFG, &IFG1
jnz HF_WAIT
bic.b #OFIFG, &IFG1 ; Clear Oscillator fault flag
bit.b #OFIFG, &IFG1 ; Test for clear

SetupPort
bic.b #001h,&P1DIR ; P1 pin 1 set to output (toggle's LED)
bic.b #01Eh,&P3SEL ; P3.1,2,3,4 SPI option select
bic.b #CS+FS+CSTART,&P3DIR ; /CS, FS & CSTART = P3 output direction
bic.b #CS+FS+CSTART,&P3OUT ; P3.5,6,7 CS & FS set

SetupInterrupt
bic.b #02h, &P1IFG ; Clear interrupt flags
bic.b #02h, &P1IES ; Set for edge selection
bic.b #02h, &P1IE ; Enable external Interrupt

SetupSPI
bic.b #040h,&ME1 ; Enable SPI TX/RX
mov.b #CHAR+SYNC+MM,&U0CTL ; 8-bit SPI Master
bic.b #SSEL0+SSEL1+STC,&U0TCTL
mov.b #02h,&U0BR0 ; Set SPI Baud Rate
mov.b #00h,&U0BR1 ; This gives 4MHz SCLK w/ 8MHz Crystal
mov.b #00h,&U0MCTL
eint ; Enable interrupts
ret

SETUP_ADC ; Initialize the AtoD Converter

bic.b #CS,&P3OUT ; Set ADC /CS Lo
mov.b #WRITE,&U0TXBUF ; Write 0xA0h to SPI (generates SCLK)
call #CLEAR ; Clear SPI TX/RX Flag
mov.b #DUMMY,&U0TXBUF ; Dummy write to SPI (generates SCLK)
call #CLEAR
bic.b #CS,&P3OUT ; Set ADC /CS Hi
bic.b #CS,&P3OUT ; Set ADC /CS Lo

; Configuration Write to ADC
; See "TLC357X.h" file for details on the following parameters
mov.b #(WRITE+SHORT_SAMP+EXT_REF),&U0TXBUF
call #CLEAR
References

1. TLC3544, TLC3548 5-V Analog, 3-/5-V Digital, 14-Bit, 200-kmps, 4-/8-Channels Serial Analog-to-Digital Converters With 0-5 V (Pseudodifferential) Inputs
2. TLC3578 Family Evaluation Module User's Guide
3. MSP430x1xx Family User's Guide
4. MSP430F13x, MSP430F14x, MSP430F14x1 Mixed-Signal Microcontrollers
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