

Using ADS8411 in a Multiplexed Analog Input Application

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ABSTRACT

This application report is intended as a guide for using an analog multiplexer to multiplex several input signals to a single high-resolution, high-speed SAR analog-to-digital converter (ADC). The ADC and the multiplexer used were the ADS8411 and the TS5A3159/3359, respectively. This document discusses the important parameters of a multiplexer and defines a few important measurements for evaluating a multiplexed system. The results of the evaluation are presented.

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1 Introduction

ADS8411 is a 16-bit, 2-MSPS analog-to-digital converter (ADC) with a 4-V reference. The device includes a 16-bit capacitor-based SAR ADC with inherent sample and hold. It has a unipolar single-ended input. The device offers a 16-bit parallel interface.

The TS5A3159 is a single-pole, double-throw (SPDT) analog switch that is designed to operate from 1.65 V to 5.5 V. The device offers a low ON state resistance and an excellent ON resistance matching with the break-before-make feature to prevent signal distortion during the transfer of a signal from one channel to another. The device has an excellent total harmonic distortion (THD) performance and consumes low power. The TS5A3359 is a single-pole, triple-throw (SP3T) version of the same switch.

2 Block Diagram

Figure 1 shows a simple block diagram of a system consisting of two input channels and the ADS8411. A driver operational amplifier is needed to drive the ADC.

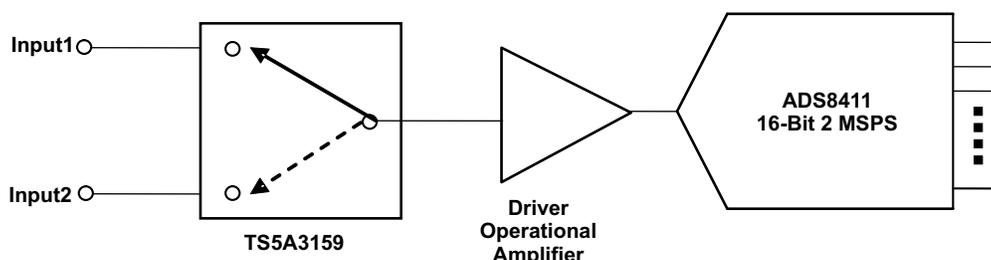


Figure 1. Simplified Block Diagram

3 Selection of Multiplexer

Figure 2 shows an equivalent circuit diagram of one of the channels of a multiplexer. C_S is the input capacitance of the channel; C_D is the output capacitance of the channel. R_{ON} is the resistance of the channel when the channel is ON. C_L and R_L are the load capacitance and resistance, respectively. V_{IN} is the input voltage of the source; R_S is the source resistance of the source. V_{OUT} is the output voltage of the multiplexer.

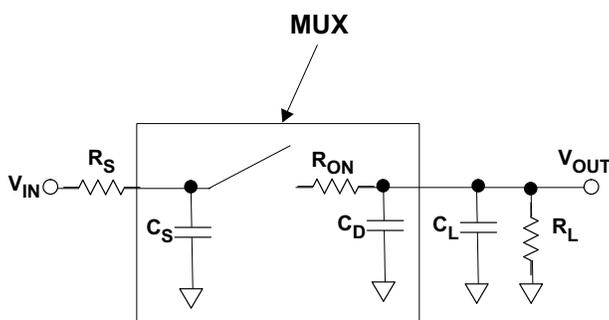


Figure 2. Multiplexer Equivalent Circuit

To improve settling time, the values of R_S , R_{ON} , C_S , C_D , and C_L need to be smaller, and the value of R_L should be large.

For TS5A3159

$$R_S = 1 \Omega$$

$$C_S = C_D = 84 \text{ pF}$$

Considering

$$R_S = 50 \Omega$$

$$C_L = 5 \text{ pF}$$

$$R_L = 10 \text{ k}\Omega$$

$$T_{RC} \text{ (time constant)} = 8.65 \text{ ns}$$

For a 16-bit system, at least 18-bit settling is required. For 18-bit settling, the time required is $(18 \times \ln 2) \times T_{RC} = 108 \text{ ns}$, which is better than 2 MSPS (500 ns). If the settling time is more than the conversion time of the ADC, the output of the multiplexer does not settle to the required accuracy which results in harmonic distortion.

One more important parameter of a multiplexer is the ON-state resistance variation with voltage. This also affects distortion because R_{ON} and R_L act like a resistor divider circuit and any variation of R_{ON} with voltage affects the output voltage. Figure 3 shows the variation of R_{ON} with V_{OUT} for TS5A3159.

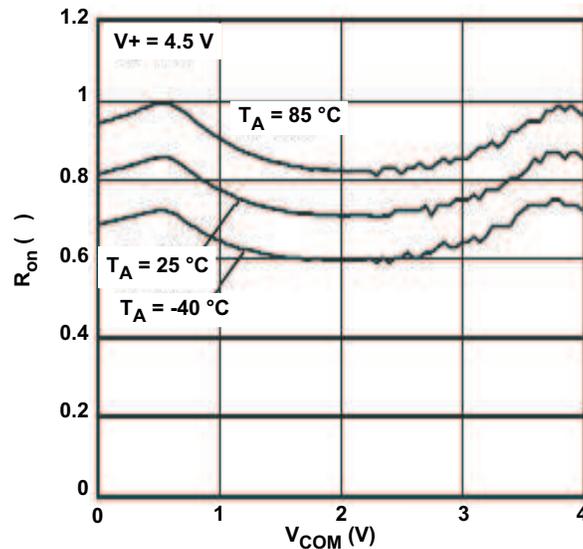


Figure 3. Variation of R_{ON} With Voltage

$$V_{OUT} = V_{IN} \times \frac{R_L}{R_L + R_{ON}} = V_{IN} \times \frac{1}{1 + \frac{R_{ON}}{R_L}} \cong V_{IN} \times \left(1 - \frac{R_{ON}}{R_L} \right) \quad (1)$$

For TS5A3159, assume that the peak variation of R_{ON} with voltage is 0.25Ω and R_L is $10 \text{ k}\Omega$. So, the variation of V_{OUT} because of R_{ON} variation is $V_{IN} \times 2.5 \times 10^{-5}$, which is -92 dB . This causes harmonic distortion. To improve harmonic distortion, the variation of R_{ON} should be low, and also R_L should be high.

4 Input Source

The input source should be a low-noise, low-distortion source with low source resistance. As discussed in the earlier section, R_S should be low to improve settling time. If the source is not a low-noise and low-distortion source, a passive filter can be added to improve the signal quality.

5 Driving Amplifier

The driving operational amplifier (OPA3 in Figure 4) in this application needs to have good slew rate and bandwidth along with low noise and distortion. The input of the operational amplifier may see a maximum step of 4 V because of MUX switching. So, even if the signal bandwidth is low, the driving OPA needs to settle from 0 V to 4 V (or 4 V to 0 V) within one ADC sampling frame. When selecting the operational amplifier, one has to ensure that it can settle from 0 V to 4 V (or from 4 V to 0 V) within the ADC sampling time (in this case 500 ns). The OPA used for driving the ADC is the THS4031.

The operational amplifiers (OPA1, OPA2 in Figure 4) used before the MUX is for signal conditioning. These operational amplifiers need to have low noise and distortion.

6 Driving Operational Amplifier Bandwidth Restriction

The bandwidth of the ADC driving operational amplifier (OPA3 in Figure 4) is restricted to get better performance. This is done by using an R–C filter at the output of OPA3. See the Analog eLab Webcasts *Quantifying Amp to ADC –Distortion Consideration* and *Quantifying Amp to ADC Interface Performance* under *Analog eLAB* on the TI Web site (www.ti.com) to learn more about this procedure.

$$\text{Bandwidth} \cong \frac{1}{2\pi R_1 C_1} \tag{2}$$

The noise contribution from an external circuit can be computed using the following guide *Op Amps for Everyone Design Guide* (SLOD006) from Texas Instruments.

7 Evaluation Setup

As shown in Figure 4, the evaluation system consists of the ADC (ADS8411), a driving operational amplifier (THS4031), the multiplexer (TS5A3159), an AC source, a DC source, and two driving operational amplifiers (two THS4031s or a single THS4032) for the sources to make them a low-impedance source, a passive band-pass filter after the AC source to filter the source noise and distortion

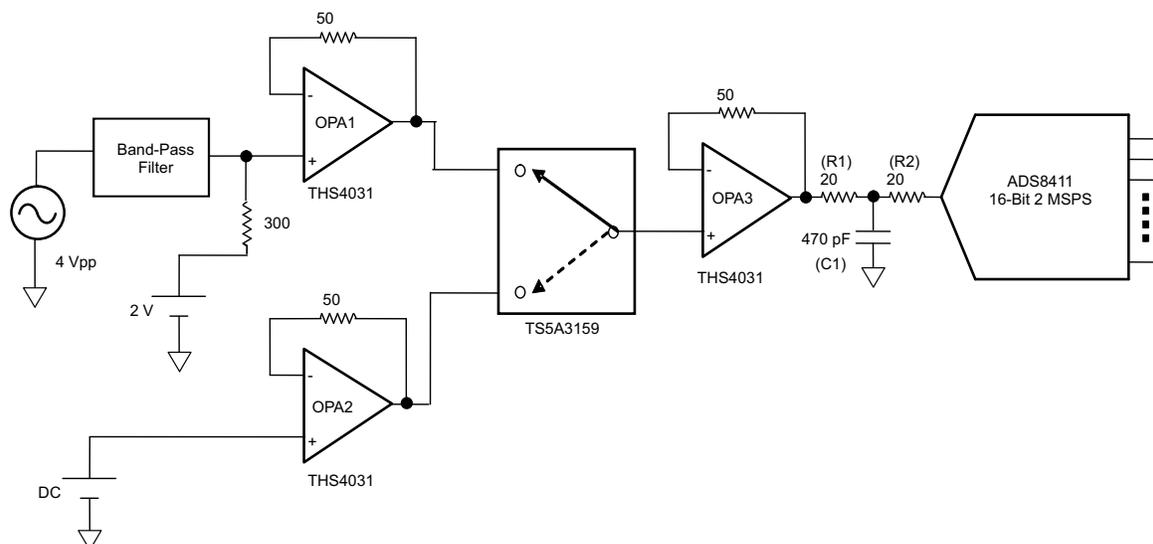


Figure 4. Evaluation Setup

8 Timing Diagram

Figure 5 shows the timing diagram of the system. The ADC has a conversion and sample phase. The MUX switches between channel 1 and channel 2, depending on the SELECT input to the MUX. The sample switch of the ADC opens after the falling edge of conversion start signal (CONVST). The MUX switching should be done after that. Some delay (t_d) occurs between the CONVST falling edge and the actual sample switch opening. Therefore, the MUX switching should occur after t_d of the CONVST falling edge. For ADS8411, t_d (max) is 50 ns; thus, each channel of the MUX gets 500–50 = 450-ns time to settle.

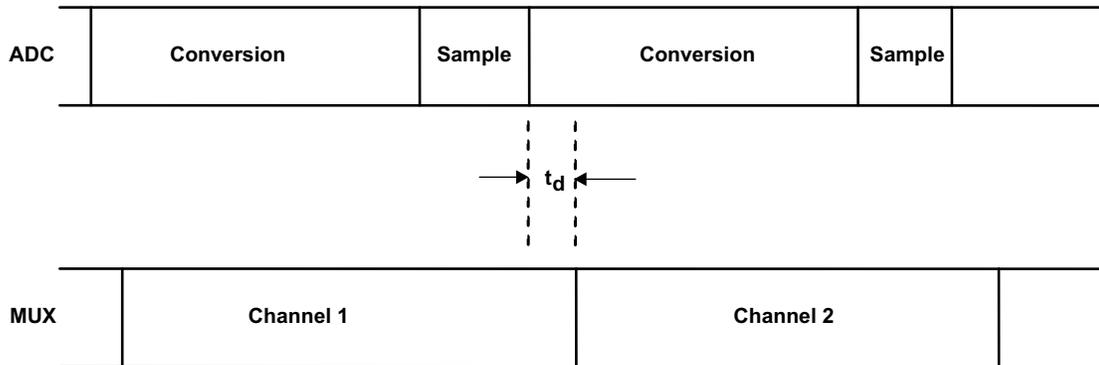


Figure 5. Timing Diagram

9 Important Measurement Parameters

AC parameters (Crosstalk, SNR, and THD) are evaluated.

Crosstalk: A sine wave is applied in channel 1, and channel 2 is fed with a DC voltage. Two channels are multiplexed at a speed which is half of the ADC speed. This ensures that the ADC sees alternate channels in two consecutive conversions. This means that each channel input is converted at a speed which is half the speed of the ADC. The converted digital output of the ADC consists of two datasets of two channels merged together. This data is post-processed and two datasets are separated out. FFT is taken for both the datasets. Ideally, the FFT of channel 1 should have the frequency of the sine wave as fundamental and harmonics along with noise bins. The FFT of the other channel should not have any AC component except the noise bins, because DC is applied to this channel. But because of multiplexing action, the FFT of channel 2 will show a tone, which has the frequency (with reduced amplitude) equal to the fundamental frequency of channel 1. The difference of the fundamentals (in dB scale) in these two FFTs is the crosstalk.

Therefore, crosstalk is equal to $10 \times \log \left(\frac{\text{Fundamental Power of Channel2}}{\text{Fundamental Power of Channel1}} \right)$

SNR: The signal-to-noise ratio is defined as $10 \times \log \left(\frac{\text{Signal Power}}{\text{Total Noise Power}} \right)$

THD: The total harmonic distortion is defined as $10 \times \log \left(\frac{\sum_{i=2}^9 (\text{i}^{\text{th}} \text{ Harmonic Power})}{\text{Signal Power}} \right)$

10 Results

The following table shows crosstalk, SNR, and THD at two different device speed and input frequencies.

DEVICE SPEED (MSPS)	INPUT FREQUENCY (kHz)	SNR	THD	CROSSTALK
1.25	20	85.6	-96.8	-109.8
1.25	100	85	-95.4	-99.6
2	20	85.6	-97.7	-119.5
2	100	84.8	-94.7	-98.6

Results

The following table shows the typical specification of ADS8411 as in the data sheet.

DEVICE SPEED (MSPS)	INPUT FREQUENCY (kHz)	SNR	THD
1.25	100	86	-90
2	100	86	-90

Figure 6 through Figure 9 show FFT of two channels at different device speeds and input frequencies.

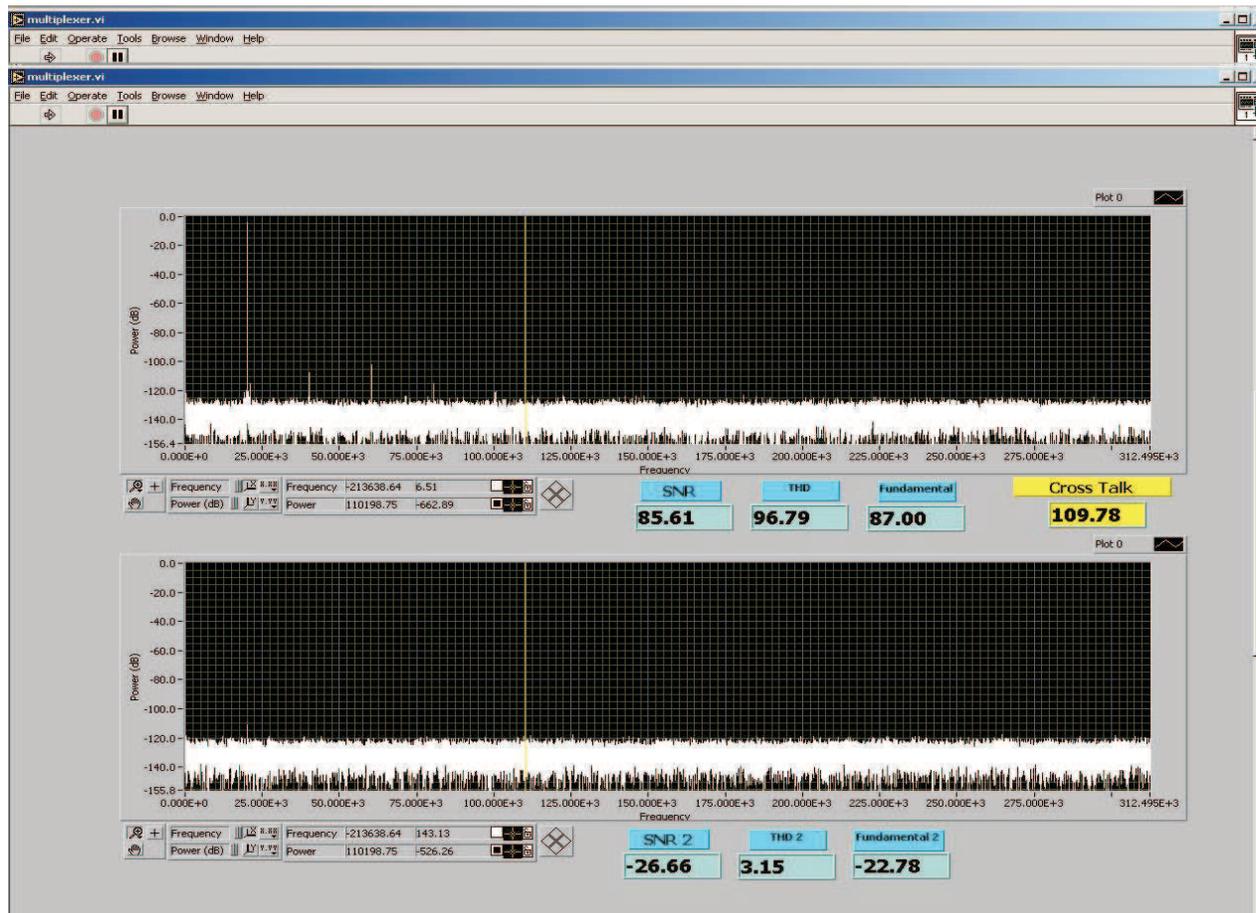


Figure 6. Input Frequency – 20.1 kHz, Device Speed – 1.25 MSPS

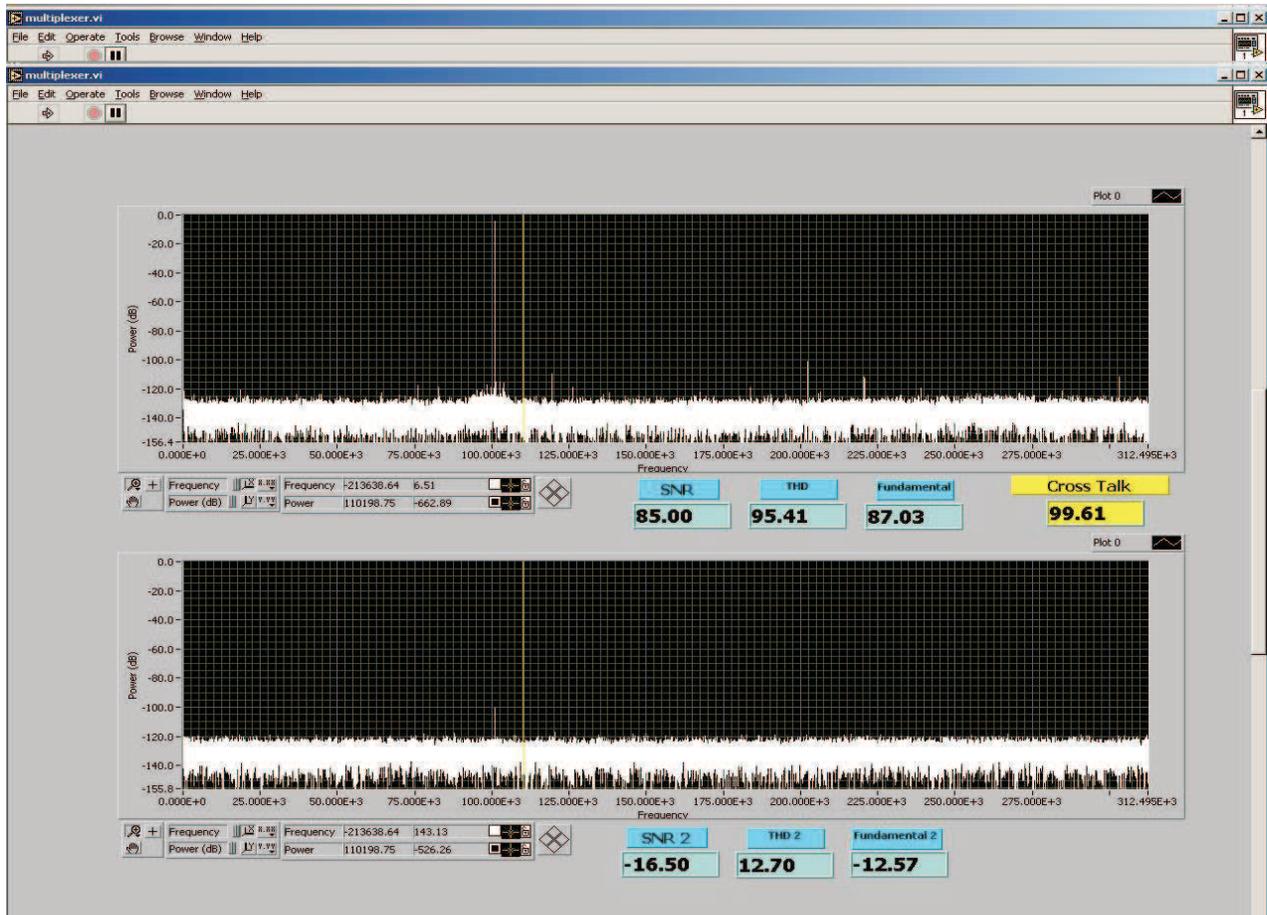


Figure 7. Input Frequency – 101.1 kHz, Device Speed – 1.25 MSPS

Results

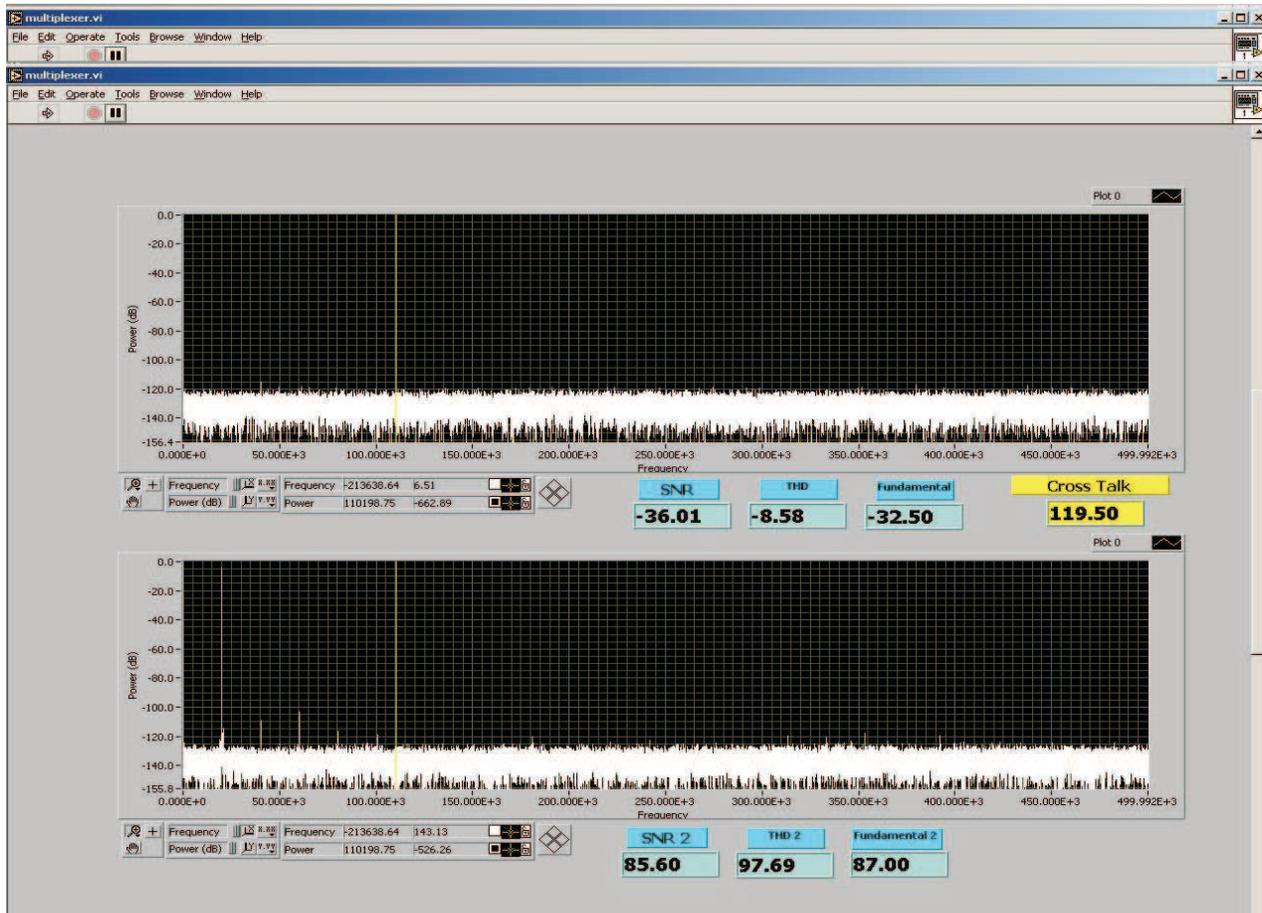


Figure 8. Input Frequency – 20.1 kHz, Device Speed – 2 MSPS

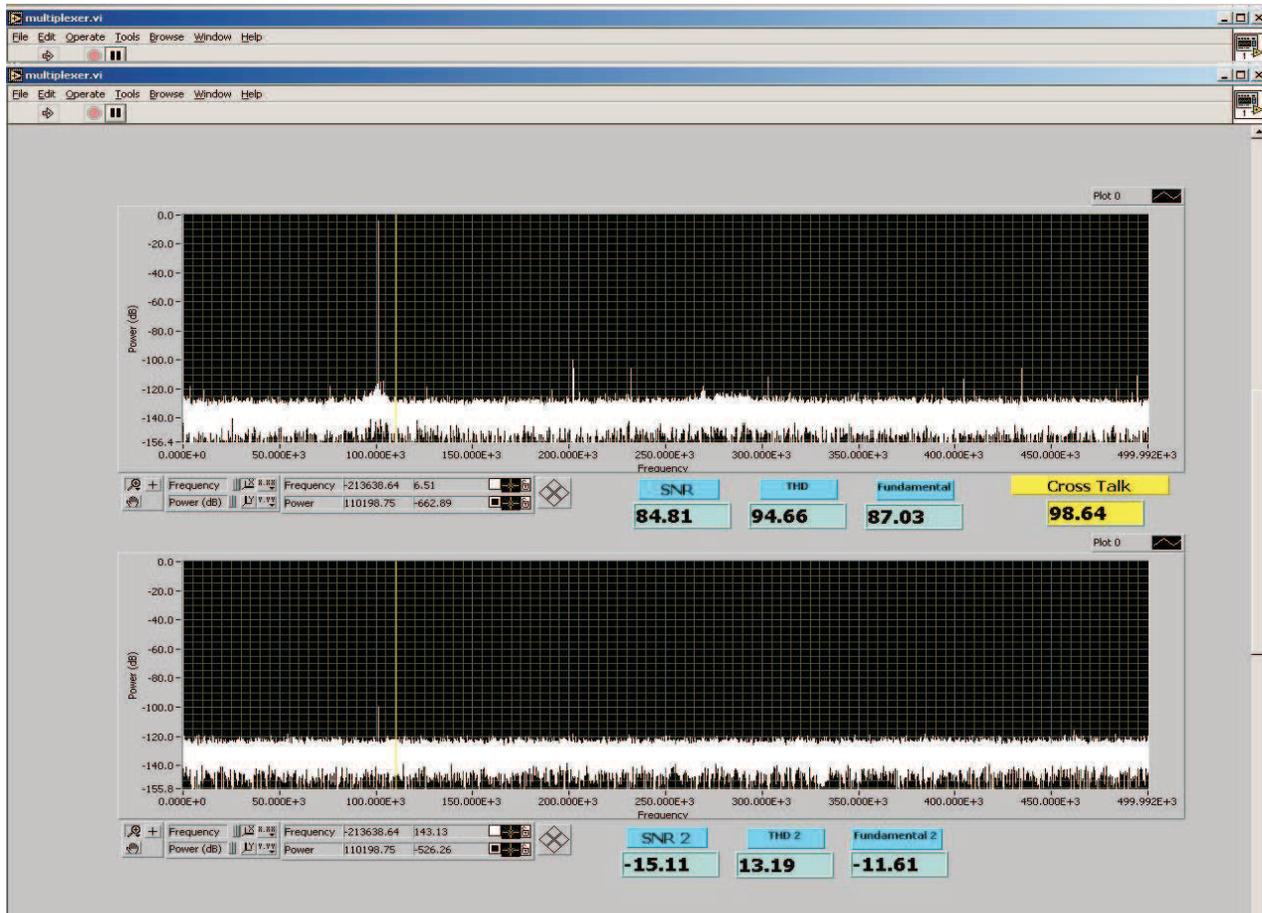


Figure 9. Input Frequency – 101.1 kHz, Device Speed – 2 MSPS

11 Effect of Bandwidth

The restriction of bandwidth by an R-C filter (after OPA3 in Figure 4) may result into better SNR and THD (Refer to *Quantifying Amp to ADC – Distortion Consideration* and *Quantifying Amp to ADC Interface Performance* under *Analog eLAB* to know more about this), but it makes the operational amplifier difficult to settle within the required accuracy. If the output does not settle properly, some residual charge of the previous channel remains in the next sampling. It appears as a crosstalk. If the throughput of the ADC is reduced, allowing the output of the operational amplifier to settle properly, the problem becomes smaller. Therefore, using a larger capacitor makes the operational-amplifier output settling slower. So, within the ADC sampling frame, the operational-amplifier output does not settle to its final level. The diagrams of Figure 10 and Figure 11 show SNR and crosstalk as a function of the filter capacitor.

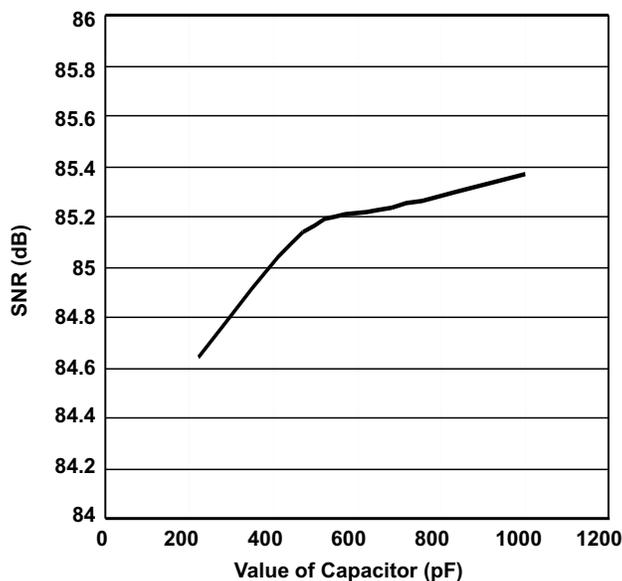


Figure 10. SNR Versus Input Bandwidth

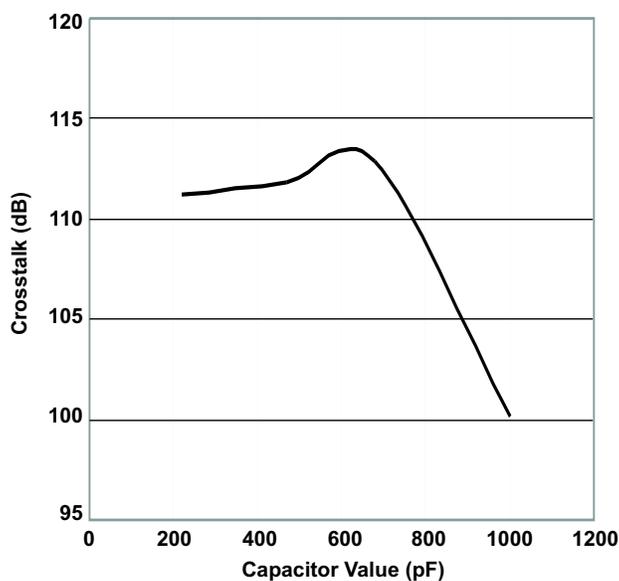


Figure 11. Crosstalk Versus Input Bandwidth

The input settling behavior is shown in [Figure 12](#) with three different bandwidths. The value of the capacitor is changed to change the bandwidth. As the bandwidth increases, the settling time improves.

$$\text{Bandwidth} \cong \frac{1}{2\pi R_1 C_1} \quad (3)$$

R1 and C1 are as shown in [Figure 4](#).

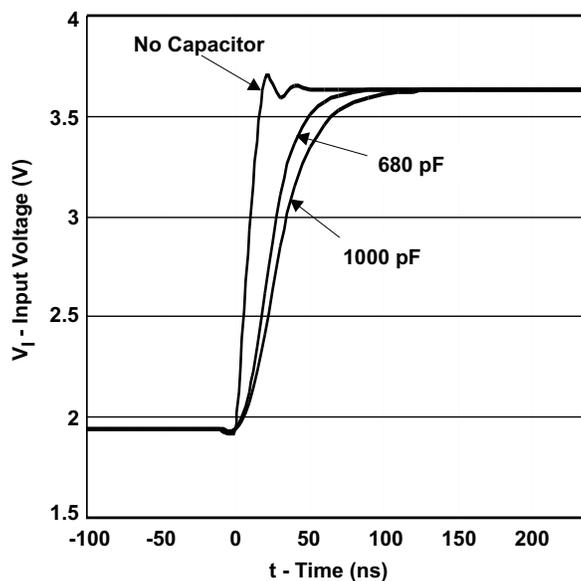


Figure 12. Input Settling With Different Values of Capacitor

12 Conclusion

TS5A3359 can be used for a three-input system.

Depending on the application, one of the parameters (SNR, THD, or crosstalk) can be improved with a compromise to another by suitably selecting the proper R-C filter and operational amplifier. For example, the ADC input capacitor can be increased to get better SNR.

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