Application Report
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Migrating From MSP430F13x/14x to MSP430F23x/24x

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ABSTRACT

The purpose of this application report is to facilitate the migration of designs based on the MSP430F133/F135/F147(1)/F148(1)/F149(1) device family to the MSP430F23x/F24x(1)/F2410 device family. In the course of this application report, the main differences between the two device families are highlighted, and migration solutions covering both software and hardware aspects are provided.

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1 MSP430x1xx Versus MSP430x2xx Family Comparison Overview

The MSP430x2xx family of microcontrollers provides an upgrade path for the MSP430x1xx family, offering more performance, lower power, and more built-in features. This enables an improved and more cost-optimized system design. Table 1 contains a general high-level comparison of the two device families, providing an overview of reasons why one should consider migrating.

Table 1. 1xx Versus 2xx High-Level Comparison

	MSP430x1xx	MSP430x2xx
Maximum CPU clock speed	8 MHz	16 MHz
Wake up from LPM3/LPM4	<6 µs	<1 µs
Standby current consumption (LPM3)	<2 µA	<1 µA
Brown-out reset	Selected devices only	All devices
Minimum voltage for flash ISP	2.7 V	2.2 V
Integrated port pullup/pulldown resistors	–	On all ports
Internal oscillator (DCO)	Large voltage and temperature drift (±20%)	Very small voltage and temperature drift (±2%) Factory calibrated
Oscillator fault detection	High-frequency crystal	High-frequency and low-frequency crystal
Additional built-in low-power low-frequency oscillator	–	12-kHz VLO
Additional oscillator features	–	Minimum pulse clock filter for increased system robustness Configurable built-in crystal load capacitors
Additional watchdog timer features	–	Invalid address detection Fail-safe clock source
Bootstrap loader (BSL)	Protected through 256-bit password	Hack proof
Flash memory configurations	Up to 60 KB	Up to 120 KB (as of 4Q07)
RAM	Up to 10 KB	Up to 8 KB (as of 4Q07)
Operating temperature (T_A)	–40°C to 85°C	–40°C to 105°C

While the MSP430F23x/24x can be considered as a direct pin-to-pin compatible drop-in to existing MSP430F13x/14x designs, there are some important details that require attention. This application report helps identify potential issues. After migration, the application benefits from all the MSP430F2xx family enhancements as indicated in Table 1. This could enable further cost savings or other system-level optimizations. This document focuses on transitioning existing designs and leaves it to the engineer to make use of additional MSP430F2xx features during migration as applicable for a given system (for example, the use of internal pullup/pulldown resistors, making changes to the clock configuration, etc.).

2 MSP430F13x/14x to MSP430F23x/24x Migration – Hardware Considerations

This section provides information on differences between the MSP430F13x/14x and MSP430F23x/24x families of devices that should be considered during migration. Fortunately, the hardware migration process is straightforward with only a few items to watch out for.

2.1 Device Package and Pinout

The good news is that a 64-pin LQFP MSP430F23x/24x device directly drops into an existing MSP430F13x/14x-based 64-pin LQFP/TQFP PCB footprint. The LQFP package variant is identical, and the PCB footprint is the same for both LQFP and TQFP. Both MSP430F13x/14x and MSP430F23x/24x are available in QFN packages. However, these packages differ slightly between the two device families. The exposed thermal pad on the MSP430F23x/24x QFN package is slightly smaller than the one on the MSP430F13x/14x package, and also the recommended SMT pad size differs slightly. Therefore, it is required to closely review the data sheet packaging specifications and the actual application PCB footprint during migration.

All MSP430F23x/24x pins can be used for the same purpose as the pins on their MSP430F13x/14x counterparts (which includes all analog and digital modules, as well as power supply and JTAG pins), enabling a transition to MSP430F23x/24x devices without changes to the application PCB.

Details regarding packaging and pinouts can be found in the device-specific data sheets. [3][4]

2.2 Current Consumption

When migrating to an MSP430F23x/24x, the difference in current consumption of the devices should be considered. For example, in LFXT1 standby mode (LPM3 using a 32-kHz watch crystal), the standby current consumption of an MSP430F23x/24x is in the 1-µA range (typical data sheet value at 3 V, 25°C), which is much lower than the current consumption of an MSP430F13x/14x device, which is in the 1.6-µA range when performing the same function. This is a great benefit for applications that operate in standby mode most of the time. The devices' active current consumptions are comparable when operating at the same frequency, temperature, and voltage conditions. See the device-specific data sheets for the exact specifications. Note that when using LFXT1 in high-frequency mode or when using XT2, the current consumption component caused by the oscillator of an MSP430F23x/24x device is slightly higher as compared to an MSP430F13x/14x device, due to differences in the oscillator design to support higher frequencies.

One additional point the designer should be aware of is that, when taking advantage of the increased maximum operating frequency the MSP430F23x/24x offers, additional current must be supplied by the system's power supply, because active-mode current consumption scales linearly with operating frequency.

2.3 Operating Frequency Versus Supply Voltage

For the MSP430, the maximum frequency at which the CPU can operate depends on the supply voltage. This specification can be found in the *recommended operating conditions* of each MSP430 data sheet. In general, it can be said that this specification differs for the MSP430F13x/14x and MSP430F23x/24x families of microcontrollers. However, an MSP430F23x/24x device can always operate under the same operating conditions in terms of supply voltage and CPU clock frequency (MCLK) as an MSP430F13x/14x device. If a designer who migrates an existing design to an MSP430F23x/24x device wants to take advantage of the increased maximum clock frequency, it is important to closely review the *recommended operating conditions* in the MSP430F23x/24x device data sheet. [4]

It is of extreme importance that this relationship is also observed during power-ramp scenarios. Violating this maximum frequency versus voltage dependency can result in unpredictable code execution. Note that MSP430F23x/24x MCUs have a built-in SVS module that can be used to ensure that this operating condition is not violated.

2.4 Device Errata

In the course of migrating an existing application to the MSP430F23x/24x, it is recommended to review and carefully consider the latest device errata sheets to ensure the application is not affected by a known device issue. Furthermore, the errata sheets typically outline workarounds along with the bug descriptions. For all MSP430 products, the device errata sheets can be found in the product folders of each product on the MSP430 web page (www.msp430.com).

3 MSP430F13x/14x to MSP430F23x/24x Migration – Firmware Considerations

This section outlines important steps to consider when transition existing software routines or an entire application to an MSP430F23x/24x device. Even though MSP430F13x/14x and MSP430F23x/24x are code compatible and share many of the same peripherals, in many cases, migration is not as simple as programming the MSP430F13x/14x binary image into an MSP430F23x/24x device. In general, an application should be rebuilt on a source-code level (including all referenced code libraries, etc.), using the appropriate MSP430F23x/24x device support files, such as the header file (msp430x24x.h) and the respective linker command file (lnk_msp430f249.cmd for TI Code Composer Essentials IDE or lnk430F249.xcl for IAR Embedded Workbench). Doing this is the first step toward a successful migration to an MSP430F23x/24x. The following sections provide more details regarding certain key aspects that should be considered.

3.1 Memory Considerations

3.1.1 Device Memory Map

The memory maps of the MSP430F13x/14x and MSP430F23x/24x are almost identical. This applies to the location and size of RAM as well as flash memory, allowing an application to keep the same linker command file during migration, in most cases. However, there are two exceptions that apply and, therefore, it is strongly recommended to rebuild the application to accommodate for the difference in the memory map. The build process makes use of the memory map information stored in the IDE linker command file and automatically accommodates these changes. The linker command files are found within the folder where the IDE was installed and have the file name extension CMD (for TI Code Composer Essentials) and XCL (for IAR Embedded Workbench).

The interrupt vector table of MSP430F23x/24x devices spans 32 memory word locations, whereas the table in MSP430F13x/14x devices spans 16 memory word locations. Furthermore, the word memory location 0xFFBE on MSP430F23x/24x devices is reserved for special bootstrap loader purposes. See Section 3.5 for more details regarding the interrupt vector table.

Furthermore, the MSP430F247(1) and MSP430F248(1) devices all have an increased RAM size of 4 KB compared to their MSP430F14x family counterparts. The application should be rebuilt to take advantage of this increased memory size. In addition, the MSP430F24x device family has a device with a memory configuration previously unavailable. The MSP430F2410 has 4 KB of RAM and 56 KB of flash memory. This device can be considered as an alternative migration option for applications that can benefit from having more RAM. Note that, in this case, the differences in memory organization are more drastic and the application code must be rebuilt in any case.

Further details regarding the device memory maps can be found in the device-specific data sheets. [3][4]

3.1.2 Information Flash Memory

Both MSP430F13x/14x and MSP430F23x/24x have 256 bytes of information flash memory located in the memory range of 0x1000 to 0x10FF. While the total memory size is the same, the memory is organized differently. The MSP430F13x/14x device information memory consists of two flash segments (INFOA and INFOB) that are 128 bytes each, whereas the MSP430F23x/24x has four segments (INFOA, INFOB, INFOC, and INFOD) that are 64 bytes each.

Applications storing data in the information memory need to consider the different segment sizes. Each information flash memory segment must be erased individually, resulting in four write accesses on an MSP430F23x/24x instead of two on the MSP430F13x/14x. Also, note that the MSP430F23x/24x INFOA segment is protected by a lock feature and requires special treatment to be erased or written to. However, in general, it is not recommended to erase INFOA or store any user data in it. INFOA comes with factory-provided device-specific calibration data, such as calibration to generate specific frequencies using the DCO. Chances are that an application can benefit from those constants.

See the *MSP430x2xx Family User's Guide* [2] for more details on the organization of the 2xx information flash memory, the INFOA lock feature, and the factory-provided calibration constants.

3.2 Serial Communication – USART Versus USCI

One of the major differences between MSP430F13x/14x and MSP430F23x/24x devices is the serial communication module. On the MSP430F23x/24x, the USCI module is implemented. It is the next-generation MSP430 communication module, offering more features and functionality to the user. USART (MSP430F13x/14x) and USCI modules are not software compatible and, therefore, MSP430F13x/14x software using the USART module needs to be adapted to make use of the USCI module.

The MSP430F24x features two independent and identical USCI modules, both of which provide two communication channels that operate simultaneously. With the MSP430F24x, for example, it is possible to service four SPI communication channels or two I^2C plus two UART channels, simultaneously. The MSP430F23x has one USCI module, providing two independent communication channels. Note that I^2C operation is a mode that was not available on MSP430F13x/14x devices.

It is not in the scope of this application report to discuss all possible aspects regarding migrating application code to use the USCI interface; however, a few items are outlined to highlight major differences between the devices (and the modules). In general, it is strongly recommended to carefully review both module descriptions in the appropriate device family user's guide [1][2], as well as to use the USCI code examples provided in the product folders on the MSP430 web page (www.msp430.com) as a starting point for any code that is newly created.

3.2.1 UART Mode

The operation of the MSP430F23x/24x USCI in UART mode and that of the MSP430F13x/14x USART are almost identical. The major differences are:

- The MSP430F23x/24x USCI uses a different baud rate generator. It utilizes a new modulation scheme, provides a two-stage modulator, and can be used to implement an oversampling baud rate generation scheme. During application migration, the baud rate register settings need to be recalculated. However, it is safe to say that the USCI module can be used to generate the same target baud rate using the same clock source that the MSP430F13x/14x USART would be able to provide.
- The start edge detection and clock activation schemes are different on the two devices. The MSP430F23x/24x features a simplified scheme whereby the USCI module automatically activates the USCI module clock source upon start edge detection and then provides an interrupt to wake up the CPU after the entire character has been received. On the MSP430F13x/14x UART, an interrupt is generated directly upon start edge detection, the application needs to handle the clock source activation itself, and then, as a second step, the character reception.
- On the MSP430F23x/24x USCI, interrupt flags are no longer cleared automatically upon entering the interrupt service routine.

3.2.2 SPI Mode

The operation of the MSP430F23x/24x USCI in SPI mode and the MSP430F13x/14x USART is almost identical. The major differences are:

- The MSP430F14x USART supports two channels of simultaneous SPI communication (USART0 and USART1), whereas the MSP430F24x USCI supports four channels (USCI_A0, USCI_B0, USCI_A1, and USCI_B1).
- The MSP430F13x USART supports one channel of SPI communication (USART0), whereas the MSP430F23x USCI supports two channels (USCI_A0 and USCI_B0).
- On the MSP430F14x, each of the four SPI communication endpoints has a dedicated interrupt vector. On the MSP430F24x, each USCI module has a two shared interrupt vectors, combining transmit and receive events for each module. On both devices, four interrupt vectors are available in total.
- On the MSP430F13x and on the MSP430F23x, each SPI communication endpoint has a dedicated interrupt vector. On both devices, two interrupt vectors are available in total.
- On the MSP430F23x/24x USCI, interrupt flags are no longer cleared automatically upon entering the interrupt service routine.
- The MSP430F23x/24x USCI defaults to an LSB-first SPI bit order. The bit order can be configured with the UCMSB bit in the UCAxCTL0/UCBxCTL0 control registers. This is different from the UART module, where the bit order is MSB first and cannot be configured.
- The maximum MSP430F23x/24x USCI bit clock frequency in SPI master mode is BRCLK, whereas on the MSP430F13x/14x USART module it is BRCLK/2.

3.3 Clock System

3.3.1 LFXT1 and XT2 Oscillators

The MSP430F23x/24x oscillator blocks supersede the ones found on MSP430F13x/14x devices. The MSP430F23x/24x oscillators can operate with the same low- and high-frequency oscillators and clock sources, but they consume less power while providing increased robustness. In addition, built-in software-configurable crystal load capacitors are provided in low-frequency (LF) mode. The power-on default for the effective load capacitance in LF mode is 6 pF, which is in line with the MSP430F13x/14x LF oscillator.

When migrating designs that use external crystals or clock sources, items to keep in mind are:

- The capability of MSP430F23x/24x devices to detect low-frequency oscillator failures and indicate them by setting the LFXT1OF flag results in another path for the global oscillator fault flag (OFIFG) to become set. This may prevent the CPU from being clocked by a crystal or an external clock source in certain scenarios.
- If the existing MSP430F13x/14x design uses an external 32-kHz crystal for low-power mode operation and periodic wakeup (LPM3), and crystal-accurate precision is not required, the MSP430F23x/24x built-in VLO oscillator can be used instead, resulting in the elimination of the external crystal and a reduced LPM3 power consumption. The VLO frequency is 12 kHz (data sheet typical value) but can be measured and virtually calibrated. For more details, see reference [5].
- If an external digital clock source is used, the MSP430F23x/24x newly available direct digital clock input mode should be used (by setting the LFXT1S1 and LFXT1S0 control bits).
- If the existing MSP430F13x/14x design uses a high-frequency crystal or resonator on LFXT1 or XT2, the appropriate frequency range must be configured in the MSP430F23x/24x clock system control register BCSCTL3. The default range setting is for use with 0.4-MHz to 1-MHz crystals or resonators. See the Basic Clock Module+ user's guide chapter for further details. [2]

3.3.2 Digitally Controlled Oscillator (DCO)

The MSP430F13x/14x and MSP430F23x/24x have different DCO modules. The MSP430F23x/24x DCO offers higher accuracy, an extended frequency range allowing operation of the device up to the maximum operating frequency, and factory-provided calibration constants to facilitate the design of systems that operate without external clock sources.

The key points that should be considered during migration are:

- The default DCO frequency of an MSP430F13x/14x device is in the 800-kHz range, but it is in the 1.2-MHz range for an MSP430F23x/24x device. This needs to be considered for applications that run the device using the default DCO settings.
- On an MSP430F23x/24x, consider loading any of the factory-provided DCO calibration constants into the DCO to achieve a deterministic and stable output frequency. The use of the DCO calibration constants may omit the need for software-FLL algorithms used on an MSP430F13x/14x device in combination with an external clock source to derive a stable high-speed system clock.
- The MSP430F13x/14x has three bits to control the fundamental frequency range (RSELx in the BCSCTL1 register), whereas the MSP430F23x/24x has four control bits. Care must be taken when porting algorithms such as a software FLL that modify these bits.
- If an MSP430F13/14x application applies hard-coded DCOx, MODx, and RSELx values to the DCO control registers, this results in a different frequency range on an MSP430F23x/24x.
- When enabling the external resistor DCO bias feature (by setting DCOR in the BCSCTL2 register), the MSP430F23x/24x DCO starts behaving like an MSP430F13x/14x DCO. In this mode, the same bit settings and external bias resistors result in the same frequency being generated. See the device-specific data sheets for further details. [3][4]

3.4 Bootstrap Loader (BSL)

MSP430F23x/24x devices have a new BSL firmware with enhanced security features. Both MSP430F13x/14x and MSP430F23x/24x device memory access is protected by a 256-bit password. However, only MSP430F23x/24x devices erase the entire device flash memory contents (including the factory-provided calibration constants stored in the INFOA flash segment) on the first attempt to access the device with an incorrect password. This behavior is configurable and needs to be considered for applications that use the BSL interface to provide in-field software upgrade capability.

3.5 Interrupt Vectors

The interrupt vector arrangement of MSP430F13x/14x and MSP430F23x/24x devices are different, and application code using interrupt-controlled program flow needs to be migrated. Migrating to an MSP430F23x/24x device involves making sure that the new interrupt vector locations are used. See Table 2 for a list of module-associated interrupt vectors that require attention.

Table 2. Changed Interrupt Vector Locations

Module	MSP430F13x/14x	MSP430F23x/24x	Comments
Timer_A3	0xFFEA, 0xFFEC	0xFFF0, 0xFFF2	
ADC12	0xFFEE	0xFFEA	
Port 1	0xFFE8	0xFFE4	
Port 2	0xFFE2	0xFFE6	
USART0, USCI_A0/B0	0xFFF0, 0xFFF2	0xFFEC, 0xFFEE	The USCI interrupt vectors are multiplexed between RX, TX, I2C Data and I2C Status events.
USART1, USCI_A1/B1	0xFFE4, 0xFFE6	0xFFE0, 0xFFE2	

In general, recompiling the MSP430F13x/14x application code using MSP430F23x/24x device support files automatically takes care of populating the interrupt vector table according to the device-specific requirements (for example, for Timer_A, ADC12, etc.). However, in some cases, the interrupt vector routines themselves also need to be modified to accommodate a different interrupt flag demultiplexing scheme (USART versus USCI).

Also, the memory range that is reserved for interrupt vectors (interrupt vector table) differs between MSP430F13x/14x and MSP430F23x/24x devices. For MSP430F13x/14x devices, this memory ranges from address 0xFFE0 to 0xFFFF (16 words), whereas for MSP430F23x/24x devices, it ranges from 0xFFC0 to 0xFFFF (32 words). In addition to this, the word memory location 0xFFBE is reserved on MSP430F23x/24x devices and used as the BSL security key (see Section 3.4).

3.6 Beware of Reserved Bits!

The MSP430F23x/24x features a range of upgraded peripherals as compared to the MSP430F13x/14x, such as the BCS+ and the Comparator+. This added functionality is partially achieved through the use of bits which were previously marked "reserved" on the corresponding MSP430F1xx peripheral. Newer generation MSP430s such as the MSP430F23x/24x make use of these bits to implement additional functionality. If left in the default state, the peripheral usually behaves the same as its MSP430F1xx counterpart. However care must be taken to not unintentionally switch some of these bits, which can be caused by migrated MSP430F13x/14x firmware. For example, consider the following comparison of CACTL2 control register of Comparator_A and Comparator_A+:

7	6	5	4	3	2	1	0
Unused				P2CA1	P2CA0	CAF	CAOUT
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	r-(0)

Figure 1. CACTL2 Bit Description, 1xx Devices

7	6	5	4	3	2	1	0
CASHORT	P2CA4	P2CA3	P2CA2	P2CA1	P2CA0	CAF	CAOUT
rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	rw-(0)	r-(0)

Figure 2. CACTL2 Bit Description, 2xx Devices

When firmware that uses the comparator module sets bit 7 and runs fine on an MSP430F14x is executed on an MSP430F24x device, it results in the comparator inputs being shorted together internally.

3.7 Timers

An undocumented feature on the MSP430F13x/14x allows the Timer_A and Timer_B modules to be used in capture mode to generate interrupts on input signal transitions with the timer in stop mode (MCx in TACTL/TBCTL is set to 00h). This feature is no longer available on MSP430F23x/24x devices. To generate capture interrupts, the respective MSP430F23x/24x timer must be running. In this specific use case, consider clocking the timer using a low frequency (e.g., ACLK) to minimize power consumption.

3.8 Analog Comparator

On the Comparator_A of MSP430F13x/14x devices, disabling the digital port functionality for an I/O pin by setting the associated bit in the Port Disable Register CAPD to prevent parasitic cross currents during analog measurements disables the digital CMOS input buffer. However, on MSP430F23x/24x devices with Comparator_A+, setting a CAPDx bit disables both input and output buffer for that pin.

4 References

1. *MSP430x1xx Family User’s Guide* (SLAU049)
2. *MSP430x2xx Family User’s Guide* (SLAU144)
3. MSP430x13x, MSP430x14x, MSP430x14x1 data sheet (SLAS272)
4. MSP430x23x, MSP430x24x(1), MSP430x2410 data sheet (SLAS547)
5. *Using the VLO Library* (SLAA340)