Introduction
Power sequencing is an essential part of many electronic designs including systems with high-performance processing devices such as FPGAs, ASICs, PLDs, DSPs, ADCs, and microcontrollers (MCU). These types of applications require specific voltage rail power-up and power-down sequencing to guarantee reliable operation, better efficiency, and overall system health. The MSP430FR2000 MCU is an ultra-low-power device that provides an elegant and cost-effective solution using only 512 bytes of nonvolatile ferroelectric random access memory (FRAM). The device’s extensive low-power modes enable a current draw of 0.5 µA when waiting on a rail power-up signal and 3.5 µA when waiting on a rail power-down signal. The design also takes advantage of the Timer_B peripheral within the MSP430™ MCU to provide a programmable sequencing delay for up to eleven output flags. To get started, download project files and a code example demonstrating this functionality.

Implementation
Several GPIOs on the MSP430FR2000 provide interrupt capabilities that can wake the device from low-power modes. Using this functionality allows the MSP430 MCU to spend most of its time in LPM4, waiting on the appropriate signal to start either a power-up or power-down sequence on the output rails. The MCU then starts the Timer_B peripheral, which provides precise timing for the output signal and controls the output flags through an interrupt-based approach. This interrupt-centric design allows for lower current consumption and more precise timing of the output flags. Figure 1 shows the inputs and outputs of the simple power sequencer example code provided with this document.

TI recommends using an external 32.768-kHz crystal to source Timer_B, but the internal reference oscillator (REFO) can be used with the trade-off of higher current consumption.

After a device reset, the simple power sequencer initializes all GPIO to output low. This configuration enables the MSP430 MCU to achieve the lowest possible power consumption. If the power sequencer is using an external crystal, pins 2.6 and 2.7 are not configured as outputs but instead setup for crystal operation. Additionally, P1.0 is configured as an input that will trigger an interrupt on a rising edge.

After initializing the GPIO accordingly, the power sequencer initializes the Timer_B peripheral. This peripheral is used to create the precise time delays between an event on the EN pin and the subsequent response on the FLAGx output. The delay is user configurable and can be easily changed in the example code by modifying the RAIL_DELAY definition at the beginning of code. Note that there is only one RAIL_DELAY variable defining the delay between consecutive output flag level changes. Equation 1 shows how to calculate the value of RAIL_DELAY for your application.

\[
\text{RAIL\_DELAY} = 32768 \times \text{DELAY} \quad (1)
\]

The Timer_B peripheral is sourced from the ACLK which is then sourced from either the REFO or the external 32.768kHz crystal. The user can choose whether to use the internal REFO or external crystal by modifying the USE_REFO definition in the example code provided. ACLK is not active in LPM4 on most MSP430 devices. Therefore, the device operates in LPM3 when Timer_B is being used to create the required delays.

Finally, after initializing the GPIO and Timer_B, the power sequencer enters LPM4 with global interrupts enabled. In this state the device is waiting on a rising edge on the EN pin which will kick-off a power-up sequence on the output rails. When the rising edge is seen, the device wakes from LPM4 and enters the pin 1 interrupt service routine. From there, Timer_B starts counting and either the power-up or power-down sequence is selected.

When Timer_B counts to the RAIL_DELAY value, an interrupt is triggered and the TB0.0 interrupt service routine is entered. From there, the current output flag is toggled and the code then points to the next flag or stops the timer if the end of the sequence is reached. There are two sets of flags setup in a linked list.
structure. One linked list is for the power-up sequence and the other is for the power-down sequence. Each node in the list contains the port bit that corresponds to the individual flag and a pointer to the next flag in the sequence. The last node in the sequence contains a NULL pointer signifying that the end of sequence was reached. This structure makes adding or removing flags from the sequence simple and quick while maintaining a small code footprint.

Performance

The firmware written for this application was optimized for use on the MSP430FR2000 and was tested with the MSP-TS430PW20 target board. The same code can be modified to work on any MSP430 device with a Timer peripheral. Figure 2 shows an example of the current profile for the example code provided with this document and Table 1 describes the device operation during each power sequencing state.

There are four basic states throughout operation of the simple power sequencer. Each state operates in either LPM3 or LPM4 with several occurrences where the device enters active mode to service interrupts. The current consumption shown in Figure 2 is based on the specifications in the MSP430FR21xx, MSP430FR2000 Mixed-Signal Microcontrollers data sheet. If using a different device variant, see that device data sheet for more accurate current consumption values.

Additionally, there is a minimum delay between the EN signal and the first flag output determined by the wake-up time from LPM4 + interrupt latency of 6 MCLK cycles. A similar minimum delay exists between consecutive output flags determined by wake-up time from LPM3 + 6 MCLK cycles. For more information on LPM wake-up times, see the device-specific data sheet.

![Figure 2. Example Sequence Profile](image)

**Table 1. Explanation of Power Sequencing States**

<table>
<thead>
<tr>
<th>State</th>
<th>Description</th>
<th>Cause of Entry</th>
<th>Current Consumption</th>
</tr>
</thead>
<tbody>
<tr>
<td>State 0</td>
<td>Device operates in LPM4 waiting on a rising edge on EN pin</td>
<td>Device power up or Falling edge last flag in power-down sequence</td>
<td>LPM4 including SVS</td>
</tr>
<tr>
<td>State 1</td>
<td>Device operates in LPM3 while counting delay for output flag power-up sequence</td>
<td>Rising edge on EN</td>
<td>LPM3 including SVS + REFO (optional) + EN pulldown</td>
</tr>
<tr>
<td>State 2</td>
<td>Device operates in LPM4 while holding the output flags high</td>
<td>Rising edge on last flag of power-up sequence</td>
<td>LPM4 including SVS + EN pulldown</td>
</tr>
<tr>
<td>State 3</td>
<td>Device operates in LPM3 while counting delay for output flag power-down sequence</td>
<td>Falling edge on EN</td>
<td>LPM3 including SVS + REFO (optional)</td>
</tr>
</tbody>
</table>

**Device Recommendations**

The device used in this example is part of the MSP430 Value Line Sensing portfolio of low-cost MCUs, designed for sensing and measurement applications. This example can be used with the devices shown in Table 2 with minimal code changes. For more information on the entire Value Line Sensing MCU portfolio, visit www.ti.com/MSP430ValueLine.

**Table 2. Device Recommendations**

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Key Features</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSP430FR2000</td>
<td>0.5KB FRAM, 0.5KB RAM, eComp</td>
</tr>
<tr>
<td>MSP430FR2100</td>
<td>1KB FRAM, 0.5KB RAM, 10-bit ADC, eComp</td>
</tr>
<tr>
<td>MSP430FR2110</td>
<td>2KB FRAM, 1KB RAM, 10-bit ADC, eComp</td>
</tr>
<tr>
<td>MSP430FR2111</td>
<td>3.75KB FRAM, 1KB RAM, 10-bit ADC, eComp</td>
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</table>
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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
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