PGA900 as a Capacitive Load Driver

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ABSTRACT

Capacitive load drive is one of the most common causes of operational amplifier stability issues. The load capacitance, \( C_L \), interacts with the open-loop output impedance of the amplifier, \( Z_O \), by adding a single or double pole in the open-loop response. The additional pole or poles degrades the circuit phase margin, resulting in transient overshoot and ringing, ac gain peaking, reduced bandwidth, and possibly full oscillations. Therefore, the design requires phase compensation to stabilize the circuit so it produces an optimal output response. Finding the open-loop output impedance lets the designer select compensation components for occasions when the PGA900 DAC gain output is used as a capacitive load driver.

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1 Introduction

Capacitive load drive is one of the most common causes of operational amplifier stability issues. The load capacitance, \( C_L \), interacts with the open-loop output impedance of the amplifier, \( Z_O \), by adding a single or double pole in the open-loop response. The additional pole or poles degrades the circuit phase margin, resulting in transient overshoot and ringing, ac gain peaking, reduced bandwidth, and possibly full oscillations. Therefore, the design requires phase compensation to stabilize the circuit so it produces an optimal output response.

One way to stabilize an operational amplifier circuit for capacitive load drive is to add a resistor, \( R_{ISO} \), between the amplifier’s output and \( C_L \). As this added resistor is outside the feedback path, this method is known as out-of-loop compensation. \( R_{ISO} \) acts with \( C_L \) and introduces a zero into the transfer function to cancel the phase shift from the poles caused by \( Z_O \) and \( C_L \). The addition of the zero in the transfer function returns the phase margin to a stable level.

However, the \( R_{ISO} \) circuit suffers from accuracy issues when the amplifier is required to drive current due to the voltage drop formed across \( R_{ISO} \). The errors could be corrected if the load is known and constant, but in cases when the circuit load is unknown or dynamic, move \( R_{ISO} \) inside the overall feedback path (see Figure 1). This configuration is known as in-loop compensation. In this configuration, dc and low-frequency feedback is provided from the load through \( R_F \), restoring the dc and low-frequency accuracy of the circuit. Feedback capacitor, \( C_F \), provides a high-frequency feedback path (\( FB_2 \)) to bypass the feedback path formed from \( R_{ISO} \), \( C_{LOAD} \), and \( R_F \) (\( FB_1 \)). This compensation method permits stable drive of any amount of capacitance load.

![Figure 1. In-Loop Compensation: Circuit for Capacitive Load Drive](image-url)
2 Selecting Compensation Components

As shown in Figure 2, the PGA900 DAC output amplifier, $Z_o$, displays complex frequency behavior. In the frequency range from DC up to amplifier bandwidth, $Z_o$ behaves as a resistor, capacitor, and inductor. If $Z_o$ is plotted with the different capacitance loads from 1 nF to 470 nF, intersections occur in the region where $Z_o$ behaves as an inductor.

![Figure 2. PGA900 Open-Loop Output Impedance $Z_o$ and Capacitors Load Impedance $Z_C$ Over Frequency](image)

For stability analysis, replace $Z_o$ with an equivalent open-loop output inductance, $L_o = 1.2294$ mH. By adding the isolating resistor, $R_{ISO}$, between the output of the amplifier (or $L_o$) and the load capacitance, $C_L$, the interaction results in the addition of a double pole, $f_p$, and a zero, $f_z$, to the unloaded open-loop gain, $A_{OL}$. To maximize bandwidth and limit the feedback loop phase-shift at high frequencies to 90°, select $R_{ISO}$ so that $f_p = f_z$. Using this criteria, calculate $R_{ISO}$ with Equation 1.

$$R_{ISO} = \sqrt{\frac{L_o}{C_L}}$$  \hspace{1cm} (1)

The feedback path through $C_F$ ($FB_2$) becomes the dominate feedback in the circuit after the frequency: $f_p' = \frac{1}{2 \pi} \times (R_{ISO} + R_F) \times C_F$. $FB_2$ must be designed so it is the dominate feedback path before $FB_1$ begins to compromise the circuit stability. Transferring feedback control to the bypass loop removes the second-pole effects from the new controlling feedback, which preserves stability. For the system to have the fastest response (fastest approach to the final value) possible without overshoot, select damping factor $\zeta = 1$. By definition, this system is critically damped. Therefore, the designer can calculate that $f_p' \leq \frac{1}{4} f_p$. To satisfy this condition, calculate the value of the feedback capacitor with Equation 2.

$$C_F = \frac{4 \times R_{ISO} \times C_L}{R_{ISO} + R_F}$$  \hspace{1cm} (2)
3 PGA900 Compensation Components for Different $C_L$

PGA900 DAC gain stage has four fixed-gain selections: 2 V/V, 4 V/V, 6.67 V/V, and 10 V/V. These gain selections result in the feedback resistor values of 75 kΩ, 112.5 kΩ, 127.5 kΩ, and 135 kΩ, respectively. Figure 3 shows the PGA900 internal circuitry for a gain selection of X V/V.

Figure 3. PGA900 Gain Selection Circuit With Capacitive Load Compensation
Using the previous procedure, select decoupling components $R_{ISO}$ and $C_F$ for different capacitive loads and gains. Table 1 to Table 4 show decoupling components that provide the highest bandwidth (BW) for 1-nF, 10-nF, 100-nF, and 470-nF capacitive loads, respectively.

Table 1. PGA900 Decoupling Components for 1-nF Capacitive Load

<table>
<thead>
<tr>
<th>$C_L$ (nF)</th>
<th>$R_{ISO}$ (Ω)</th>
<th>Gain (V/V)</th>
<th>$R_F$ (kΩ)</th>
<th>$C_F$ (pF)</th>
<th>BW (kHz)</th>
</tr>
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<tbody>
<tr>
<td>1</td>
<td>1100</td>
<td>2</td>
<td>75</td>
<td>56</td>
<td>37.3</td>
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<tr>
<td>1</td>
<td>1100</td>
<td>6.67</td>
<td>127.5</td>
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<td>33</td>
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Table 2. PGA900 Decoupling Components for 10-nF Capacitive Load

<table>
<thead>
<tr>
<th>$C_L$ (nF)</th>
<th>$R_{ISO}$ (Ω)</th>
<th>Gain (V/V)</th>
<th>$R_F$ (kΩ)</th>
<th>$C_F$ (pF)</th>
<th>BW (kHz)</th>
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<tbody>
<tr>
<td>10</td>
<td>348</td>
<td>2</td>
<td>75</td>
<td>180</td>
<td>11.7</td>
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<tr>
<td>10</td>
<td>348</td>
<td>6.67</td>
<td>127.5</td>
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<td>11.8</td>
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<tr>
<td>10</td>
<td>348</td>
<td>10</td>
<td>135</td>
<td>100</td>
<td>11.8</td>
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Table 3. PGA900 Decoupling Components for 100-nF Capacitive Load

<table>
<thead>
<tr>
<th>$C_L$ (nF)</th>
<th>$R_{ISO}$ (Ω)</th>
<th>Gain (V/V)</th>
<th>$R_F$ (kΩ)</th>
<th>$C_F$ (pF)</th>
<th>BW (kHz)</th>
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<tbody>
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<td>100</td>
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<td>2</td>
<td>75</td>
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<tr>
<td>100</td>
<td>110</td>
<td>6.67</td>
<td>127.5</td>
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<tr>
<td>100</td>
<td>110</td>
<td>10</td>
<td>135</td>
<td>330</td>
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Table 4. PGA900 Decoupling Components for 470-nF Capacitive Load

<table>
<thead>
<tr>
<th>$C_L$ (nF)</th>
<th>$R_{ISO}$ (Ω)</th>
<th>Gain (V/V)</th>
<th>$R_F$ (kΩ)</th>
<th>$C_F$ (pF)</th>
<th>BW (kHz)</th>
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<tbody>
<tr>
<td>470</td>
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<tr>
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<td>135</td>
<td>680</td>
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Using values from Table 3 for a 100-nF capacitive load, small signal and large signal step response measurements were taken to verify stable circuit transient behavior. Figure 4 to Figure 11 show the results of these measurements. As predicted, all of these responses have similar response, critically damped, fast settling without overshoot.
4 Conclusion

Finding the open-loop output impedance lets the designer select compensation components for occasions when the PGA900 DAC gain output is used as a capacitive load driver. The component selection maximizes bandwidth and phase margin of the system for a specific capacitive load. Keeping the system response critically damped obtains the fastest output signal settling without overshoot. It is the designer's responsibility to adjust component values to ensure desired operation over the temperature range and the initial and life tolerances of the component.

5 References

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