

Empowering Designs With Power Management IC (PMIC) for Processor Applications

Bhaskar Ramachandran and Sanjay Singh

Integrated Power Group

ABSTRACT

As systems continue to shrink in both size and power usage while simultaneously growing in functionality, designers continuously face the challenge of how to efficiently power the systems. Whether battery-powered or connected to a main power supply, the increased capabilities in processing technology, input/output (IO), and connectivity require changes to the system design to effectively deliver power and optimize the overall efficiency of the system.

Historically, when systems were simpler, the various voltage rails and current levels required by the processor and its peripherals were supplied by a handful of discrete power-regulator integrated circuits (ICs). The application processor was directly involved in powering up and powering down these discrete regulators, and also handled the sequencing and different power states within the system. Today however, advanced embedded systems and processors require controlled and choreographed sequencing of the various power domains.

Today's embedded and processor systems require individual control of the various power domains to selectively turn off circuits in sleep and low-power modes for conservation of battery charge. Tasking the application processor with this power sequencing and control wastes processing resources while increasing the system software complexity, and it is not always possible because new processors require more complex powering sequences before they can begin code execution.

This application report outlines the need for a highly programmable and reconfigurable power management IC (PMIC) to address the power-management challenges, and the document explains how a PMIC for a processor platform is the most effective way to deal with this challenge.

Contents

1	Cost.....	2
2	Area.....	2
3	Flexibility and Performance.....	3
4	Integration.....	4
5	External Event Detection	4
6	Power-Up and Power-Down Sequencing.....	5
7	System Monitor and Fault Handling	5
8	Summary.....	6
9	References and Related Documentation	6

1 Cost

For many projects when selecting a power solution, the primary criteria is the *cost* of the processor system. For some, system performance is only a secondary concern. Using a PMIC helps reduce the overall cost of ownership while still maintaining the best possible system performance. This may seem counter intuitive given that discrete power regulators are usually offered at very low cost, due to their wide application and market base. However, with all the discrete power ICs required for the system, the external passives, the glue logic required for sequencing, enable and disable functions, the cost of manufacturing, assembly, and inventory are added together, the PMIC-based system design ends up offering a lower-cost solution with minimal external components.

There are several low-end discrete components that are available in the market, but the performance and added solution can lower overall system value and performance. Adding to the cost of the components are the additional hidden costs of debugging issues in a system with more components, the amount of engineering effort required by both hardware and software designers, and the time-to-market. As a cost factor, a PMIC clearly offers a cost-competitive system solution.

Table 1. PMIC Comparison Against Discrete Solutions

Features	High-End Discrete	Low-End Discrete	PMIC
Solution size	Large	Large	Smaller
Performance	Best	Worst	Competitive
Cost	\$\$\$	\$	\$\$

2 Area

As systems adopt modern processors with complex power requirements and continue to add more peripherals that bring additional voltage-rail requirements and output needs, the device-packing density gets extremely high and PCB real estate is at a prime. Additionally, for battery-powered systems, the battery-pack size must also grow larger to support these features with a reasonable recharge rate, which further reduces the space available for the electronics.

Thanks to the continued miniaturization of IC technology and the ability to integrate multiple functions into a single IC, system architects are able to meet these demands with highly integrated system-on-chip (SoC) ICs, thereby solving the problem of providing multiple features in a small real estate. As the miniaturization trend continues, the ultra-small channel-length transistors and very low-voltage ratings are no longer suitable to process and manage power on chip.

The power management circuits usually must interface directly with the power supply, and the process technology required to build high-efficiency power switches are not compatible with the process technology conducive to SoC. This necessitates a separate PMIC capable of working in tandem with the SoC. As it is true with the SoC integration, the real estate needed for the integrated power solution in a PMIC goes down significantly compared to a discrete offering.

In the discrete solution, each power regulator IC requires its own dedicated band-gap reference, low-dropout (LDO) regulator for biasing internal control circuits, dedicated comparators and logic, and so on. With a PMIC, these auxiliary building blocks, such as reference, bias supplies and many others can be shared for the multiple integrated power regulators saving significant area.

The PMIC advantage is obvious due to having additional package area included along with reserved area for component placement and soldering each discrete power regulator. Another significant area of savings comes from the ability to have on-chip digital logic. Using on-chip digital logic supports various supply sequencing requirements and glue logic necessary to control the power regulators in a PMIC versus a discrete implementation with on-board glue logic and passives to provide a similar system sequencing and control.

Figure 1 shows an example of a power system for an SoC. Discrete solutions require external components such as comparators, voltage references, and so on. A PMIC integrates everything needed to perform these functions, such as sequencing. Figure 1 also shows an example of space saving (IC only) for a PMIC solution.

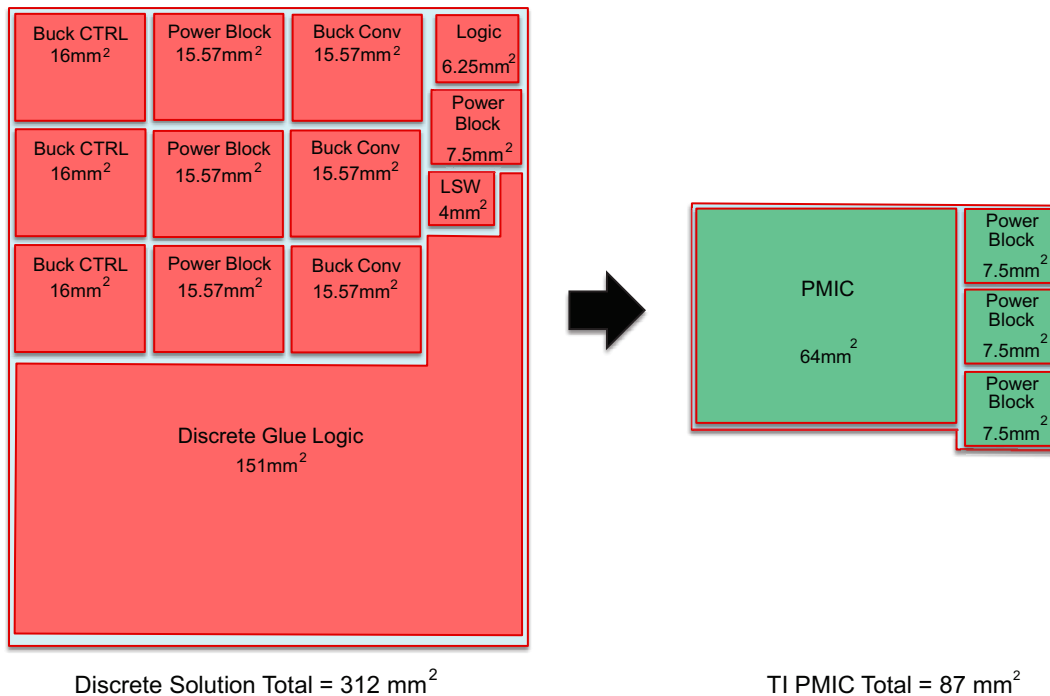


Figure 1. Total Solution Size for PMIC Versus a Discrete Power Implementation

3 Flexibility and Performance

The discrete solution is generally perceived as a solution with greater flexibility because power rails can be easily added or removed from the design at any time during the platform-development phase. Also, because the individual rails can be easily optimized for efficiency by picking the right discrete solution for the operating voltage and current, proponents of discrete power solutions argue that the discrete power offers the best performance as well.

It is true that there is some amount of flexibility and the opportunity to optimize the efficiency of individual power rails by choosing the right discrete ICs, but it should also be kept in mind that such an exercise of optimizing the system performance and providing flexible power rail voltage and current options also goes into designing a PMIC. In fact, these design tradeoffs are carefully thought through during the PMIC definition and design phase, which saves the time and effort for the platform systems engineer making these decisions during the limited time available for platform development.

IC vendors offer a wide portfolio of PMICs for the same application so that a specific PMIC with the desirable feature set can be married to a processor system, thus providing the best possible efficiency and performance. For instance, Texas Instruments offers multiple PMICs such as the TPS65218, TPS65023, and TPS650860 devices, and even more for the FPGA processor platforms. Furthermore, in the case where additional power outputs are required above what a PMIC can provide, it is still possible to supplement the PMIC solution with discrete solutions, which allows for simplification of a large part of the system while still maintaining flexibility in the number of outputs required.

When a suitable PMIC is found to meet the system needs, the PMIC offers many performance benefits that are unique to the integrated solution and cannot be obtained through any discrete power solution. For example, the PMIC is able to achieve very low supply quiescent currents (IDDQ) for the system due to the shared bias and control lines in addition to the ease of ability to control the various power rails within the PMIC.

Also, because the processor has multiple power modes of operation, the rail voltage to processor and other subsystems can be scaled back or even turned off during different system power modes to save power dissipation and improve thermal output. Many PMICs offer dynamic voltage scaling (DVS) and decay modes for their rails to support these system power modes, thereby achieving the highest possible system efficiency. For example, the TPS65218 device is a PMIC suitable for processor power providing very low IQ during low-power modes. The TPS650860 device also offers very wide voltage range DVS capability and supports decay-mode for all the switched-mode power rails.

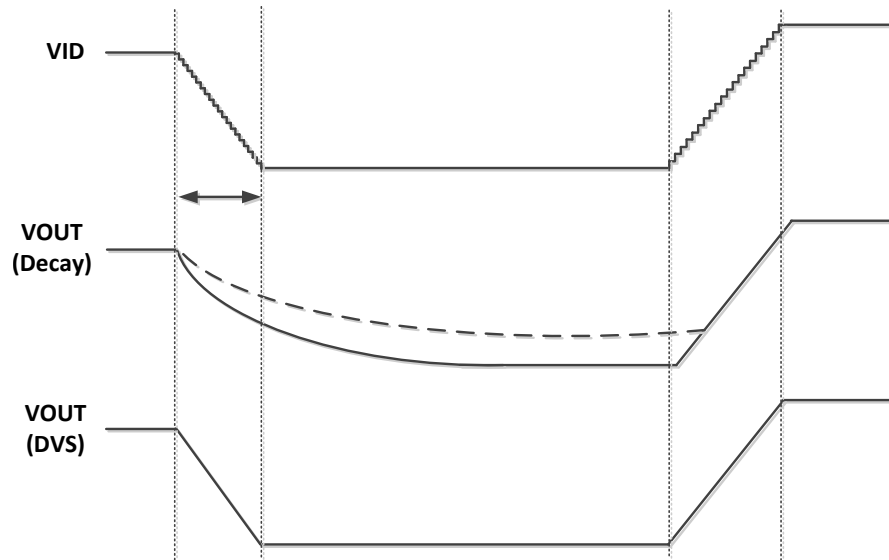


Figure 2. Example of a DVS and Decay-Mode Timing Diagram

Implementing such features in a discrete solution is usually challenging as it requires routing many on-board signals to the various discrete rails to convey the system states. Or, it may rely on firmware to send commands through the I2C interface to various discrete power ICs to implement DVS and decay modes, which is very slow and creates difficulty with system timing and sequencing. By combining the power control into a single IC, the system software requirements are further reduced by allowing the power control to be centralized into a single driver rather than individual small drivers for each component. This combination also reduces the need to run communication signals, such as I2C to multiple devices, by providing the control on a single I2C bus.

4 Integration

One of the greatest values of using a PMIC in any type of ARM, x86, FPGA, or microcontroller-based system is the high level of integration. These PMICs offload supervisory tasks from the SoC like power-up and power-down sequencing, on/off control, fault handling, reset, and power good. These tasks are usually done in software performed by the SoC. This integration takes a load off the SoC, decreases the amount of external ICs and components needed, in addition to decreasing the software complexity of the system.

5 External Event Detection

Most systems rely on some external events (for example: pushbutton press, AC, USB, battery-power application, GPIO assertions in mobile, industrial, and automotive applications) to wake up the system or events like pushbutton press-to-power cycle or AC, USB, or battery removal to reset or reboot the system. A PMIC can detect these events and wake up the system or interrupt the main application processor in the system to start controlling.

6 Power-Up and Power-Down Sequencing

Power-up and power-down control are particularly important for the application processor because multiple blocks have critical timing dependencies. Intelligent power management must also handle the increasing numbers channels. The sequence-up phase is initiated by external events or processor command through GPIO or I2C communication. The controlled supplies sequence-up with user-configured order of rails and inter-rail delays.

All supplies must exceed a user-defined sequence-up threshold within the configured power-good timer time out. If any supply fails to turn on properly, a sequence fault occurs, and all controlled supplies are shut down. When all supplies reach their sequence-up threshold, the supply monitor begins. PMICs integrate the power sequencing into their digital core. Having this integration removes the need for an external microcontroller and comparator logic to control the sequencing for the system; in turn this saves time, cost, complexity, and space.

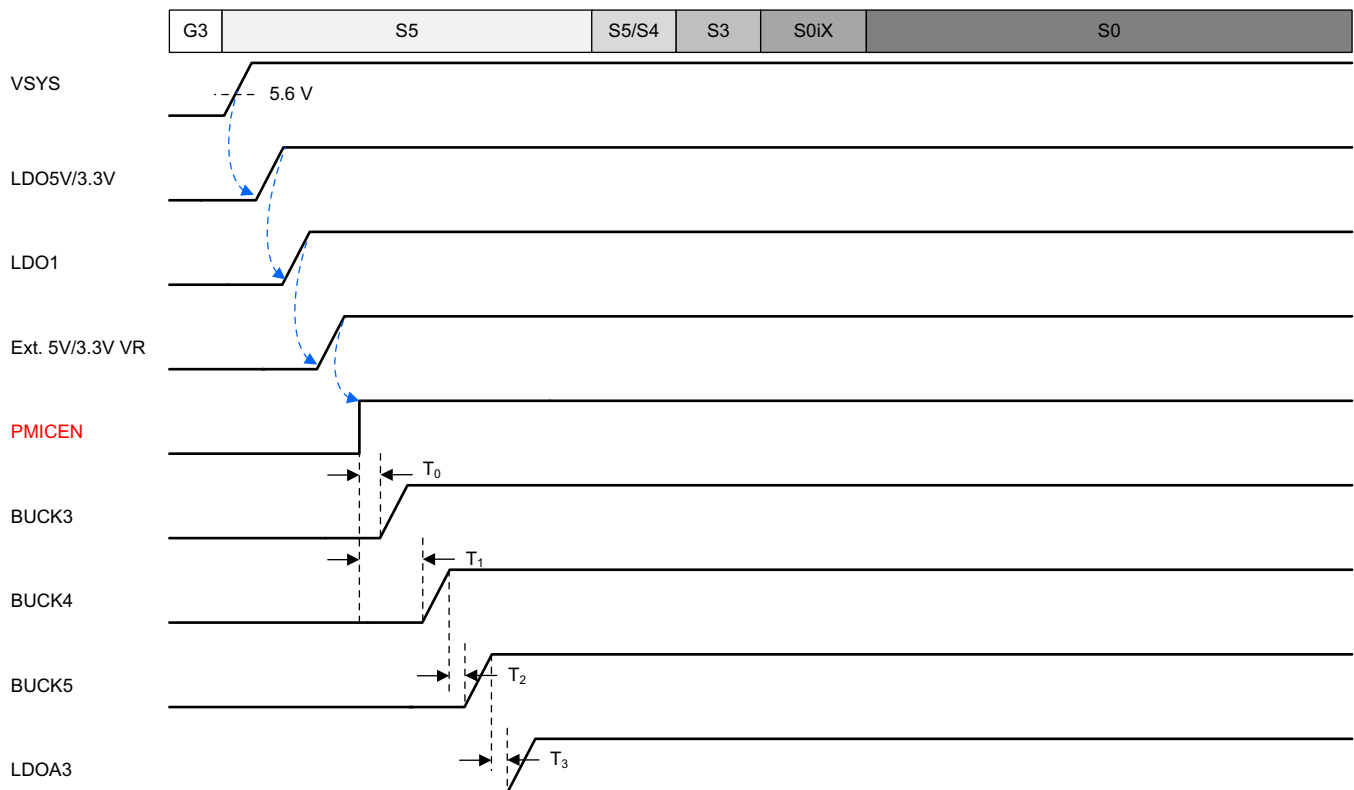


Figure 3. An Example of a Power-Up Sequencing for SoC

7 System Monitor and Fault Handling

Supply and fault monitoring is critical for any system. Faults like channels, under voltage and overvoltage, IC over-temperature, and main supply UVLO thresholds can be damaging to the system. A PMIC can detect all these faults and take immediate action without waiting for the main processor to take control to avoid system or power failure. When a fault is detected, it is communicated to the main processor; in parallel, a graceful shutdown sequence is initiated by the PMIC to enter a low-power mode.

8 Summary

PMICs offer a great solution for solving the complex problem of system power delivery in today's processor platforms. With the high integration, low system cost, small area, and system flexibility, a PMIC is a great solution for any ARM, FPGA, or x86-based system. Systems requirements are becoming more constrained. PMICs offer many features that meet these requirements like integrated sequencing, DVS control, fault control, power good, battery chargers, and more. All these features empower smaller, more robust, cost effective, and power efficient systems. Texas Instruments offers a wide and strong portfolio of PMICs for processor and system power.

9 References and Related Documentation

[Texas Instruments Power Management Multi-Channel IC \(PMIC\) Solutions](#)

[TPS65218](#)

[TPS65023](#)

[TPS650860](#)

Revision History

Changes from June 17, 2015 to October 31, 2015	Page
<ul style="list-style-type: none"> Changed <i>Example of a DVS and Decay-Mode Timing Diagram</i> 	4

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com